MICRO ELECTRONICS

1978 DATA CATALOG

GENERAL INSTRUMENT CORPORATION ▪ MICROELECTRONICS

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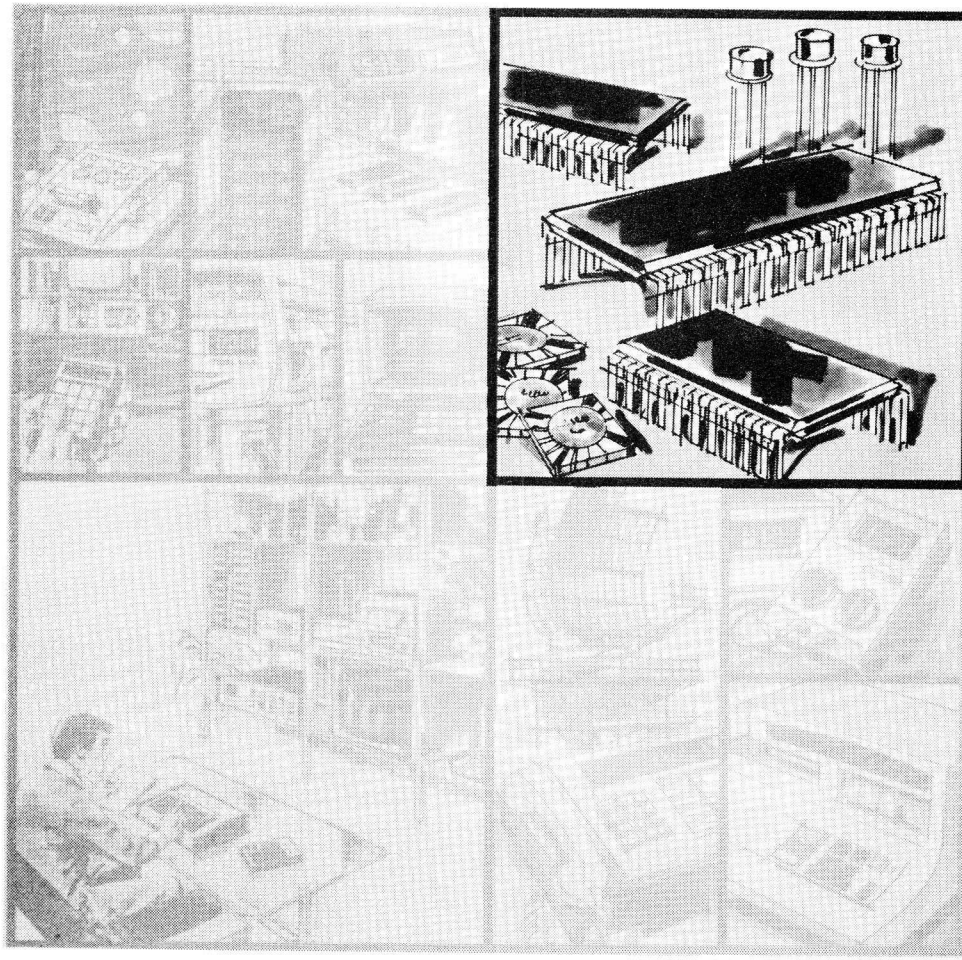

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Microprocessor 2

MICROPROCESSOR - 2		Series 8000 LSI Circuits				
FUNCTION	DESCRIPTION	PART NUMBER	SYSTEM FUNCTION	PACKAGE	FEATURES	PAGE NO.
8 BIT MICRO-PROCESSOR SYSTEM	The LP8000 Logic Processor is a complete 8-bit single chip microprocessor with 48 general purpose internal registers. The 8-bit data bus is supplemented by a 6-bit address bus to give a 14-bit address capability.	LP8000	PROCESSOR	40 DIP	Two chip minimum system consisting of the LP8000 Processor and the LP6000 Program Memory (plus clock). 48 basic instructions. Binary and decimal arithmetic. Direct and indirect I/O capability. Automatic subroutine nesting on memory devices.	2-52
		LP6000	PROGRAM MEMORY	40 DIP		2-52
		LP1030	CLOCK GENERATOR	8 DIP		2-52
		LP1010	I/O BUFFER	40 DIP		2-52
		LP1000	MEMORY INTERFACE	40 DIP		2-52

MICROPROCESSOR - 2 Series 1600 LSI Circuits

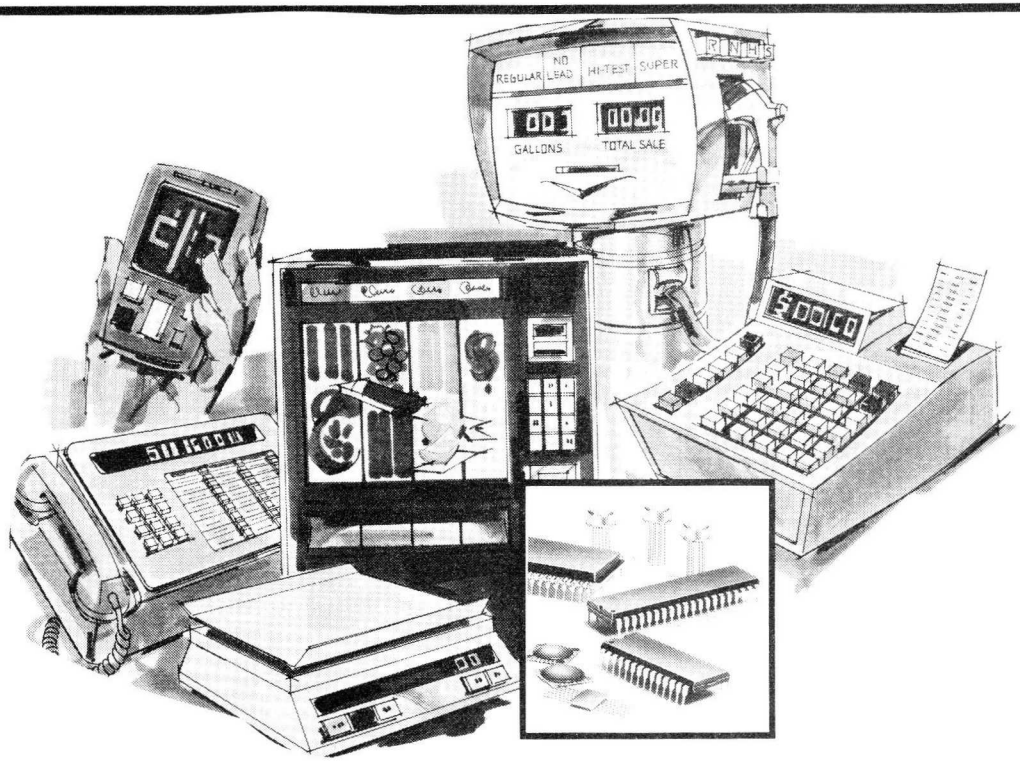
FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
16 BIT SINGLE CHIP MICRO-PROCESSOR	The CP1600 utilizes third generation minicomputer architecture with 8 general purpose registers. The 16-bit word enables fast and efficient processing of alpha-numeric or byte oriented data. The 16-bit address capability permits access to 65,536 words of memory or peripheral devices.	CP1600	40 DIP	8 program accessible 16-bit general purpose registers. 87 basic instructions. 4 addressing modes. Unlimited interrupt nesting and priority resolution. 16-bit 2's complement arithmetic and logic. Direct memory access (DMA) for high speed data transfer. 65K memory using single address. Cycle times: 600ns (CP1600), 500ns (CP1600A), 1μs (CP1610).	2-4
		CP1600A	40 DIP		2-4
		CP1610	40 DIP		2-4
DIGITAL TO ANALOG CONVERTER	Contains 4 registers which can be loaded or read through a 10-bit I/O port.	DAC 1600	40 DIP	10-bit bidirectional data bus. Synchronous/asynchronous loading. Manual input mode. Designed to interface to a process control loop.	2-12
INPUT/ OUTPUT BUFFER	A programmable buffer in which data is transferred to/from a peripheral on 16 bidirectional lines.	IOB 1680	40 DIP	Single 16-bit or dual 8-bit I/O ports. Parity check on both ports. Three levels of priority. Automatic handshake logic and signals.	2-16
18 CHANNEL ANALOG MULTIPLEXER	A binary addressed mux which includes an on-chip address latch.	MUX 1600	28 DIP	Connects 1 of 18 analog inputs. On-chip address latch. 0 to 6 Volt input range. Analog output controlled by chip select signal.	2-22
NEW READ ONLY MEMORIES	A series of 20K ROMs, organized 2048 x 10, which feature a single 16-bit bus for both address and data.	RO-3-9500	28 DIP	Includes on-chip address latches, bus control logic, and 5-bit chip select decode.	2-24
		RO-3-9501	40 DIP	Above, plus a separate 10-bit output address latch for controlling up to 1K of external RAM.	2-24
		RO-3-9502	40 DIP	Above, except external RAM output address latch is a full 16 bits.	2-24

MICROPROCESSOR - 2 Series 1600 Hardware

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
GIMINI SINGLE CARD MICRO-COMPUTER	Provides full 16-bit processing power on a single card; a complete operating system.	SC1600	12⅞" × 17" PC Board	16K words of RAM. 14K words of PROM sockets. 1K words of EAROM. Up to 16 input and 16 output lines. UAR/T-RS232 serial I/O channel. Real-time clock.	2-31
GIMINI MICRO-COMPUTER SYSTEMS	A modular design for maximum configurability; all control/ timing signals and buses are fully buffered.	GIMINI	13 Board Positions	Complete microcomputer system. Separate data, address, and control buses. Up to 65K memory space. Unlimited DMA channels. Nested interrupt system with full priority resolution. GIMINI II has integral power supply.	2-32
NEW		*GIMINI II	7 Board Positions		2-32
GIMINI PC MODULES	Analog to Digital Module	AD1600	9¼" x 9¼" PC Board	±10V, 12 bit A/D. Standard conversion rate of 25kHz.	2-34
	Control Console Module	CC1600		All panel control logic including memory and switch/display registers.	2-35
	Digital to Analog Module	DA1600		±10V, 12 bit D/A. Four D/A's are provided on one module.	2-36
	General Purpose Module	GP1600		Two addressable 16 bit ports with two addressable status registers.	2-37
	Reader-Punch Interface	I/O1600		TTY-EIA interface. Four channels with interrupt logic.	2-38
NEW	Floppy Disc Interface	*I/O1610		Two serial and one parallel I/O port with interrupt logic.	2-39
	Microcomputer Module	MC1600		Complete processing unit with clocks and buffered buses.	2-40
NEW	Microcomputer Module	*MC1610		Above, plus contains the monitor operating system.	2-41
	PROM Memory Module	PM1600		16 4K PROM sockets for a maximum 4K x 16 memory.	2-42
NEW	PROM Programmer Module	*PP1610		Programs two 2708 or 2716 UV PROMs.	2-43
	RAM Memory Modules	RM1601/02		8K x 16 memory: static (RM1601) or dynamic (RM1602).	2-44
NEW	RAM Memory Module	*RM1610		Selectable 8K/16K/32K x 16 memory.	2-46

*For future release.

Microcomputer 3



MICROCOMPUTER - 3	SBA Series LSI Circuits				
FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
1 BIT SINGLE CHIP MICRO-COMPUTER	The SBA can directly evaluate a set of Boolean equations. Thirty programmable inputs and outputs as well as memory make the SBA a true 1-bit microcomputer.	**SBA**	40 DIP	24 basic instructions including AND, OR, XOR, COMPARE, INVERT. 1023 words of ROM program. 30 programmable inputs, outputs or multiplexed inputs/outputs. 16 element stack. 120 element read/write memory.	**3-30**
SINGLE CHIP DEVELOPMENT MICRO-COMPUTER	SBA microcomputer without ROM.	**SBA-1**	64 DIP	ROM data lines are brought out to pins to allow the use of any external RAM or PROM to aid in program development.	**3-41**

MICROCOMPUTER - 3	SBA Series Hardware / Software				
FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
SBA FIELD DEMO SYSTEM	Contains an SBA-1, a program counter, and sockets for 5 IK PROMs.	**SBA-FD**	7½" x 9" PC Board	Includes demultiplexing circuitry for the 30 I/O lines with DIP switches for changes in I/O assignment.	**3-42**
SBA COMPILER	Converts a list of Boolean equations to optimized SBA code.	**SBACOMP**	—	Produces two output files, one of which may be used directly with the SBA simulation program SBASIM. Available in either Host System or CP1600 assembly language for a GIMINI system.	**3-43**
SBA SIMULATOR	Simulates all SBA actions for program debug and verification.	**SBASIM**	—	Available in either a Host System version or in CP1600 assembly language for execution on a GIMINI microcomputer.	**3-48**

MICROCOMPUTER - 3 — PIC Series LSI Circuits

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
8 BIT SINGLE CHIP MICRO-COMPUTER	The PIC 1650 series of single chip microcomputers contain RAM, I/O, and a central processing unit as well as a customer defined ROM to specify the overall functional characteristics of the device.	**PIC 1650**	40 DIP	User programmable. 32 8-bit registers. 512 x 12-bit ROM for program. Arithmetic logic unit. 4 sets of 8 user-defined TTL compatible input/output lines. Self-contained oscillator. Single +5V power supply.	**3-4**
		***PIC 1645**	18 DIP	All the features of the PIC 1650 but with less ROM (256 × 12), fewer I/O lines (4 in, 4 out, 4 I/O) and registers (24). Plus external interrupt capability.	**3-13**
		PIC 1655	28 DIP	All the features of the PIC 1650 but with fewer I/O lines (4 in, 8 out, 8 I/O).	**3-14**
		***PIC 1670**	40 DIP	All the features of the PIC 1650 but with double the amount of ROM (1024 x 12) and a 4 level stack area.	**3-15**
SINGLE CHIP DEVELOPMENT MICRO-COMPUTER	PIC 1650 microcomputer without ROM and with the addition of a HALT pin.	**PIC 1664**	64 DIP	ROM address and data lines are brought out to pins to allow the use of any external RAM or PROM to aid in program development. Can be stopped or single-stepped.	**3-16**

*For future release.

MICROCOMPUTER - 3 — PIC Series Hardware

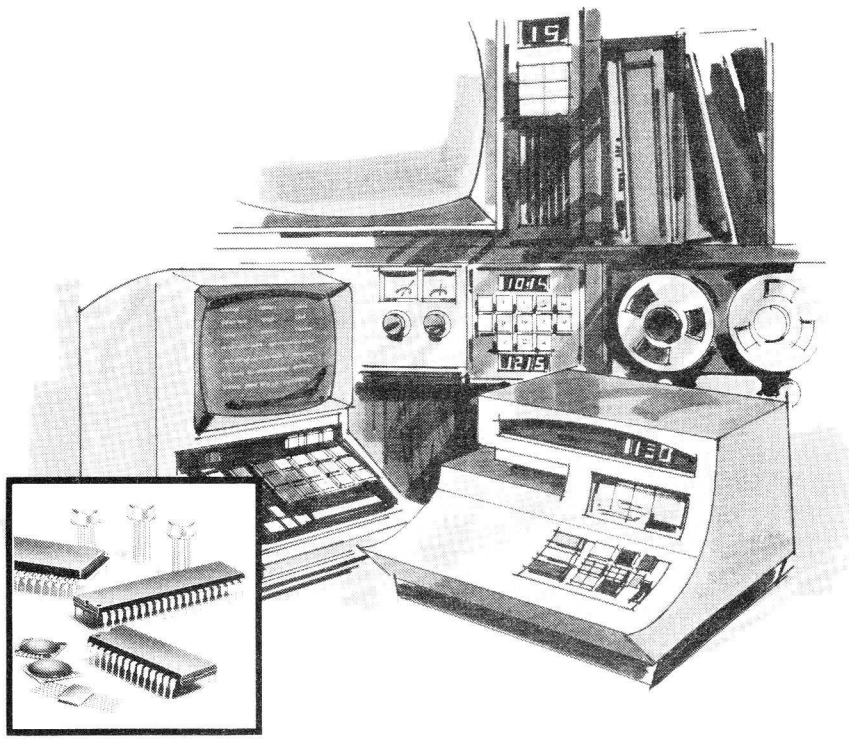
FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
PIC DEVELOPMENT SYSTEM	Contains a pre-programmed PIC 1650, a PIC 1664, 512 x 12 RAM, a TTY interface, and a cabled 40 pin DIP plug.	**DB1650**	8" x 8½" PC Board	The pre-programmed PIC 1650 contains PICBUG, a program which enables loading a PIC 1650 program and providing in-circuit emulation capability and full debug commands.	**3-19**
PIC FIELD DEMO SYSTEM	Contains a PIC 1664 and sockets for external PROMs. Provision for an on-board RC oscillator or external clock.	**FD1664**	4" x 6½" PC Board	Supplied with a ribbon cable terminated in a 40 pin DIP plug, to demonstrate a PIC system before committing to a masked ROM.	**3-20**

MICROCOMPUTER - 3 — PIC Series Software

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
PIC ASSEMBLER	Converts symbolic source programs for the PIC 1650 into suitable code.	**PICAL**	—	Produces a binary paper tape output which may be loaded and executed by the DB1650 or used to directly mask program a PIC chip. Available in either Fortran IV or CP1600 assembly language for a GIMINI system.	**3-21**
PIC SIMULATOR	Simulates all PIC instructions for program debug and verification.	**PICSIM**	—	Available in either Fortran IV or CP1600 assembly language for execution on a GIMINI microcomputer.	**3-24**

FUNCTIONAL INDEX

Memory 4



MEMORY - 4 Random Access Memories

FUNCTION	DESCRIPTION	PART NUMBER	ACCESS TIME	CYCLE TIME	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
1K RAM	1,024 bits organized 256 x 4	**RA-3-4256**	500ns	500ns	+5	24 DIP	Power-down mode.	**4-4**
		RA-3-4256A	650ns	650ns	+5	24 DIP	Power-down mode.	**4-4**
		RA-3-4256B	650ns	650ns	+5	22 DIP		**4-4**

MEMORY - 4 Electrically Alterable Read Only Memories

	FUNCTION	DESCRIPTION	PART NUMBER	READ ACCESS	ERASE TIME	WRITE TIME	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
	512 BIT EAROM	512 bits organized 32 x 16	**ER2051**	3μs	50ms	50ms	+5, −28	28 DIP	Word erase.	**4-18**
NEW		512 bits organized 64 x 8	**ER2055**	4μs	50ms	50ms	+5, −28	22 DIP	Word erase.	**4-21**
NEW	IK RAM/EAROM	1,024 bits organized 256 x 4	**ER1711**	900ns	16ms	16ms	+5, −12	22 DIP	Cycle time: 1.5μs	**4-13**
	1400 BIT SERIAL EAROM	1,400 bits organized 100 x 14	**ER1400**	2.8μs	16ms	16ms	−35	14 DIP	Word erase.	**4-10**
	4K EAROM	4,096 bits organized 1,024 x 4	**ER2401**	2μs	100ms	10ms	±5, −14, −24	24 DIP	Bulk erase.	**4-24**
			ER3400	900ns	10ms	1ms	+5, −12, −30	22 DIP	Word/bulk erase.	**4-36**
	8K EAROM	8,192 bits organized 2,048 x 4	**ER2805**	1.65μs	100ms	10ms	±5, −14, −24	24 DIP	Bulk erase.	**4-30**

MEMORY - 4 Read Only Memories

FUNCTION	DESCRIPTION	PART NUMBER	REPLACES	ACCESS TIME	CLOCKS / VOLTAGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
2K ROM	2,560 bits organized 512 x 5	**RO-3-2560**	—	450ns	Static	+5	18 DIP		**4-42**
4K ROM	4,096 bits organized 512 x 8	**RO-3-4096**	—	500ns	Static	+5	22 DIP		**4-44**
5K ROM	5,120 bits organized 512 x 10	**RO-3-5120**	EA4000	500ns	Static	+5	24 DIP		**4-46**
8K ROM	8,192 bits organized 2,048 x 4	**RO-5-8192**	AMI S8865	1.2μs (typ.)	2/TTL	+5, −12	24 DIP		**4-48**
16K ROM	16,384 bits organized 2,048 x 8	**RO-3-8316A**	INTEL 8316A AMI S6831A	850ns	Static	+5	24 DIP		**4-51**
		RO-3-8316B		450ns					**4-51**
		RO-3-9316A	INTEL 8316E AMI S6831B SY2316B	850ns	Static	+5	24 DIP	Replaces 2716 UV EPROM.	**4-51**
		RO-3-9316B		450ns					**4-51**
		RO-3-9316C		350ns					**4-51**
	16,384 bits organized 4,096 x 4	**RO-3-16384**	AMI S8996	1μs	Static	+5	24 DIP	Address latch.	**4-60**
NEW 32K ROM	32,768 bits organized 4,096 x 8	**RO-3-9332A**	TMS4732 SY2332 SIG 2633	850ns	Static	+5	24 DIP		**4-56**
		RO-3-9332B		450ns					**4-56**
		RO-3-9332C		350ns					**4-56**
NEW 64K ROM	65,536 bits organized 8,192 x 8	***RO-3-9364B**	MK36000	450ns	Static	+5	24 DIP	Edge-activated.	**4-59**

*For future release.

Note: All Read Only Memories are mask-programmable.

MEMORY - 4 Keyboard Encoders / Character Generators

FUNCTION	DESCRIPTION	PART NUMBER	REPLACES	ACCESS TIME	CLOCKS / VOLTAGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits.	**AY-5-2376**	SMC KR2376	10-100kHz Scan rate	1/TTL or Int. Osc.	+5, −12	40 DIP	2 key rollover.	**4-64**
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	**AY-5-3600**	SMC KR3600	10-100kHz Scan rate	1/TTL or Int. Osc.	+5, −12	40 DIP	2/N key rollover.	**4-69**
		AY-5-3600-PRO	—					Preprogrammed binary codes.	**4-75**
NEW CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	**AY-3-4592**	—	11-66kHz Scan rate	1/TTL or Int. Osc.	+5	40 DIP	Also usable: inductive, Hall effect, mechanical switches.	**4-78**
CHARACTER GENERATORS	2,240 bits organized as 64 - 5 x 7 characters.	**RO-5-2240S**	MK2302 FSC3257	1μs (typ.)	1/TTL for Scanning	+5, −12	24 DIP	Column output, on-chip scan.	**4-88**
	2,560 bits organized as 64 - 5 x 8 characters.	**RO-3-2513**	SIG 2513	450ns	Static	+5	24 DIP	Row output.	**4-92**
	5,184 bits organized as 64 - 9 x 9 characters.	**RO-5-5184**	—	5μs (typ.)	1/TTL for Scanning	+5, −12	24 DIP	On-chip left/right scanning.	**4-97**

Note: All Keyboard Encoders and Character Generators are mask programmable. Standard patterns are available.

MEMORY - 4 Static Shift Registers

FUNCTION	DESCRIPTION	PART NUMBER			MAXIMUM FREQUENCY	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
		0 to 70°C	−55 to +125°C	0 to 70°C					
VARIABLE	32 bit variable length.	**SS-5-1032**	**SS-6-1032**	—	1MHz	+5, −12	16 DIP	1, 1, 2, 4, 8, 16 S/R.	**4-106**
DUAL REGISTERS	Dual 16 bit.	**SS-5-8211**	**SS-6-8211**	**SS-7-2016**	2MHz	+5, −12	16 DIP	Dual data input.	**4-124**
		SS-5-8212	**SS-6-8212**	**SS-7-8212**	2MHz	+5, −12	14 DIP, 8 TO		**4-126**
	Dual 50 bit.	**SL-5-2050**	**SL-6-2050**	**SL-7-2050**	1MHz	+5, −12	14 DIP, 8 TO		**4-108**
	Dual 64 bit.	**SL-5-2064**	**SL-6-2064**	**SL-7-2064**	1MHz	+5, −12	14 DIP, 8 TO		**4-110**
	Dual 100 bit.	**SL-5-C2100**	—	**SL-7-C2100**	2MHz	+5, −12	14 DIP, 8 TO		**4-112**
	Dual 128 bit.	**SL-5-2128**	—	**SL-7-2128**	1MHz	+5, −12	14 DIP, 8 TO		**4-114**
		SL-5-C2128	—	—	2MHz	+5, −12	14 DIP, 8 TO		**4-116**
QUAD REGISTERS	Quad 16 bit.	**SL-5-4016**	—	**SL-7-4016**	2MHz	+5, −12	14 DIP		**4-118**
	Quad 25 bit.	**SL-5-4025**	**SL-6-4025**	**SL-7-4025**	1MHz	+5, −12	14 DIP		**4-120**
	Quad 32 bit.	**SL-5-4032**	**SL-6-4032**	**SL-7-4032**	1MHz	+5, −12	14 DIP		**4-122**

SS-7/SL-7 Series available only in Europe.

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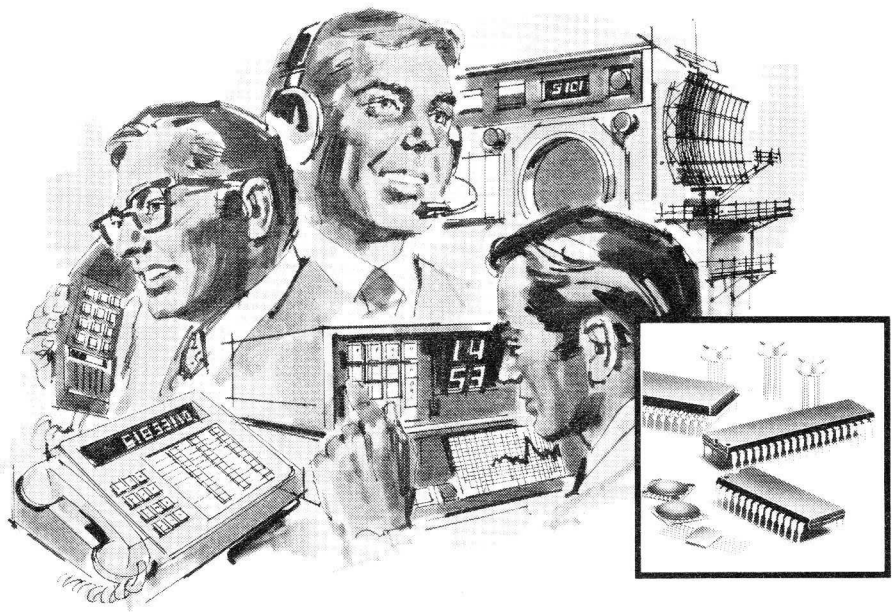
Telecommunications 5



TELECOMMUNICATIONS - 5 Telecom Hybrids

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
UNIVERSAL ACTIVE FILTERS	Generate any filter response by means of external connections.	ACF 7032C	16 TO	The design provides for independent control of Frequency, Q, and Amplifier Gain, and is usable throughout the frequency range of 10Hz to 10kHz.	5-48
		ACF 7092C	16 DIP		5-48
NEW LOW PASS FILTERS	PCM transmit filters.	ACF 7270C	8 SIP	Minimum 32 dB attenuation at 4.2kHz and an in-band ripple of ±0.125 dB from 300Hz to 3kHz. ACF 7272C also includes 60Hz attenuation.	5-52
		*ACF 7272C	14 SIP		5-56
	PCM receive filters	ACF 7271C	8 SIP	Minimum 32 dB attenuation at 4.2kHz. Compensated for sinx/x response. ACF 7273C also includes gain adjust input.	5-54
		*ACF 7273C	14 SIP		5-57
BAND PASS FILTERS	Full wave detector and a factory tunable four pole fixed bandwidth band pass filter.	ACF 7300C	14 DIP	Center frequency range (F_o): 540Hz to 1980Hz.	5-58
		ACF 7301C		Center frequency range (F_o): 700Hz to 1700Hz.	5-60
		ACF 7302C		Center frequency range (F_o): 2280Hz to 3825Hz.	5-62
	Detects and passes the 2600Hz signalling frequency.	ACF 7310C	28 DIP	Minimum attenuation from center frequency of 2600Hz: 30 dB ±200Hz, 50 dB ±500Hz, 70 dB ±1000Hz.	5-64
	DTMF/tone detection band pass filters.	ACF 7323C	12 TO	These two pole constant Q filters are available in the standard AT&T tone frequencies and in the standard MF steps.	5-66
		ACF 7363C	10 SIP		5-66
		ACF 7383C	16 DIP		5-66
BAND REJECTION FILTERS	Dial tone suppression, rejects frequencies of 350 and 440Hz.	*ACF 7401C	20 DIP	Provides for 0 dB insertion loss in the pass band of 697Hz through 1633Hz. Also provides 60Hz attenuation.	5-68
	Rejects the 2600Hz signalling frequency.	ACF 7410C	34 DIP	Minimum attenuation of 60dB ±15Hz from the center frequency of 2600Hz.	5-69
BAND SEP FILTER	Isolates low and high groups of DTMF frequencies.	ACF 7711C	16 DIP	Minimum attenuation of 30 dB for the adjacent frequencies of 941Hz and 1209Hz. 0 dB in the pass bands, 25 dB out of band.	5-70

*For future release.

TELECOMMUNICATIONS - 5 Telephony

	FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
	5 CHANNEL RELAY DRIVER	Isolates +5V logic and exchange-powered relays.	AY-5-9050	+5, −48	14 DIP	Separate logic and exchange grounds, each driver is capable of supplying 50mA.	5-4
	PUSH BUTTON TELEPHONE DIALLERS	Converts push button input to rotary dial pulses.	AY-5-9100	See data sheet.	18 DIP	20 digit storage, selectable dialling rate, selectable mark/space ratio, selectable inter-digital pause. Redial of last number and access pause facility (except on AY-5-9118).	5-7
			AY-5-9106		18 DIP		5-7
			AY-5-9110		18 DIP		5-7
			AY-5-9118		14 DIP		5-7
			AY-5-9120		18 DIP		5-7
			AY-5-9151/52	+2.5 to +5	18 DIP		5-14
			AY-5-9153/54		28 DIP		5-14
			AY-9-9600	−1.5 to +8	16/22 DIP		5-33
	REPERTORY DIALLER	Stores ten 22 digit telephone numbers.	AY-5-9200	See data sheet.	16 DIP	Complements the AY-5-9100 series to provide storage of up to ten 22 digit telephone numbers. Stackable.	5-20
	DUAL-TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	+5	14 DIP	12 tone pairs, 3.52dB high group pre-emphasis.	5-26
			AY-3-9401		16 DIP	16 tone pairs, 2dB high group pre-emphasis.	5-26
			AY-3-9410		16 DIP	16 tone pairs, 3 or 6dB high group pre-emphasis.	5-26
			*AY-9-9086	+1.5 to +8	16 DIP	16 tone pairs, 3.58 MHz crystal reference.	5-6
	CLOCK GENERATOR	Generates 2-phase clocks from a single power supply.	AY-5-9500	−4 to −15	14 DIP	Generates the 2-phase clocks for the AY-5-9100/9200.	5-29
	DUAL-TONE MULTI-FREQUENCY RECEIVERS	Detects and converts DTMF/ tone telephone frequencies.	AY-5-9801/21	+8.5, −8.5	28 DIP	4 bit output code, on-chip Op Amps.	5-34
			AY-5-9802/22		40 DIP	1 of 16 output code, on-chip Op Amps.	5-34
			AY-5-9803/23		40 DIP	2 of 8 output code, on-chip Op Amps.	5-34
			AY-5-9804/24		28 DIP	Binary output code, on-chip Op Amps.	5-34
			AY-5-9805/25		24 DIP	4 bit output code.	5-34
			AY-5-9806/26		40 DIP	1 of 16 output code.	5-34
			AY-5-9807/27		24 DIP	2 of 8 output code.	5-34
			AY-5-9808/28		24 DIP	Binary output code.	5-34
NEW	CODEC	Duplex Delta-Sigma/PCM converter.	AY-3-9900	+9, +5	24 DIP	With external D-S modulator, provides full duplex PCM. Pin-selectable A-Law/μ-Law.	5-39
NEW	MICRO-COMPUTER DIALLER	A single-chip microcomputer pre-programmed for in-telephone applications.	TZ2001	+5	40 DIP	Push button dialling (pulse output), display of up to 12 dialled digits, 32 telephone number storage with one button selection, 6 digit clock and elapsed time display, provision for add-on of scientific calculator (C/CF-599).	5-45

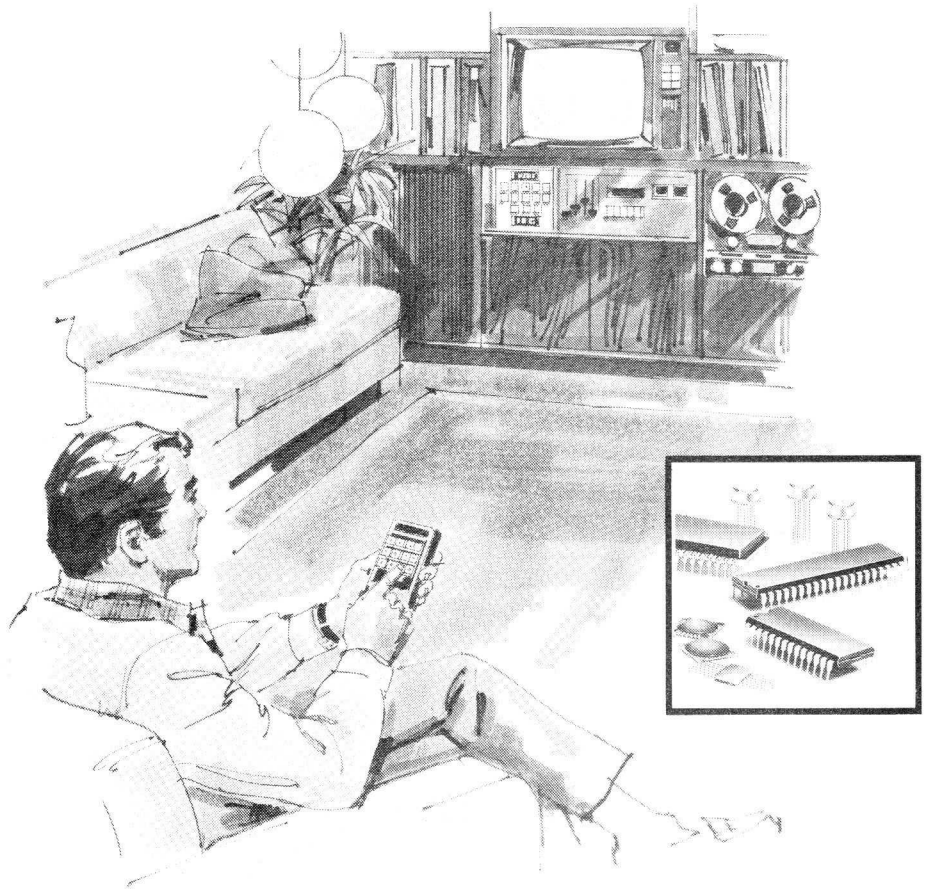
*For future release.

TELECOMMUNICATIONS - 5 Data Communications

FUNCTION	DESCRIPTION	PART NUMBER	MAXIMUM BAUD	MAXIMUM FREQUENCY	TEMP. RANGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
UAR/T	Complete 5-8 bit receiver/ transmitter interface.	AY-5-1013A	40kB	640kHz	0 to 70	+5, −12	40 DIP	1 or 2 stop bits.	5-74
		AY-6-1013	22.5kB	360kHz	−55 to +125	+5, −12			5-74
		AY-3-1014A	30kB	480kHz	0 to 70	+5 to +14		1, 1½, or 2 stop bits	5-74
		AY-3-1015D	30kB	480kHz	0 to 70	+5			5-74
P/SAR	Programmable receiver interface.	AY-8-1472B	640kB	640kHz	0 to 70	+5, −12	40 DIP	Programmable mode selection and trans-mission codes.	5-87
P/SAT	Programmable transmitter interface.	AY-8-1482B	640kB	640kHz	0 to 70	+5, −12	40 DIP		5-94
16 CHANNEL MULTIPLEXER	Multiplexes 16 analog chan-nels with on-chip logic control.	AY-5-1016	—	2MHz	0 to 70	+5, −12	40 DIP	Current mode or voltage mode.	5-102
		AY-6-4016			−55 to +125				5-102

FUNCTIONAL INDEX

Entertainment 6



ENTERTAINMENT - 6 Radio

	FUNCTION	DESCRIPTION	PART NUMBER	AM/MW/SW IF OFFSET	FM/VHF IF OFFSET	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
	FREQUENCY COUNTERS	Counts & displays MW, SW, and VHF frequencies.	AY-5-8100	460kHz	10.7MHz	+5, −12	28 DIP	4½ digit display drive, 0-99 FM channel mode.	6-4
			AY-5-8102	455kHz					6-4
	FREQUENCY COUNTERS WITH CLOCK	Counts and displays AM/FM frequencies, with a 4-digit clock.	AY-3-8110	262.5kHz	10.46 to 10.76MHz	+10 to +16	28 DIP	12 hr. clock, 10kHz AM steps, 200kHz FM steps.	6-8
			AY-3-8112	455kHz					6-8
NEW			AY-3-8114	455kHz				24 hr. clock, 100kHz FM steps.	6-8
	FUNCTION	**DESCRIPTION**	**PART NUMBER**	**SYSTEM FUNCTION**		**SUPPLY VOLTAGES**	**PACKAGE**	**FEATURES**	**PAGE NO.**
	STEREOMEGA PLL DIGITAL TUNING SYSTEM	Provides full electronic control of a varactor-tuned AM/FM radio. Includes storage of 5 AM & 5 FM "favorite" stations.	AY-3-8115	CONTROLLER		+10 to +13	40 DIP	Provides PLL capability on-chip freq. division, reference osc.	6-12
			ER1400	EAROM MEMORY		+12, −24	14 DIP	Non-volatile storage of station tuning information.	6-20
			AY-3-8116	CLOCK		+5 to +13	28 DIP	12 hour clock, time or frequency select inputs.	6-23
NEW			AY-3-8117	DISPLAY DRIVER		+9 to +13	40 DIP	Latches & decodes multiplexed display data.	6-26

ENTERTAINMENT - 6 Television

FUNCTION	DESCRIPTION	PART NUMBER	SYSTEM FUNCTION	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
OMEGA 82 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 82-channel television from a two-digit calculator-like keyboard entry.	T-1002	CONTROLLER	+12	40 DIP	Accepts keyboard/remote inputs to control system.	6-30
		T-1102	DISPLAY DRIVER	+12	40 DIP	Stores, decodes, displays selected channel number.	6-30
		ER1400	EAROM MEMORY	+12, −24	14 DIP	Non-volatile storage of station tuning information.	6-34
		MEM 4956	D/A CONVERTER	+12, V_{REF}	14 DIP	Converts output to coarse and fine tune outputs.	6-37
		T-1201	FAVORITE CHANNEL MEMORY	+12	40 DIP	A 20-line EAROM for single-digit channel selection.	6-30
ECONOMEGA 16 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 8, 12 or 16 channel television, featuring automatic or manual tuning.	AY-3-8203	CONTROLLER	+12	40 DIP	Accepts direct/remote inputs to control system.	6-40
		ER1400	EAROM MEMORY	+12, −24	14 DIP	Non-volatile storage of station tuning information.	6-34
		MEM 4956	D/A CONVERTER	+12, V_{REF}	14 DIP	Converts output to coarse and fine tune outputs.	6-37

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
ON-SCREEN CHANNEL/TIME DISPLAY	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display (ref. AY-5-1203A clock circuit)	AY-5-8300	+18	14 DIP	Channels 0-15, upper right screen display.	6-46
		AY-5-8301			Channels 1-16, upper right screen display.	6-46
		AY-5-8310	+18	24 DIP	Channels 0-15 or 00-99 or time, upper right screen display.	6-46
		AY-5-8311	+12			6-46
		AY-5-8320	+18		Channels 1-16 and/or time, upper right screen display, automatic on channel change.	6-46
		AY-5-8321	+12			6-46
		AY-5-8322	+13	24 DIP	Channels 1-16 and/or time, lower center screen display, automatic on channel change.	6-46
		AY-5-8324				6-46
NEW ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor-tuned TV sets.	AY-3-8330A	+12	16 DIP	Four bands, mask-programmable band or channel number display and display position.	6-57
		AY-3-8331				6-57
		AY-3-8335				6-57

ENTERTAINMENT - 6 Remote Control

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
R/C SYSTEM I	30 channel discrete frequency ultrasonic transmitter.	SAA 1024	+9	16 DIP	30 ultrasonic control frequencies in the range 34-44kHz. Crystal controlled.	6-62
	30 channel discrete frequency ultrasonic receiver.	SAA 1025	+18	16 DIP	16 TV channel selection (& 5 spares), on/off signal, 8 analog functions.	6-64
R/C SYSTEM II	23 channel PCM ultrasonic or infrared transmitters.	AY-5-8410	+15	18 DIP	23 control channels, either local control at receiver (AY-5-8410) or remote control (AY-5-8411).	6-68
		AY-5-8411	+9			6-68
	31/63 channel PCM ultrasonic or infrared receiver.	AY-5-8420	+15	14 DIP	5 or 6 bit modes, error-detection, on-chip oscillator, LED "receive" driver output.	6-70
R/C SYSTEM III	30 channel discrete frequency ultrasonic transmitter.	AY-5-8450	+9	16 DIP	30 ultrasonic control frequencies, interfaces with a 5 x 6 matrix keyboard.	6-72
	16 channel discrete frequency ultrasonic receivers.	AY-5-8460	+12, −6	18 DIP	Interfaces directly with OMEGA keyboard, plus on/off, recall, 4 analog functions.	6-74
		AY-5-8461				6-74
R/C SYSTEM IV	264 command PCM infrared transmitter.	*AY-3-8470	+9	28 DIP	8-bit PCM system plus 8 PWM analog commands. 4 x 8 keyboard (32 x 8 with shifts).	6-78
	264 command PCM infrared receiver.	*AY-3-8475	+12	40 DIP	5-bit program output. CPU data bus interface for full 264 functions.	6-81

*For future release.

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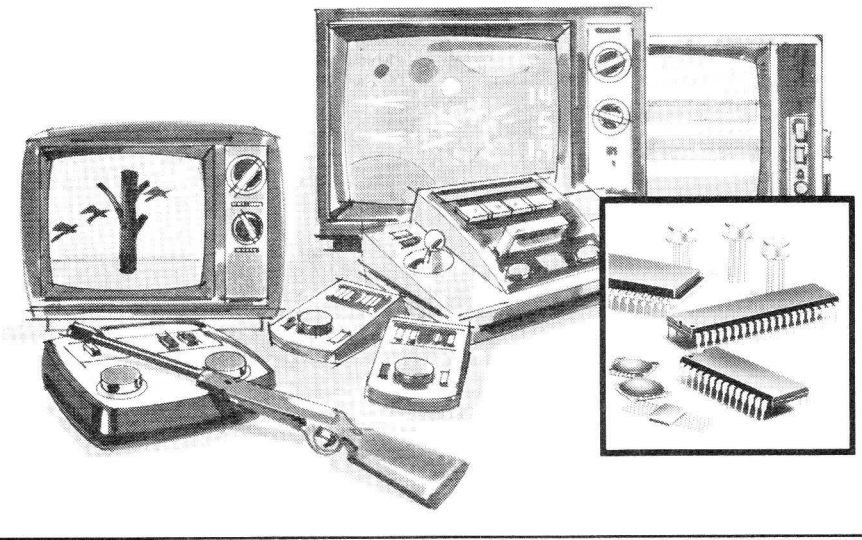
TV Games 7



TV GAMES - 7 Dedicated TV Games

	FUNCTION	DESCRIPTION	PART NUMBER	GAMES	LINE STANDARD	PACKAGE	FEATURES	PAGE NO.
	BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500	Tennis Practice Soccer Rifle I Squash Rifle II	625	28 DIP	On-screen scoring. Sound generation. Selectable paddle size, ball speed, rebound angles.	7-4
			AY-3-8500-1		525			7-4
	BALL & PADDLE (TWO AXIS)	Six selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8550	Tennis Practice Soccer Rifle I Squash Rifle II	625	28 DIP	Above, plus color-coding of score and player, and "hit" and "miss" scoring in Practice game.	7-16
			AY-3-8550-1		525			7-16
	COLOR PROCESSOR	Adds color to the AY-3-8500-1 and AY-3-8550-1.	AY-3-8515	—	525	16 DIP	Colors changed by the "game select" inputs.	7-25
NEW	ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603	Roadrace Qualify	625	28 DIP	Each player maneuvers around other cars on the race track. Color display with the AY-3-8615.	7-26
			AY-3-8603-1		525			7-26
NEW	WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605	Sea Battle Counterattack I&II Night Battle Space Battle I&II	625	28 DIP	Fire depth charges, missiles, and torpedoes. Varied skill selection. Color display with the AY-3-8615.	7-28
			AY-3-8605-1		525			7-28
NEW	WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606	Wipeout I - IV Color Squares I - IV Breakthrough I&II	625	28 DIP	Skill selection including paddle size, ball size, and ball speed. Color display with the AY-3-8615.	7-32
			AY-3-8606-1		525			7-32
NEW	SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607	Skeet I - IV Attack I - IV Destruct I - IV	625	28 DIP	Three dimensional target effect by diminishing target size. Color display with the AY-3-8615.	7-36
			AY-3-8607-1		525			7-36
	SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610	Tennis Practice Hockey Gridball Soccer Basketball I&II Squash Target I&II	625	28 DIP	Realistic ball service & scoring. Individually selectable paddle sizes. Color-coded score. Color display with the AY-3-8615.	7-40
			AY-3-8610-1		525			7-40
	COLOR PROCESSOR	Adds color to the "8600" series dedicated TV Game circuits.	AY-3-8615	—	525	28 DIP	Colors changed by the "game select" inputs.	7-51
	BATTLE	A two player "tank battle" game where each player has a steerable tank and a fire control button.	AY-3-8710	Tank Battle	625	28 DIP	The on-screen "battlefield" includes anti-shell barricades and exploding mines.	7-52
			AY-3-8700-1		525			7-52
	MOTORCYCLE	A one player game where the player controls the speed of a motorcycle on a three track course.	AY-3-8760	Stunt Cycle Drag Race Motocross Enduro	525 or 625	28 DIP	Selectable NTSC/CCIR compatibility. Pro-Am game difficulty selection. Full color display.	7-56

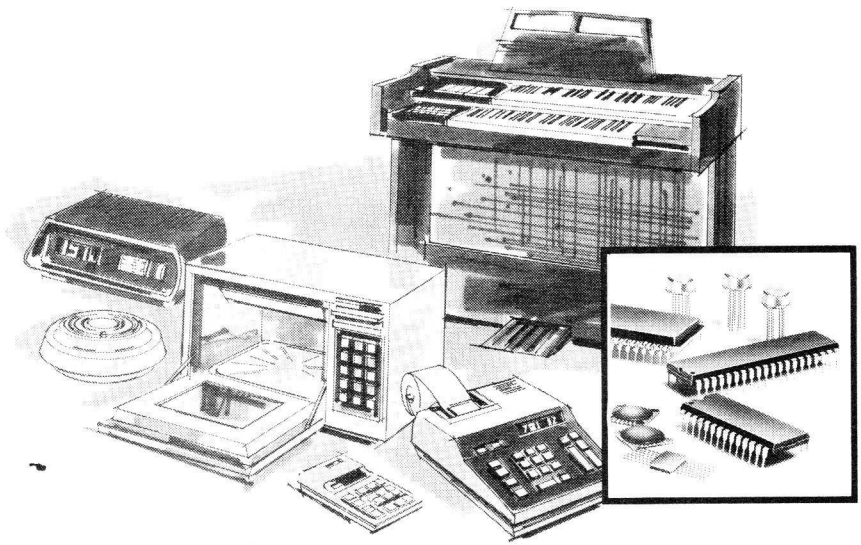
TV GAMES - 7 Programmable TV Games

FUNCTION	DESCRIPTION	PART NUMBER	GAME FUNCTION	PACKAGE	FEATURES	PAGE NO.
GIMINI ECONOMY "8600" PROGRAMMABLE GAME SYSTEM	With a single AY-3-8615 "resident processor" chip in the game console, the GIMINI Economy "8600" minimizes system cost. Each game cartridge provides full color games with realistic sounds and scoring.	AY-3-8615	RESIDENT PROCESSOR	28 DIP	Console-mounted game/color processor.	7-64
		AY-3-8603	ROADRACE CARTRIDGE	28 DIP	Two racing games—one or two players.	7-68
		AY-3-8603-1				
		AY-3-8605	WARFARE CARTRIDGE	28 DIP	Six battle games—one or two players.	7-69
		AY-3-8605-1				
		AY-3-8606	WIPEOUT CARTRIDGE	28 DIP	Ten games encompassing combat, strategy, and skill.	7-70
		AY-3-8606-1				
		AY-3-8607	SHOOTING CARTRIDGE	28 DIP	Twelve target games—one or two players.	7-71
		AY-3-8607-1				
		AY-3-8610	SUPERSPORT CARTRIDGE	28 DIP	Ten ball and paddle and target games.	7-72
		AY-3-8610-1				
		AY-3-8765	MOTORCYCLE CARTRIDGE	28 DIP	Four motorcycle racing/jumping games.	7-73
GIMINI CHALLENGER "8950" PROGRAMMABLE GAME SYSTEM	BASIC COMPONENTS: A complete microprocessor programmable game with only 3 LSI chips (plus standard RAM), the GIMINI Challenger "8950" is ideal for sports games and games of chance and mental skill.	CP1610	MICROPROCESSOR	40 DIP	A full 16-bit microprocessor for processing all game data.	7-86
		AY-3-8950	TV INTERFACE/ GRAPHICS ROM	40 DIP	Generates video and sound. On-chip 64 character graphics ROM.	7-78
		AY-3-8950-1				
		RO-3-9501	PROGRAM ROM	40 DIP	A 2048 x 10 ROM which contains the executive plus resident games.	7-92
		2112A	SYSTEM RAM	16 DIP	Customer-supplied 256 x 4 RAMs(minimum of two required).	7-99
	OPTIONAL COMPONENTS: The basic "8950" system can be expanded to include additional ROM and RAM, and to add complex sound generation.	RO-3-9500	CARTRIDGE ROM	28 DIP	A 2048 x 10 ROM which contains additional game programs.	7-92
		2112A/2114	PROGRAM/ SYSTEM RAM	16/18 DIP	Customer-supplied 256 x 4 or 1K x 4 RAMs to increase system capabilities.	7-99
		AY-3-8910	SOUND GENERATOR	40 DIP	Provides programmed generation of complex sound effects.	7-100
GIMINI DELUXE "8900" PROGRAMMABLE GAME SYSTEM	BASIC COMPONENTS: A complete microprocessor programmable game with only 5 LSI chips, the GIMINI Deluxe "8900" offers the capability for maximum game flexibility with detailed graphics definition and manipulation.	CP1610	MICROPROCESSOR	40 DIP	A full 16-bit microprocessor for processing all game data.	7-107
		*AY-3-8900	TV INTERFACE	40 DIP	Processes graphics data and generates all video signals.	7-107
		*AY-3-8900-1				
		RO-3-9502	PROGRAM ROM	40 DIP	A 2048 x 10 ROM which contains the executive program.	7-108
		RO-3-9503	GRAPHICS ROM	40 DIP	A 2048 x 8 ROM which stores 256-8 x 8 graphics characters.	7-108
		*RA-3-9600	SYSTEM RAM	40 DIP	Contains a 352 x 16 memory plus a 20 word "current line" buffer.	7-108
	OPTIONAL COMPONENTS: The basic "8900" system can easily be expanded to include additional games plus software-controlled graphics interaction, complex sound generation, and supplementary peripherals.	RO-3-9500	CARTRIDGE ROM	28 DIP	A 2048 x 10 ROM which contains additional game programs.	7-109
		2112A/2114	PROGRAM/ GRAPHICS RAM	16/18 DIP	Customer-supplied 256 x 4 or 1K x 4 RAMs to increase system capabilities.	7-109
		AY-3-8910	SOUND GENERATOR	40 DIP	Provides programmed generation of complex sound effects.	7-109
		*AY-3-8915	COLOR PROCESSOR	16 DIP	Generates a single composite color signal from AY-3-8900-1 digital input.	7-109
		*AY-3-8920	TAPE CASSETTE INTERFACE	40 DIP	Interfaces system to standard audio cassette decks.	7-109
		IOB 1680	INPUT/OUTPUT BUFFER	40 DIP	General purpose buffer for keyboards, displays etc.	7-109

*For future release.

FUNCTIONAL INDEX

Consumer 8



CONSUMER - 8 Calculators

FUNCTION	DESCRIPTION	PART NUMBER 6½-9½V LED	PART NUMBER 7-9V LED	PACKAGE	FEATURES	PAGE NO.
8 DIGIT BASIC	Basic 4 functions and %.	C-683D	C-1683D	28 DIP		8-16
		C-685D	C-1685D		Plus one-key or multi-key memory.	8-16
8 DIGIT ALGEBRA	Basic 4 functions, %, x^2 $\sqrt{x}$, 1/x, +/−, memory.	C-687D	C-1687D			8-16
		C-689D	C-1689D		Plus brackets and inch-cm. conversion.	8-16

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
9 DIGIT SCIENTIFIC	Full 21 function calculator circuit for 15V fluorescent displays.	CF-599	28 DIP	Basic 4 functions, %, sin, cos, tan, arc sin, arc cos, arc tan, ln x, e^x, $\log_{10}$, 10^x, $\sqrt{x}$, 1/x, x^2, y^x, +/−, memory, pi, two levels of parentheses, trig functions in degrees or radians.	8-15
12 DIGIT PRINTING	Basic 4 functions and %, decimal select mode, memory-in-use indicator, rounding options, non-add (#)/date key, and other features.	C-717X	40 DIP	Plus Accumulator and Grand Total Memories. Interfaces with Seiko 310 printer.	8-18
		C-718		Plus Accumulator, item counter, and 4-key memory. Interfaces with Seiko 310 printer.	8-19
NEW		C-1720		Features of C-718 but interfaces with Seiko 320 printer.	8-20
DISPLAY INTERFACE	Adds display capability to above printing calculators.	C-719	28 DIP	For both LED and fluorescent displays.	8-21

CONSUMER - 8 Clocks

FUNCTION	DESCRIPTION	PART NUMBER	FLASHING SECONDS	ZERO BLANKING	50/60Hz OPERATION	PACKAGE	FEATURES	PAGE NO.
4 DIGIT	12/24 hour clocks with features for most clock/timing applications.	AY-5-1200A		✓	✓	24 DIP	For 7-segment fluor. display.	8-24
		AY-5-1202A	✓	✓	✓	24 DIP	For 7-segment fluor. display.	8-24
		AY-5-1203A	✓		✓	24 DIP	BCD outputs.	8-24
		AY-5-1204A	✓		✓	24 DIP	For 7-segment fluor. display	8-24
		AY-5-1224A		✓	✓	16 DIP	BCD or 7-seg. LED outputs.	8-27
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	✓	✓	✓	28 DIP	Includes snooze alarm and pre-settable timeswitch.	8-29
4 DIGIT AUTO CLOCK	12 hour clock, timing derived from 3.58MHz TV crystal.	CK3500		✓	Crystal Input	40 DIP	For 7-segment LED display.	8-41
		CK3500F					For 7-segment fluor. display.	8-41

CONSUMER - 8 Music

FUNCTION	DESCRIPTION	PART NUMBER	MAXIMUM FREQUENCY	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
TOP OCTAVE GENERATORS	Generates a complete octave of musical frequencies.	**AY-1-0212**	1.5MHz	−14, −27	16 DIP	12 outputs, 50% duty cycle.	**8-48**
		AY-1-0212A	2.5MHz				**8-48**
		AY-3-0214	4.5MHz	+10 to +16	16 DIP	12 outputs, 50% duty cycle.	**8-50**
		AY-3-0215				13 outputs, 50% duty cycle.	**8-50**
		AY-3-0216				13 outputs, 30% duty cycle.	**8-50**
LATCHING NETWORK	Establishes priority of 13 pedal latch inputs/outputs.	**AY-1-1313**	20kHz	−12, −27	40 DIP	Stackable for expanded latching/ priority function.	**8-54**
RHYTHM GENERATOR	Generates 6 rhythms, drives 8 instruments.	**AY-5-1315**	10kHz	−15	18 DIP	Resets for coupling chords to rhythm, 32 beat pattern, mask programmable.	**8-56**
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass.	**AY-5-1317A**	50kHz	−15	40 DIP	Mixed outputs, sustain, top key priority.	**8-58**
PIANO KEYBOARD	Electronically simulates piano keyboard operation.	**AY-1-1320**	—	−10, −27	40 DIP	12 keys per unit, "loudness" proportional to key press velocity.	**8-62**
FREQUENCY DIVIDERS	4 stage divider.	**AY-1-5051**	1MHz	−13, −27	10 TO	Arranged 2+1+1.	**8-66**
	5 stage divider.	**AY-1-6721/5**			10 TO	Arranged 3+2.	**8-66**
	6 stage divider.	**AY-1-6721/6**			12 TO	Arranged 3+2+1.	**8-66**
	7 stage dividers.	**AY-1-5050**			14 DIP	Arranged 3+2+1+1.	**8-66**
		AY-1-1007B	50kHz	−12, −27	14 DIP	Arranged 3+2+1+1, power-on reset.	**8-52**

CONSUMER - 8 Appliances

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
CLOCK / TIMERS	24 hour programmable, repeatable on/off time switch with 4 digit clock.	**AY-5-1230**	−12 to −18	28 DIP	50Hz input (50 or 60Hz on AY-5-1231), BCD or 7-segment direct fluorescent display drive outputs, zero blanking, 24 hour display (12 or 24 hour on AY-5-1231).	**8-70**
		AY-5-1231		40 DIP		**8-70**
		AY-5-1232		28 DIP		**8-70**
		AY-5-1233		28 DIP		**8-70**
OVEN / COOKER TIMERS	Appliance timers with clock. Full control of "start" time, "stop" time, or "duration."	***AY-3-1250**	+12	28 DIP	Three timed outputs, "minute minder" feature, 12/24 hour system, 4 digit display (AY-5-1250) or 14 digit display (AY-5-1251).	**8-74**
		***AY-3-1251**		40 DIP		**8-74**
MICROWAVE OVEN TIMER	Three mode magnetron control, timer and 4 digit clock.	**AY-5-1260**	−5, −16	40 DIP	99 minute/99 second oven control and minute timer, status indicators, audio output.	**8-80**
DIGITAL THERMOMETER	Deep-freeze thermometer, −40°C to 0°C.	***AY-3-1270**	+9	40 DIP	For LCD/LED display, ±1°C accuracy, power fail/over-range indication (flashing display).	**8-82**
COINBOX MEMORY	Memory/credit accumulator for coin-operated equipment.	**AY-1-8622**	−12, −27	40 DIP	Seven different coin inputs, credit and "bonus" features.	**8-85**
VIDEO TAPE TIMER	Program "start" time for 2/4 hour video tape recorders.	**VTR 3300**	+7.5 to +15	28 DIP	12 or 24 hour time, direct drive for 7-segment LED's.	**8-90**

*For future release.

CONSUMER - 8 Security

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
SMOKE DETECTORS	Complete ionization smoke detector circuitry.	**MEM 4962**	+9	14 DIP	On-chip input MOSFET and output driver, low battery warning.	**8-98**
	Circuitry for ionization, photoelectric, or both.	**MEM 4963**	+9	14 DIP	As above, plus an interconnection capability for common alarm in multiple-unit installations.	**8-100**

The MEM 4962 is recognized under the Component Program of Underwriters Laboratories, Inc.

FUNCTIONAL INDEX

Industrial/Mosfet 9

INDUSTRIAL/MOSFET - 9 Counters / DVMs

FUNCTION	DESCRIPTION	PART NUMBER	MAX. COUNT FREQUENCY	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NO.
3½ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-5-3507	40kHz	−15	18 DIP	Range to 1999, 7-segment outputs.	9-8
		AY-5-3510			16 DIP	Range to 1999, BCD outputs.	9-8
3¾ DIGIT DVM	DVM logic utilizing single ramp integration.	AY-5-3500	200kHz	−7.5, −15	28 DIP	Ranges: 999, 1999, 2999. Dual polarity, BCD & 7-segment outputs.	9-4
4¾ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-3-3550	400kHz	+5	40 DIP	Auto-range, auto-zero, auto-polarity, BCD & 7-segment outputs.	9-13
4 DIGIT COUNTER	Counts, stores, and decodes 4 decades to BCD outputs.	AY-5-4057	500kHz	+5, −12	16 DIP	BCD outputs.	9-24
4 DIGIT COUNTER/ DISPLAY	Counts, stores, and decodes 4 decades to 7-segment outputs.	AY-5-4007	600kHz	+5, −12	24 DIP	BCD outputs, true/complement control.	9-18
		AY-5-4007A			40 DIP	Includes all features of AY-5-4007 and AY-5-4007D.	9-18
		AY-5-4007D			24 DIP	Serial output with shift clock input, 3 carry outputs.	9-18

INDUSTRIAL/MOSFET - 9 Mosfet Transistors

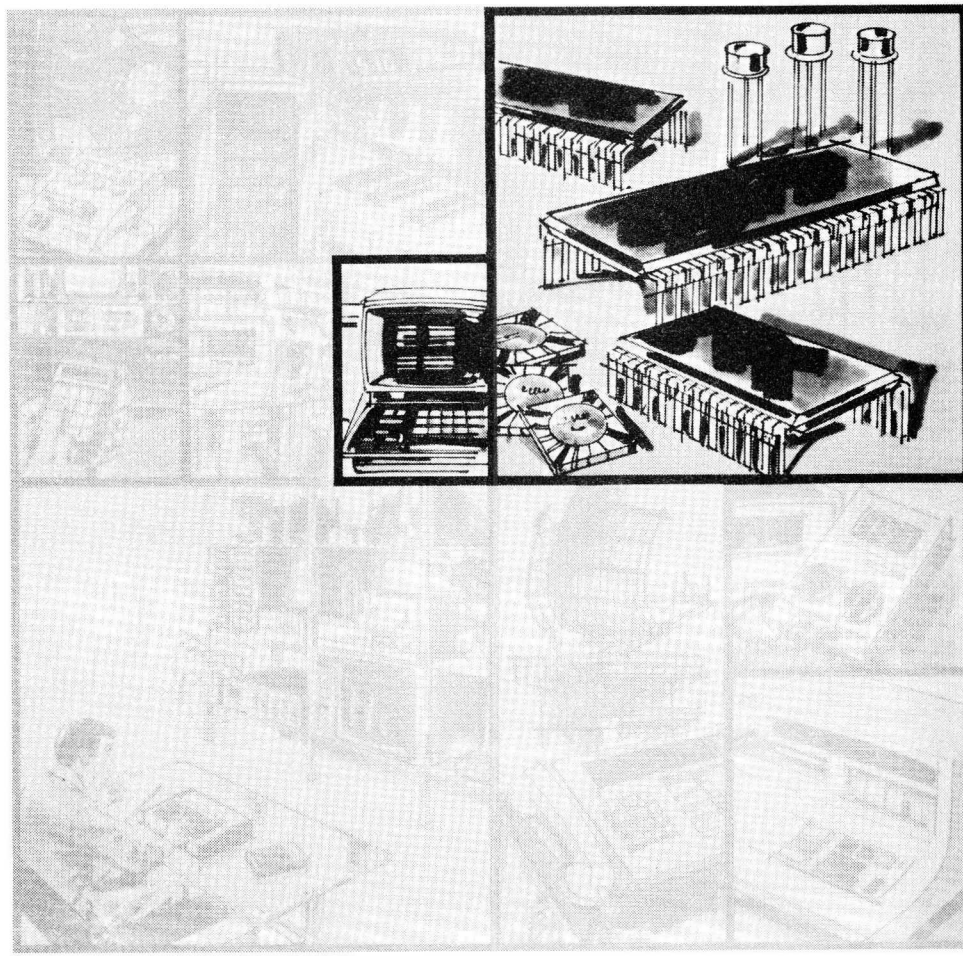
TYPE	PART NUMBER	$BV_{DSS/GSS}$ VOLTS-MIN.	I_{GSSF} nA-TYP.	$V_{GS\ (th)}$ V-MIN/MAX.	$r_{DS(on)}$ OHMS-TYP.	PAGE NO.	PART NUMBER	$BV_{DSS/GSS}$ VOLTS-MIN.	I_{GSSF} nA-TYP.	$V_{GS\ (th)}$ V-MIN/MAX.	$r_{DS(on)}$ OHMS-TYP.	PAGE NO.
P-CHANNEL ENHANCEMENT MODE	MEM511	−30/−30	−0.05	−3/−6	150	9-34	MEM560C	−30/−30	−0.2	−1/−3.5	175	9-62
	MEM511A	−30/−30	−0.5	−3/−6	300	9-36	MEM561	−30/−50	−0.05pA	−1.5/−3	100	9-64
	MEM511C	−25/−25	−0.05	−3/−6	150	9-38	MEM561C	−25/−40	−0.5,.A	−1.5/−3	150	9-64
	MEM517	−30/−25	−0.15	−2.5/−5	35	9-40	MEM806	−40/−40	−0.1pA	−2/−5.5	150	9-112
	MEM517A	−30/−25	−0.15	−2.5/−5	35	9-42	MEM806A	−40/−40	−0.05pA	−2/−5.5	150	9-112
	MEM517C	−25/−25	−0.15	−2.5/−5	35	9-44	MEM807	−40/−40	−0.1	−2/−5.5	150	9-114
	MEM520	−30/−40	−0.03pA	−3/−6	150	9-46	MEM807A	−40/−40	−0.2	−2/−5.5	150	9-114
	MEM520C	−25/−25	−0.1pA	−3/−6	150	9-48	MEM814	−35/−35	−0.1	−1.5/−3	80	9-116
	MEM556	−50/−50	−0.1	−3/−6	700	9-50	MEM816	−30/−30	−0.2	−2/−5	150	9-118
	MEM556C	−45/−45	−0.3	−3/−6	700	9-56	MEM817	−45/±200	−0.05pA	−2.5/−5.5	150	9-119
	MEM560	−35/−35	−0.1	−1.5/−3	100	9-62	MEM823	−35/±200	−0.05pA	−2.5/−5.5	150	9-120
TYPE	**PART NUMBER**	**BV_{DSS} VOLTS-MIN.**	**I_{GSSF} nA-TYP.**	**$V_{GS\ (th)}$ V-MIN/MAX.**	**$r_{DS(on)}$ OHMS-TYP**	**PAGE NO.**	**PART NUMBER**	**BV_{DSS} VOLTS-MIN.**	**I_{GSSF} nA-TYP.**	**$V_{GS\ (th)}$ V-MIN/MAX.**	**$r_{DS(on)}$ OHMS-TYP.**	**PAGE NO.**
DUAL P-CHANNEL ENHANCEMENT MODE	MEM550	−30	−0.1	−3/−6	250	9-50	MEM954A	−30	−0.03	−2/−5	100	9-121
	MEM550C	−25	−0.2	−3/−6	250	9-50	MEM954B	−30	−0.03	−2/−5	100	9-121
	MEM551	−30	−0.03pA	−3/−6	250	9-50	MEM955	−35	−0.02pA	−2/−5	100	9-121
	MEM551C	−25	−1.0pA	−3/−6	250	9-50	MEM955A	−35	−0.02pA	−2/−5	100	9-121
	MEM954	−30	−0.03	−2/−5	100	9-121	MEM955B	−35	−0.02pA	−2/−5	100	9-121
TYPE	**PART NUMBER**	**$BV_{DSS/GSS}$ VOLTS-MIN.**	**I_{GSSF} nA-TYP.**	**$V_{GS\ (th)}$ V-MIN/MAX.**	**$r_{DS(on)}$ OHMS-TYP**	**PAGE NO.**	**PART NUMBER**	**$BV_{DSS/GSS}$ VOLTS-MIN.**	**I_{GSSF} nA-TYP.**	**$V_{GS\ (th)}$ V-MIN/MAX.**	**$r_{DS(on)}$ OHMS-TYP.**	**PAGE NO.**
N-CHANNEL ENHANCEMENT MODE	MEM562	20/±30	1.0pA	0.5/4	150	9-66	MEM711	25/±30	0.1	0.5/1.5	50	9-106
	MEM562C	20/±30	10pA	0.5/4	150	9-66	MEM712	25/±30	.01	0.5/2	50	9-108
	MEM563	20/±30	1.0pA	0.5/4	40	9-68	MEM712A	30/±30	.01	0.5/2	30	9-108
	MEM563C	20/±30	10pA	0.5/4	50	9-68	MEM713	20/±30	10pA	0.5/2	50	9-110
TYPE	**PART NUMBER**	**$BV_{DSS/GSS}$ VOLTS-MIN.**	**I_{GSS} mA-TYP.**	**I_{GSS} nA-TYP.**	**$V_{GSS(off)}$ VOLTS-MAX.**	**PAGE NO.**	**PART NUMBER**	**$BV_{DSS/GSS}$ VOLTS-MIN.**	**I_{DSS} mA-TYP.**	**I_{GSS} nA-TYP.**	**$V_{GSS(off)}$ VOLTS-MAX.**	**PAGE NO.**
N-CHANNEL DEPLETION MODE	MEM554	20/+5, −10	5	0.01	−1.5	9-52	MEM632	25/±6	6	20	−4/−2	9-84
	MEM554C	20/+5, −10	5	0.05	−1.5	9-54	MEM636	20/±6	15	50	−4	9-88
	MEM557	20/±10	5	0.01	−4	9-58	MEM637	20/±6	15	20	−4	9-88
	MEM557C	20/±10	5	0.05	−4	9-60	MEM638	20/±6	15	20	−4	9-88
	MEM564C	20/±6	5	1.0	−1.5	9-70	MEM639	20/±6	10	—	−6	9-92
	MEM571C	20/±6	4	±10	—	9-72	MEM655	20/±6	4	±10	−4	9-94
	MEM610	20/±6	10	—	−6	9-74	MEM660	20/+30, −20	3	—	−4	9-96
	MEM614	20/±6	5	1.0	−1	9-76	MEM667	20/±100	3	0.05pA	−4	9-98
	MEM616	25/±6	10	20	−4	9-78	MEM670	20/±100	3	0.05pA	−4	9-99
	MEM617	20/±6	6	20	−4	9-78	MEM680	25/±6	4/30	50	−4	9-100
	MEM618	20/±6	10	20	−4	9-78	MEM681	25/±6	2/20	50	−4	9-100
	MEM619	20/±6	15	20	−4	9-82	MEM682	25/±6	3/20	50	−4	9-100
	MEM630	25/±6	6	20	−4/−2	9-84	MEM683	20/±6	15	20	−4	9-104
	MEM631	25/±6	10	20	−4/−3	9-84						

INDUSTRIAL/MOSFET - 9 Mosfet Analog Switches

FUNCTION	DESCRIPTION	PART NUMBER	P-P INPUT RANGE	ON RESISTANCE	TEMPERATURE RANGE	SUFFIX/PACKAGE	PAGE NO.
ANALOG SWITCHES	4 Channel Switch	MEM780	20V	30Ω	−65 to +85 (Plastic DIP) −65 to +125 (Ceramic DIP, Flat Pack)	P-14 Plastic DIP	9-124
		MEM781				D-14 Ceramic DIP	9-124
		MEM851	30V	100Ω		F-14 Flat Pack	9-126
	6 Channel Switch	MEM855	25V	350Ω			9-132
		MEM856	40V	1000Ω		P-24 Plas. DIP, D-24 Cer. DIP, F-24 Flat Pack.	9-134
	8 Channel Switch	MEM857	25V	150Ω			9-136
	10 Channel Switch	MEM853	25V	150Ω		P-14 Plas. DIP, D-14 Cer. DIP, F-14 Flat Pack.	9-128
DRIVER	4 Channel Driver	MEM4900	—	—			9-140

MICROPROCESSOR 2

Series 1600 2- 3
Series 8000 2-51



MICRO ELECTRONICS

SERIES 1600 MICROPROCESSOR

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
LSI CIRCUITS			
16 BIT SINGLE CHIP MICRO-PROCESSOR	The CP1600 utilizes third generation minicomputer architecture with 8 general purpose registers. The 16-bit word enables fast and efficient processing of alpha-numeric or byte oriented data. The 16-bit address capability permits access to 65,536 words of memory or peripheral devices.	CP1600	2-4
		CP1600A	2-4
		CP1610	2-4
DIGITAL TO ANALOG CONVERTER	Contains 4 registers which can be loaded or read through a 10-bit I/O port.	DAC 1600	2-12
INPUT OUTPUT BUFFER	A programmable buffer in which data is transferred to/from a peripheral on 16 bidirectional lines.	I/OB 1680	2-16
18 CHANNEL ANALOG MULTIPLEXER	A binary addressed mux which includes an on-chip address latch.	MUX 1600	2-22
READ ONLY MEMORIES	A series of 20K ROMs, organized 2048 x 10, which feature a single 16-bit bus for both address and data.	RO-3-9500	2-24
		RO-3-9501	2-24
		RO-3-9502	2-24
HARDWARE			
GIMINI SINGLE CARD MICRO-COMPUTER	Provides full 16-bit processing power on a single card; a complete operating system.	SC1600	2-31
GIMINI MICRO-COMPUTER SYSTEMS	A modular design for maximum configurability; all control/timing signals and buses are fully buffered.	GIMINI	2-32
		GIMINI II	2-32
GIMINI PC MODULES	Analog to Digital Module	AD1600	2-34
	Control Console Module	CC1600	2-35
	Digital to Analog Module	DA1600	2-36
	General Purpose Module	GP1600	2-37
	Reader-Punch Interface	I/O 1600	2-38
	Floppy Disc Interface	I/O 1610	2-39
	Microcomputer Module	MC1600	2-40
	Microcomputer Module	MC1610	2-41
	PROM Memory Module	PM1600	2-42
	PROM Programmer Module	PP1610	2-43
	RAM Memory Modules	RM1601/02	2-44
	RAM Memory Module	RM1610	2-46

16-Bit Single-Chip Microprocessors

FEATURES

- 8 program accessible 16-bit general purpose registers
- 87 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1600: 600ns cycle time, 3.3 MHz 2-phase clock
- CP1600A: 500ns cycle time, 4MHz 2-phase clock
- CP1610: 1μs cycle time, 2MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

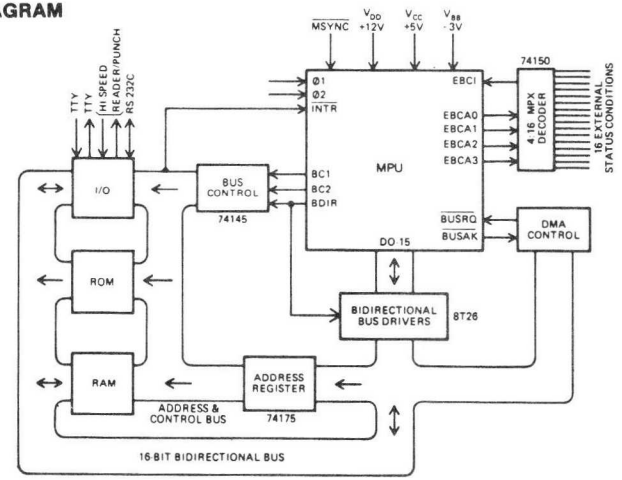
DESCRIPTION

The CP1600/CP1600A/CP1610 are compatible members of the Series 1600 Microprocessor products family. Each is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories, and Random Access Read/Write Memories are fully compatible with the CP1600/CP1600A/CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1600/CP1600A/CP1610 utilize third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1600 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROLS

$\overline{\text{STPST}}$
Input
STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

$\overline{\text{MSYNC}}$
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL SIGNALS

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

$\overline{\text{BUSRQ}}$
Input

$\overline{\text{BUSAK}}$
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

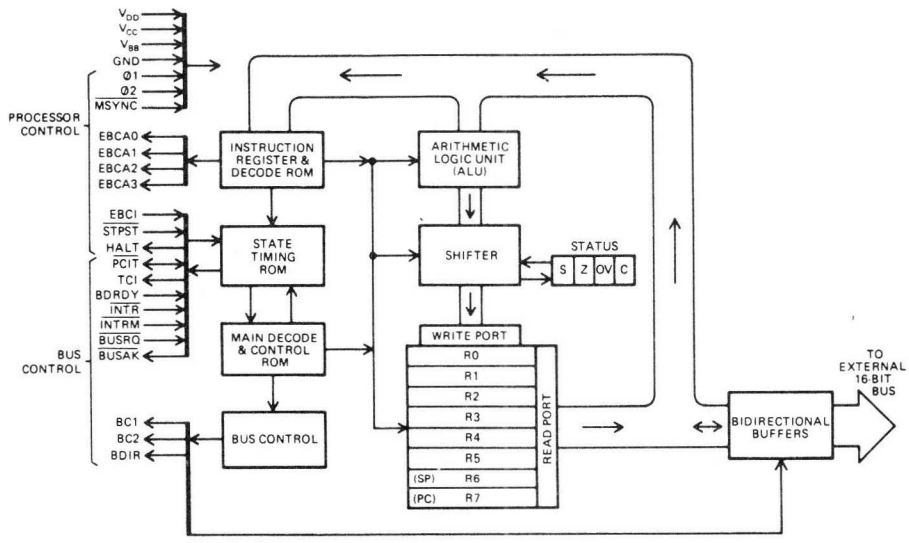
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

$\overline{\text{INTR}}$, $\overline{\text{INTRM}}$
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

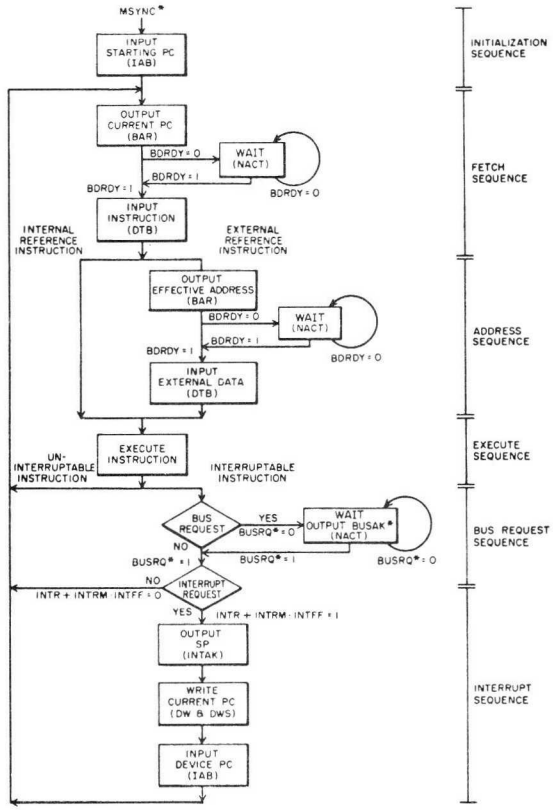
TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

$\overline{\text{PCIT}}$
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1600 INTERNAL BLOCK DIAGRAM



SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

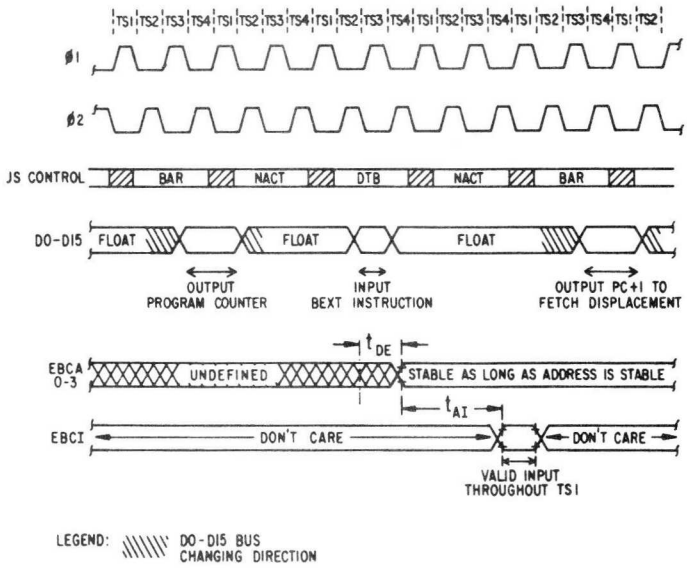
BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET SUMMARY

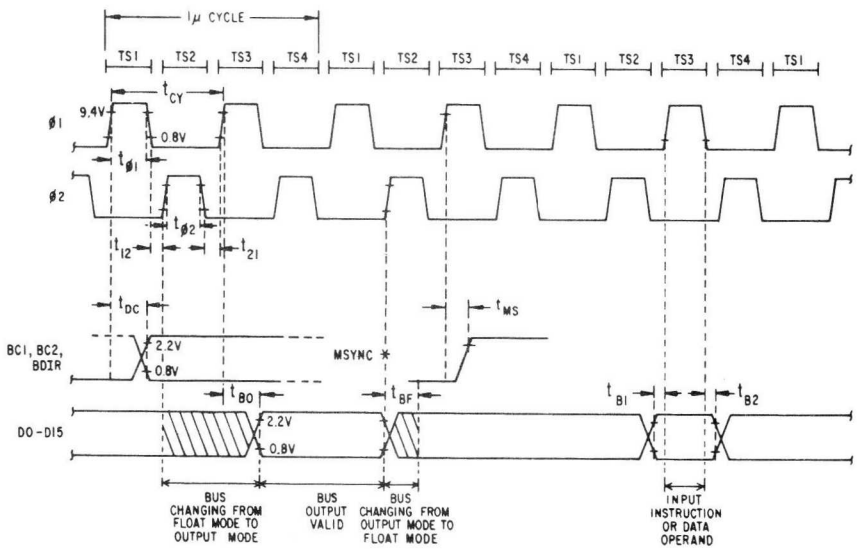
		Mnemonics	Operation	Microcycles Dir.	Indr.	Imm.	Stack	Comments
External Reference Instructions	Arithmetic & Logic	ADD	ADD	10	8	8	11	Result not saved
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	
	I/O	MVO	MoVe In	10	8	8	11	
		MVI	MoVe In	10	8	8	11	
Internal Register Instructions	Register to Register	ADDR	ADD contents of Registers	6				Add one cycle if Register 6 or 7, except*. Result not saved
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr.	6				
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		MOVR	MOVe Register	6				
	Single Register	CLRR	CLeaR Register	6				XORR with itself
		TSTR	TeST Register	6				
		JR	Jump to address in Register	7*				PC←(RRR)
		INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				Two Words
		SIN	Software INterrupt	6				Pulse to PCIT pin
		RSWD	Return Status WorD	6				
		PULR	PULl from stack to Register	11*				PULR=MVI @ R6
		PSHR	PuSH Register to stack	9*				PSHR=MVO @ R6
	Register Shift	SLL	Shift Logical Left	6				one or two position shift capability. Add two cycles for 2-position shift
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
		SWAP	SWAP 8-bit bytes	6				2-position=SWAP twice
Control Instructions		HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				Not Interruptible
		TCI	Terminate Current Interrupt	4				
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
Jump Instructions		J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable Interrupt	12				
Conditional Branch Instructions		B	unconditional Branch	7				Displacement in PC+1 PC←PC±Displacement Add 2 cycles if test condition is true.
		BC, BLGE	Branch on Carry, C=1	7				
		BNC, BLLT	Branch on No Carry, C=0	7				
		BOV	Branch on OVerflow, OV=1	7				
		BNOV	Branch on No OVerflow, OV=0	7				
		BPL	Branch on PLus, S=0	7				
		BMI	Branch on Minus, S=1	7				
		BZE, BEQ	Branch on ZEro or EQual	7				Z=1
		BNZE, BNEQ	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S¥OV=1
		BGE	Branch if Greater than or Equal	7				S¥OV=0
		BLE	Branch if Less than or Equal	7				ZV(S¥OV)=1
		BGT	Branch if Greater Than	7				ZV(S¥OV)=0
		BUSC	Branch if Sign ≠ Carry	7				C¥S=1
		BESC	Branch if Sign = Carry	7				C¥S=0
		BEXT	Branch if External condition is True	7				4 LSB of Instruction are decoded to select 1 of 16 external conditions.

1 MICROCYCLE = 2 CLOCK CYCLES

BUS TIMING DIAGRAM



TYPICAL INSTRUCTION SEQUENCE



BRANCH ON EXTERNAL CONDITION INSTRUCTION

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions: (unless otherwise noted)

V_{DD}=+12V±5%, 70mA(typ), 110mA(max.) V_{BB}= −3V±10%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.4	–	V_{DD}	V	
Low	V_{ILC}	0	–	0.6	V	
Logic Inputs						
Low	V_{IL}	0	–	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	–	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	–	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	–	–	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	–	–	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	–	–	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	120		–	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	–	–	ns	
Clock Period	t_{cy}	0.3	–	2.0	μs	
Rise & Fall Times	tr, tf	–	–	15	ns	
Master SYNC:						
Delay from φ	tms	–	–	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	–	–	120	ns	1 TTL Load & 25 pF
Output delay from φ2 (output to float)	t_{BF}	–	50	–	ns	
Input setup time before φ1	t_{B1}	0	–	–	ns	
Input hold time after φ1	t_{B2}	10	–	–	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	–	–	120	ns	
BUSAK Output delay from φ1	t_{BU}	–	150	–	ns	
TCI Output delay from φ1	t_{TO}	–	200	–	ns	
TCI Pulse Width	t_{TW}	–	300	–	ns	
EBCA output delay from BEXT input	t_{DE}	–	–	150	ns	
EBCA wait time for EBCI input	t_{AI}	–	–	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; t φ1 t φ2 = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
Input Capacitance						
D0-D15	CIN	—	6	12	pF	
All Other	—	—	5	10	pF	
Output Capacitance						
D0-D15 in high impedance state	C_D	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions: (unless otherwise noted)

V_{DD}=+12V±5%, 70mA(typ), 140mA(max.) V_{BB}= −3V±10%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.4	—	V_{DD}	V	
Low	V_{ILC}	0	—	0.6	V	
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	—	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	—	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}		V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	—	—	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	—	—	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	95		—	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	—	—	ns	
Clock Period	t_{Cy}	0.25	—	2.0	μs	
Rise & Fall Times	tr, tf	—	—	15	ns	
Master SYNC:						
Delay from φ	tms	—	—	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	—	—	95	ns	1 TTL Load & 25 pF
Output delay from φ2 (output to float)	t_{BF}	—	50	—	ns	
Input setup time before φ1	t_{B1}	0	—	—	ns	
Input hold time after φ1	t_{B2}	10	—	—	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	—	—	200	ns	
BUSAK Output delay from φ1	t_{BU}	—	150	—	ns	
TCI Output delay from φ1	t_{TO}	—	200	—	ns	
TCI Pulse Width	t_{TW}	—	300	—	ns	
EBCA output delay from BEXT input	t_{DE}	—	—	150	ns	
EBCA wait time for EBCI input	t_{AI}	—	—	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; $t_{\phi 1}$ $t_{\phi 2}$ = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
Input Capacitance						
D0-D15	CIN	—	6	12	pF	
All Other	—	—	5	10	pF	
Output Capacitance						
D0-D15 in high impedance state	C_D	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions: (unless otherwise noted)

V_{DD}=+11V±5%, 70mA(typ) , 110mA(max.) V_{BB}= −3V±10%, 0.2mA(typ) , 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ) , 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.0	–	V_{DD}	V	
Low	V_{ILC}	0	–	0.6	V	
Input current	—	—	—	15	mA	$V_{IHC} = V_{DD} - 1$
Logic Inputs						
Low	V_{IL}	0	–	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	–	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	–	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	–	–	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	–	–	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	–	–	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	250		–	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	–	–	ns	
Clock Period	t_{cy}	0.5	–	2.0	μs	
Rise & Fall Times	tr, tf	–	–	15	ns	
Master SYNC:						
Delay from φ	tms	–	–	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	–	–	200	ns	1 TTL Load & 25 pF
Output delay from φ2 (output to float)	t_{BF}	–	50	–	ns	
Input setup time before φ1	t_{B1}	0	–	–	ns	
Input hold time after φ1	t_{B2}	10	–	–	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	–	–	200	ns	
BUSAK Output delay from φ1	t_{BU}	–	150	–	ns	
TCI Output delay from φ1	t_{TO}	–	200	–	ns	
TCI Pulse Width	t_{TW}	–	300	–	ns	
EBCA output delay from BEXT input	t_{DE}	–	–	150	ns	
EBCA wait time for EBCI input	t_{AI}	–	–	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; t φ1 t φ2 = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
Input Capacitance						
D0-D15	CIN	—	6	12	pF	
All Other	—	—	5	10	pF	
Output Capacitance						
D0-D15 in high impedance state	C_D	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

Dual Digital to Analog Converter

DESCRIPTION

The DAC1600 Digital to Analog Converter has been designed to serve as a powerful, yet economic interface to a process control loop. The DAC1600 provides two 10-bit Pulse Width Modulated outputs and an array of switch inputs and light driver outputs. Essentially the DAC1600 contains four registers which can be loaded or read through a 10-bit I/O data port. Fig. 1 shows the data base information in these registers.

ANALOG OUTPUTS

The value of the analog outputs SP and VO are determined respectively by the ten-bit numbers loaded in the Set Point Register and the Valve Register. An output is a pulse train with a period of approximately 1kHz (1MHz/1024) whose high/low ratio is inversely related to the 10-bit value stored in the register. (See Fig. 2).

The high/low ratio is unaffected by temperature and supply variations and is the basis of the 10-bit D/A accuracy. The length of the high or low portions of the pulse will never be in error by more than a fraction of an LSB.

If the chip output (SP or VO) is passed through a low pass filter the result will be approximately equal to the desired analog voltage. However, it will not be accurate because, while the output ratio is accurate, the chip's output voltage levels are not, and would thereby degrade the accuracy of the signal. The chip's output should be used to drive a good switch which, in conjunction with a voltage reference and filtering will yield an analog voltage having 10-bit accuracy.

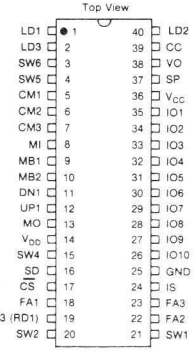
VALVE REGISTER (Manual Mode)

In addition to being a register, the Valve Register (B) is also an UP/DOWN counter. By setting MI (Manual Interrupt) to a "1" and either UP or DN to a "1", the B register will be slewed up or down. This allows an operator to manually adjust the B register value. The design allows bumpless, balanceless transfers between computer and manual control. In order to provide both a precise degree of manual control and an ability to slew the B register through a substantial change, a variable slewing rate has been incorporated in the chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



MODE REGISTER

The first five bits of Mode Register (A) may be used to store the mode of control. Manual Interrupt is in bit 1. Bits M2, M3, M4 and M5 can be read or loaded via the I/O bus or set by inputs from three switch inputs CM1, CM2, or CM3. The condition of these bits is encoded and output on light drivers MB1 and MB2. The Mode Register may be used to inform the operator of computer determined conditions or inform the computer of operator actions.

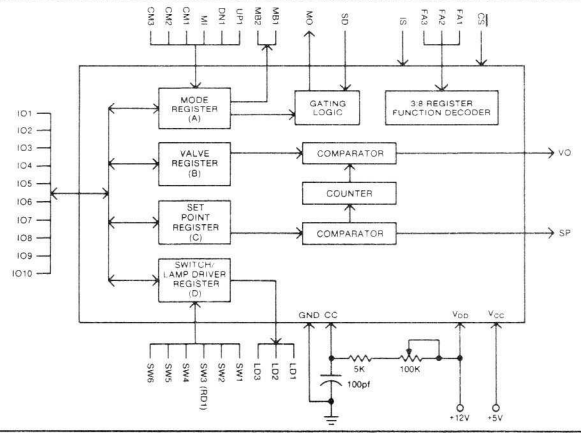
SWITCH/LAMP DRIVER REGISTER

The Switch/Lamp Driver Register contains three light drivers which can be used for panel alarm lights. It also stores six switch inputs.

ADDITIONAL ALARM FEATURE

Light driver M0 outputs a 2 cps signal which can flash a light to attract an operator's attention.

BLOCK DIAGRAM



PIN FUNCTIONS

I01-10: 10 bit bidirectional data bus. Data can be loaded synchronously or asynchronously. Data are read onto the I/O bus without strobing.

MI: Manual input line. It forces the chip into a manual mode of operation.

$\overline{CS}$: Chip select line. It is low active for synchronous data transfer, high active for asynchronous data transfer.

IS: Input strobe line. It loads one of the four internal registers defined by FA1-3, when $\overline{CS}$ is low. If the chip is in the manual mode via MI, the ability to load one of the four registers, namely, the valve register, is unconditionally inhibited independent of the $\overline{CS}$ signal.

FA1-3: Function select lines. It is used to specify one of the four registers and whether an input or output function is to be performed. See Table 2 for definition.

CM1-3: Control mode lines. A pulse on one of these lines will alter the bit M3, M4 or M5 in the mode register. See Table 3.

UP1, DN1, RD1: Up counting, down counting and reversing lines. They are used to control the direction of counting serially in the valve register during the manual mode. Overflow or underflow of the register is prevented by internal circuitry. See Table 4 for definition.

SD: DAC1600 shed signal. It is used in conjunction with manual input line to form different manual mode outputs. See Table 5.

MO: DAC1600 manual mode output. It oscillates around 2Hz whenever MI is low and SD is high. See Table 5.

MB1, MB2: Mode bit-lines. They are used to indicate the status of the mode register. See Table 6.

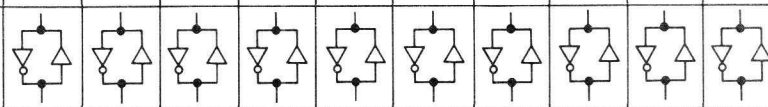
VO: Valve register output. It is a 10 bit pulse width modulated waveform. See Fig. 2

SP: Set point register output. It is a 10 bit pulse width modulated waveform. See Fig. 2.

CC: DAC1600 counter clock input.

SW1-SW6: They are used by CPU as switch word. SW3 (RD1) is also used in reversing the direction of counting in valve register during manual mode.

LD1-LD3: Panel lamp driver outputs.

	IO-10	IO-9	IO-8	IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1
I/O Buffer										
Register A (mode register)	1	1	1	UP+	DN+	M5	M4	M3	M2	M1+
Register B (valve register)	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1
Register C (set point register)	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1
Register D (switch/lamp driver register)	0	SW6+	SW5+	SW4+	SW3+	SW2+	SW1+	LD3	LD2	LD1

+Read only locations

Fig. 1 REGISTERS DATA BASE

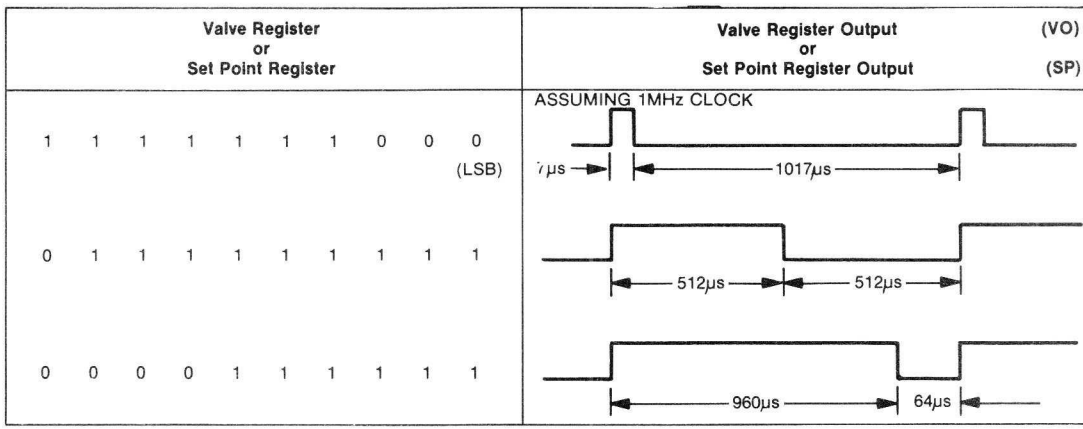


Fig. 2 PULSE WIDTH MODULATED OUTPUT WAVEFORMS

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

T_A = 0°C to 75°C
V_{DD} = +12V ± 5%
V_{CC} = +5V ± 5%

Symbol	Characteristic	Min.	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5	+0.65	V	*
V_{IH}	Input High Voltage	2.2	V_{CC}	V	*
I_{IN}	Input Current	—	± 10	µA	V_{IN} = 0V to 5.25V
I_{LOH}	Output Lkg. Curr.	—	10	µA	$\overline{CS}$ = 2.2V IO (1-10) = 4.0V
I_{LOL}	Output Lkg. Curr.	—	-10	µA	$\overline{CS}$ = 2.2V; V_{CC} = 5.25 V; IO (1-10) = 0.4V
C_{IN}	Input Capac	—	8	pF	f = 1MHz
C_{OUT}	Output Capac	—	10	pF	f = 1MHz @ V_{OUT} = 0.0V Tri-State Mode
V_{OL}	Output Low Voltage	—	0.45	V	*I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.7	V_{CC}	V	*I_{OH} = 300µA, C_L = 100pF
I_{CC}	Supply Current	—	5	mA	
I_{DD}	Supply Current	—	25	mA	No Load

* Applies to TTL compatible inputs and outputs. See Table 1 for other inputs and outputs.

Table 1: THE FOLLOWING TABLE DEFINES INTERNAL PULL UP CURRENT SOURCES

Signal	In / Out	Pull Up	Comp	Loading
FA1,2,3	In	To +5V	TTL	⩽ 1ma @ .4V
LD1	Out	—	—	Load Type A
LD2	Out	—	—	Load Type A
MI	In	None	Comp Type 1	
M0	Out	—	—	Load Type A
CM1	In	None	Comp Type 1	
CM2	In	None	Comp Type 1	
CM3	In	None	Comp Type 1	
MB1	Out	—	—	Load Type A
MB2	Out	—	—	Load Type A
SW3 (RD1)	In	To +5V	TTL	⩽1ma @ .4V
SW2	In	To +5V	TTL	⩽1ma @ .4V
SW1	In	To +5V	TTL	⩽1ma @ .4V
V0	Out	—	—	Load Type B
SP	Out	—	—	Load Type A
UP1	In	None	Comp Type 1	
SW5	In	None	Comp Type 1	
DN1	In	None	Comp Type 1	
SW6	In	None	Comp Type 1	
SW4	In	None	Comp Type 1	
LD3	Out	—	—	Load Type A
SD	In	To +5V	TTL	⩽1ma @ .4V
CC	In	Series RC to Common		
IS	In	To +5V	TTL	⩽1ma @ .4V
$\overline{CS}$	In	To +5V	TTL	⩽1ma @ .4V
I01, -10	In/Out	Tri State	—	Load Type C

COMPATIBILITY

Comp. Type 1 — High ..... 4V to 12V
Low 0.4V

LOADING

Load Type A — Source ..... 2.5 mA @ 4V Min
Sink ..... 300 µA @ 0.4V Max

Load Type B — Source ..... 10 µA @ 9V Min
Sink ..... 1mA @ 1.2V Max

Load Type C — Sink ..... 1.6 mA 0.45V Max
Source ..... 300 µA @ 2.7V Min
Cap ..... 100 pF Max Load

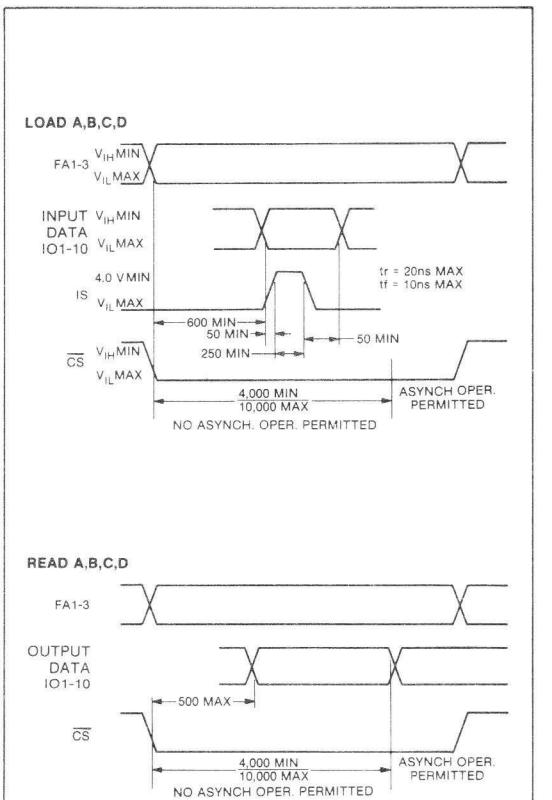


Fig. 3 TIMING DIAGRAM

Table 2 REGISTER AND FUNCTION SELECT

FA				
3	2	1	Operation	Condition
0	0	0	Load 'A'	
0	0	1	Load 'B'	MI+ = 0
0	1	0	Load 'C'	
0	1	1	Load 'D'	
1	0	0	Read 'A'	
1	0	1	Read 'B'	
1	1	0	Read 'C'	
1	1	1	Read 'D'	

Table 3 MODE CONTROL

CM						
3	2	1	M5	M4	M3	M2
		⊓	1	0	0	0
	⊓		0	1	0	0
⊓			0	0	1	0

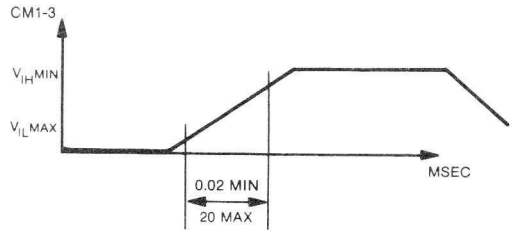


Table 4 MANUAL MODE FUNCTION CONTROL

MI	$\overline{CS}$	UP1	DN1	RDI	Operation
1	1	0	0	0	No Op
1	1	0	0	1	No Op.
1	1	0	1	0	Incr "B"
1	1	0	1	1	Decr "B"
1	1	1	0	0	Decr "B"
1	1	1	0	1	Incr "B"
1	1	1	1	0	Indeterminate
1	1	1	1	1	Indeterminate
1	0*	X	X	X	No Op.
0	0	X	X	X	As specified by FA1-3
0	1	X	X	X	No Op.

INCR/DECR speed is controlled by an internal variable frequency clock. The clocking rates are as follows:

16Hz for 2 seconds
64Hz for 2 seconds
128Hz thereafter until UP1 or DN1 are deactivated

*If $\overline{CS}$ remains low for longer than 10 μsec. normal operation (per UP/DN) will resume.

Table 5 MANUAL MODE OUTPUT

MI	SD	MO
0	0	0
0	1	⊓⊓⊓ f = 2Hz
1	0	1
1	1	1

Table 6 MODE REGISTER STATUS

				MB	
M5	M4	M3	M2	2	1
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

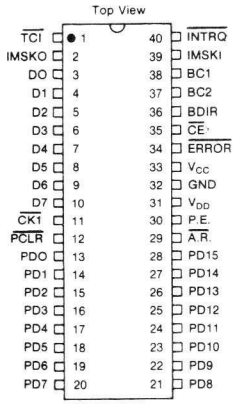
Input/Output Buffer

FEATURES

- Single 16-Bit Port or Dual 8-Bit Ports for Bidirectional Input/Output
- Parity Check Logic on Both Ports
- Three Levels of Priority Interrupt Logic
- 'Real Time' Presetable 16-Bit Timer
- Capability to Monitor Peripheral Error Status
- Three Interrupt Vectors for Error, I/O and Timer
- Automatic Handshake Logic and Signals
- Control Register
- TTL Compatible

PIN CONFIGURATION

40 LEAD DUAL IN LINE

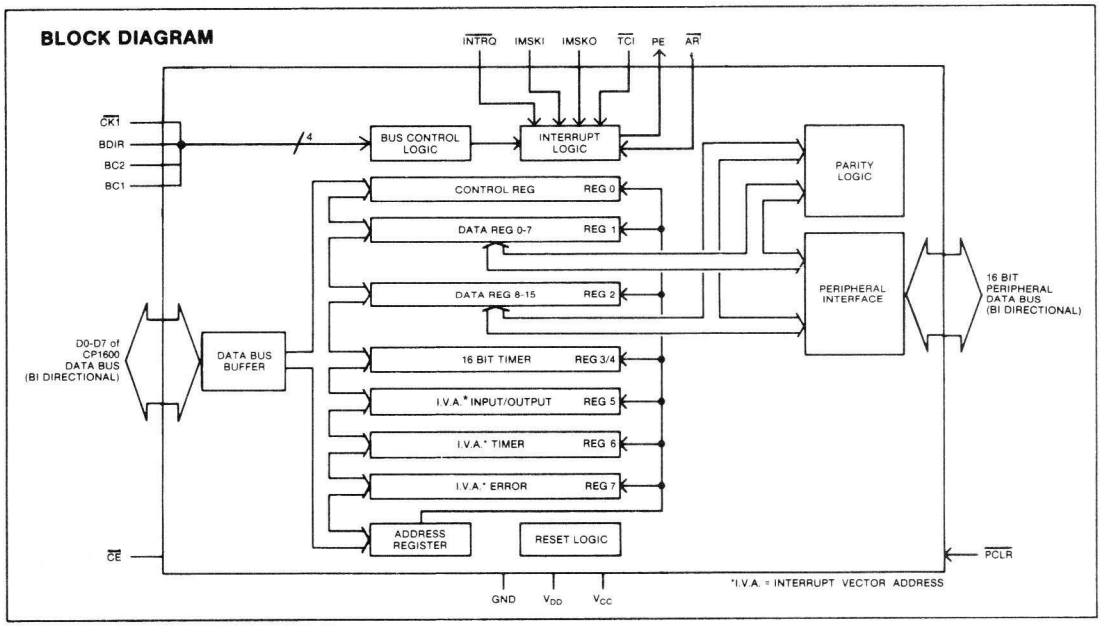


DESCRIPTION

The IOB1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing facilities for the CP1600 microprocessor with a minimum of additional components. The circuit is fabricated in General Instrument N-Channel Ion Implant GIANT II process insuring high performance with proven reliability and production history.

The IOB1680 enables efficient interfacing between a peripheral and the CP1600 by the use of six 8-bit registers and a 16-bit programmable timer. Two of the 8-bit registers are a buffer store between the CP1600 and the bidirectional I/O lines to peripheral, latching any data sent to them from the CP1600. Three other 8-bit registers hold the Interrupt Vector Addresses associated with I/O, Error Status and the Timer. The Control Register governs the operation and characteristics of the IOB1680 and provides a convenient means for the CP1600 to monitor I/O status information. The 16-bit timer gives the IOB1680 a real time capability which is suitable for confirming system security and for timing peripheral activities. These registers are initialized after power clear by the CP1600 program writing the required interrupt vector addresses into the appropriate registers. The interrupt vectors may also be altered at any time by program.

BLOCK DIAGRAM



IOB1680/CP1600 SIGNALS

Data Bus:

D0-D7 (Input/Output/High Impedance)
DATA 0-7: The bidirectional data lines D0-D7 are used to transmit data and address information between the Series 1600 Microprocessors and the IOB1680. These correspond to the lower 8-bits of the Series 1600 Microprocessor's data bus. These data lines have tristate capability, being in the high impedance state except when transferring data or status information from the IOB1680 under control of the control bus signals BDIR, BC1 and BC2.

Bus Control Signals

BDIR, BC1, BC2 (Inputs)
Bus DIRection, Bus Control 1 and 2: Bus control signals from the CP1600 which define the state of data bus operations. These signals are decoded internally by the IOB1680 to control its operation.

$\overline{\text{TCI}}$ (Input)
Terminate Current Interrupt: A pulse output by the CP1600 in response to the TCI instruction to indicate the end of the current interrupt service routine.

$\overline{\text{INTRQ}}$* (Output)
INTerrupt ReQuest: This output is pulled low to a logic '0' by the IOB1680 to request an interrupt from the series 1600 Microprocessor. This is an open drain output capable of sinking 1.6mA with an output voltage 0.5V. Because of the open drain feature the $\overline{\text{INTRQ}}$ output of several IOB1680s can be wired ORed together.

$\overline{\text{CK1}}$ (Input)
ClocK 1: This clock defines when the bus control signals BDIR, BC1 and BC2 are valid and is used in the IOB1680 to strobe their decode signals. It is also used to increment the timer.

$\overline{\text{CE}}$ (Input)
Chip Enable: This low true address input enables the IOB1680 for data read and write operations.

IMSKI/MSK0 (Input/Output)
Interrupt MaSK In, Interrupt MaSK Out: These two signals are used to form the interrupt priority daisy chain and prevent a lower priority device from requesting an interrupt while a higher device is being serviced. The IMSKI input of the IOB1680 which is to have highest priority must be connected to GND.

IOB1680 PERIPHERAL SIGNALS

Data

PD0-PD15 (Input/Output)
Peripheral Data 0-15: Communication of data to and from the peripheral device is via this 16 bit highway. Each output can sink 1.6mA for an output voltage of 0.5V. In the high state each output can source 100μA. These lines can be used as wire ORed inputs by 'pulling down' the line to a logic '0' sinking the 100μA externally.

Peripheral Control Signals:

PE (Output)
Peripheral Enable: This output is a function of the Ready bit of the control register. When it is at a logic '0' no action is required by the peripheral, a '1' indicates that peripheral activity has been requested by the CP1600.

$\overline{\text{AR}}$ (Input)
Attention Request: This input from the peripheral device is normally high at a logic '1' and is taken low to a logic '0' by the peripheral to request attention. This edge triggers the Ready bit of the control register forcing it to a logic "1", causing an interrupt request to be made via the $\overline{\text{INTRQ}}$ output if the peripheral interrupt enable bit of the control register is set. If the interrupt is disabled the Ready bit of the control register can be used in 'polling' handshake routines.

$\overline{\text{ERROR}}$ (Input)
ERROR: The error status of the peripheral is indicated by this input; being low indicating an error condition, e.g. tape low.

$\overline{\text{PCLR}}$ (Input)
Power CLeaR: Initializes registers.

INTERNAL CONTROL SIGNALS

Control Register:

The Control Register can be written and read under program control. The function of the individual bits are:

Bit 7—Parity Status for Peripheral Data 0-7:
The parity of the low order byte of the Peripheral Data bus is indicated by this Control bit, a logic '1' indicates even parity while a '0' indicates odd.

Bit 6—Parity Status for Peripheral Data 8-15:
Similar to bit 7, but indicates the parity of the high order byte of Peripheral Data.

Bit 5—Timer Clock Enable (TCE):
The clock to the 16-bit timer is controlled via TCE, the clock is enabled by setting TCE to a logic '1'. The timer can only request an interrupt when its clock is enabled by TCE.

Bit 4—Timer Interrupt Enable (TIE):
For the timer to cause an interrupt request on the $\overline{\text{INTRQ}}$ output TIE must be set to a logic '1', a '0' disables the timer interrupt logic.

Bit 3—Peripheral Interrupt Enable (PIE):
PIE must be set to a logic '1' to enable interrupt requests on the $\overline{\text{INTRQ}}$ output as a result of peripheral Attention Request or Error Status conditions.

Bit 2—Data Width Select (DWSL):
The re-enabling of the peripheral by automatic handshake can be chosen to occur with 8 or 16-bits wide data; DWSL being an '0' indicates an 8-bit wide data word while a '1' indicates a sixteen bit wide data word.

Bit 1—Error Summary
The ERROR STATUS of the peripheral is indicated by this bit of the Control Register, being a logic '0' shows an error condition. This will cause an interrupt request on the $\overline{\text{INTRQ}}$ output if PIE is set to a '1'.

Bit 0—Ready
This READY bit indicates the operational status of the peripheral. When it is a logic '0' the peripheral is active while a logic '1' indicates that the peripheral is idle and requiring service. The $\overline{\text{AR}}$ input going low indicates to the Ready bit the end of a peripheral activity and thereby causes the Ready bit to be set. In this condition, if the PIE bit is set, an interrupt request results via the $\overline{\text{INTRQ}}$ output. Reading or writing to the Peripheral Data lines causes the resetting of this Ready bit re-enabling the peripheral activity.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{CC} and all other input/output voltages with respect to GND ..... -0.3V to +18V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

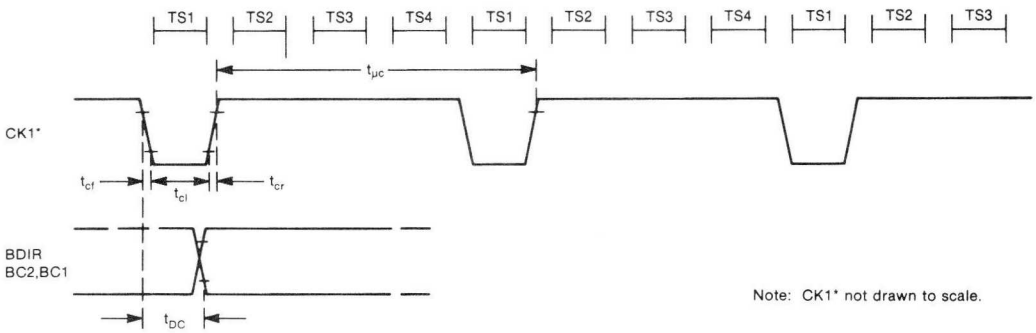
Standard Conditions (unless otherwise noted)

All voltages referenced to GND
V_{DD} = +12V ±5%
V_{CC} = +5V ±5%
Operating Temperature (T_A) = 0°C to +70°C

Characteristic		Symbol	Min	Typ**	Max	Unit	Condition
DC CHARACTERISTICS							
Clock Input:	High	V_{ihc}	2.4	—	V_{DD}	V	
	Low	V_{ilc}	0	—	.5	V	
Logic Inputs:	High	V_{ih}	2.4	—	V_{CC}	V	
	Low	V_{il}	0	—	.65	V	
Logic Outputs:	High	V_{oh}	2.4	V_{CC}	—	V	I_{oh} = 100μA
	Low	V_{ol}	—	—	.5	V	I_{ol} = 1.6mA
AC CHARACTERISTICS							
Clock Inputs							
$\overline{CK1}$	Clock period	tμc	0.4	—	4.0	μs	
	Clock width	tcl	70	—	—	ns	
	Rise & Fall times	tcr,tcf	—	—	10	ns	
CAPACITANCE (T_A = 25°C, V_{DD} = +12V, V_{CC} = +5V)							
Input Capacitance:	D0-D7	C_{in}	—	6	12	pF	V_{in} = 0V
	All others		—	5	10	pF	V_{in} = 0V
Output Capacitance:		C_{out}	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



Note: CK1* not drawn to scale.

CIRCUIT DESCRIPTION

This circuit is designed to provide all the data buffering and control functions required when interfacing the Series 1600 Microprocessor System to a simple peripheral device. Data is transferred to and from the peripheral on 16 bidirectional lines, each of which can be considered to be an input or output. The transfer of information with the CP1600 is accomplished via an 8-bit highway, the 16-bits being transferred as two 8-bit bytes. The register addresses are assigned CP1600 memory locations, as follows (N is an arbitrary starting address):

Register Address	Description
N	Control Register
N + 1	Data Register Low Order 8-bits
N + 2	Data Register High Order 8-bits
N + 3	Timer Low Order 8-bits
N + 4	Timer High Order 8-bits
N + 5	Peripheral Interrupt Address Vector
N + 6	Timer Interrupt Address Vector
N + 7	Error Interrupt Address Vector

8-Bit Data Registers

These two 8-bit registers are the buffer store between the CP1600 and the peripheral interface. These registers, when addressed, accept data from the CP1600 data bus during a Move Out (MVO) instruction to the peripheral lines on the IOB1680.

During a CP1600 Move In (MVI) instruction, the data present on the IOB1680 peripheral lines is transferred to the CP1600 data bus. If the registers have not been set to a '1' prior to the Move In instruction, the data read will be the wire OR of the peripheral data and that contained in the registers.

These two registers have consecutive word addresses N + 1 and N + 2. The high order byte is held in register N + 2.

16-Bit Binary Counter-Timer

This 16-bit down counter can be set under program control to give any count length up to 64K. Since only 8-bits are available to transfer data between the CP1600 and the IOB1680 the counter must be set as two 8-bit bytes, these bytes having word addresses N + 3 and N + 4. The clock for the timer is the Series 1600 Microprocessor System clock divided by 8. The clock input to the counter is enabled when the 'timer clock enable' bit of the control register is set to a '1', being disabled when this bit is reset to a '0'.

Everytime the count reaches zero the timer signals 'end of count' which will generate an interrupt request via the $\overline{\text{INTRQ}}$ output of the IOB1680 if both the 'timer interrupt enable' and 'timer clock enable' bits of the control register are both set to a '1'. The clock to the timer is still enabled after this interrupt request has been made and remains so even after it has been serviced, assuming that the service routine did not disable it by resetting the TCE bit of the control register. After requesting an interrupt therefore the counter begins from a count of 64K, giving the IOB1680 a Real Time Clock capability.

The timer has the lowest priority on the IOB1680 daisy chain. The peripheral error summary has the highest priority.

When the timer is set under program control the 'end of count' logic is reset clearing any previously unserviced interrupt requests from the timer. The acknowledge flip flop and the control register are unaffected.

It is not possible to read the 'current' state of the timer as it is counting in 'real time' and therefore asynchronously with any program running on the CP1600. A typical operating sequence is:

1. Load two bytes of counter.
2. Set 'timer interrupt enable' and 'timer count enable' bits of Control Register.

If an interrupt is required only once after the preset count the service routing would reset the 'timer clock enable' bit of the Control register disabling the timer clock and interrupt capability. If, however, the interrupt was required on a regular 'real time' basis then the service routine would leave the 'timer interrupt enable' and 'timer clock enable' bits set.

8-Bit Interrupt Vector Address Registers

The start address of the interrupt service routines for the error status, peripheral and timer are held in these three registers. The 8-bit Interrupt Vector Addresses are written into these registers during system initialization. When an interrupt request ($\overline{\text{INTRQ}}$), generated from the IOB1680 is acknowledged by an INTAK from the CP1600, the subsequent IAB signal on the control bus causes the contents of the appropriate interrupt vector address register to be strobed onto the lower 8-bits of the CP1600 data bus. This data is used as the program counter start address of the interrupt service routine.

The word addresses of these registers are N + 5, N +6 and N + 7. This corresponds to the peripheral, timer and error respectively.

Power Clear Status of Circuit

Reset logic sets the initial state of the chip upon application of Power Clear. In this condition the states of the on chip registers are:

(a) **Data Registers.**
These are set to a logic '1' so that the peripheral input/output interface is high at a logic '1', this allows the peripheral lines to be used as inputs without any setting up procedure.

(b) **Timer.**
This is set to its maximum count length of 64K, all bits set to a logic '1'.

(c) **Interrupt Vector Address Registers.**
These registers have all their bits reset to a '0' by the power on reset logic.

Control Register.

(i) Bit 0 - Ready. This bit is set to a logic '1' indicating that no activity is required by the peripheral.

(ii) Bit 1 - Error Summary. This is a hard wired input indicating the status of the peripheral and is unaffected by the power on reset logic.

(iii) Bit 2 - Data Width Select. This bit is reset to a logic '0', selecting the data width of the interface to be 8-bits.

(iv) Bit 3 - Peripheral Interrupt Enable.
Bit 4 - Timer Interrupt Enable.
Both bits 3 and 4 are reset to a '0' at power on, disabling interrupts from the peripheral, and the timer.

(v) Bit 5 - Timer Clock Enable. During power up this bit is reset to a logic '0' disabling the counter clock.

(vi) Bit 6 - Parity Data 8-15.
Bit 7 - Parity Data 0-7.
Both these bits will be at a logic '1' showing even parity as the data register bits are all set to a '1'. This assumes no inputs from the peripheral; if this is not so, these bits will settle to a state depending upon the wire OR condition of the data registers and the peripheral inputs.

Interrupt Logic

The interrupt priority of the peripheral error status, peripheral interface and the timer is established by a daisy chain. The peripheral error status has the highest priority and the timer the lowest.

If a number of IOB1680s are being used then they can be connected in a daisy chain using the signals IMSKI, IMSKO and $\overline{\text{TCI}}$ to define their priority. An interrupt request is made by the IOB1680 pulling down, to a logic '0', the $\overline{\text{INTRQ}}$ output. This output is open drain enabling wire OR capability. The acknowledgement to this request is an INTAK signal via the Series 1600 Microprocessor control bus. Each IOB1680 decodes this signal which sets an acknowledge flip flop in the interface of the interrupting device, causing the IMSKO output of that device to go to a '1'. This propagates to all lower priority devices causing their IMSKI inputs to go to a '1', thus disabling their interrupt capability.

When an IAB is valid on the control bus only the highest priority interrupting device must strobe its Interrupt Vector Address onto the Data Bus. Thus the IMSKI input of a device controls its IAB decode. The IAB signal is only enabled on the IOB1680 which has its IMSKI input at a logic '0' and its acknowledge flip flop set.

If two devices interrupt simultaneously they will both be acknowledged by an INTAK since this is decoded on each chip. However, the IMSKO output of the higher priority device going to a '1' will force the IMSKI input of the lower priority interrupting device to a '1'. The IMSKI input of the lower priority device being set to a '1' disables the IAB decode of the control bus thereby resolving simultaneous interrupts.

The negative edge of the TCI signal from Series 1600 Microprocessor resets the interrupt logic of the highest priority device whose interrupt logic has been set by an interrupt request and acknowledged by an INTAK.

The IMSKI/IMSKO daisy chain has a propagation delay which allows a maximum of eight IOB1680s to be daisy chained in series.

The IMSKI input to the highest priority device should be connected to Gnd.

Control Logic

The CP1600 control bus signals BDIR, BC1, BC2 are decoded to perform the internal control functions required.

Parity Logic

The peripheral interface is constantly monitored and the parity of bits 0-7 and 8-15 checked. Depending on the parity of these two words, bits 6 and 7 of the control register are updated. These bits can be conveniently accessed by the CP1600 for use in branch instructions.

Branching on Parity

Bits 6 and 7 of the IOB1680 Control register contain the parity status of the upper and lower eight bits of the peripheral interface respectively. The positioning enables the standard branch instructions of the CP1600 to be conveniently utilized. A typical example is:

```
MVI CTRLRS, R;Fetch Control Register
RLC R2, 2
BNC     ;Branch if lower eight bits have odd parity
BC      ;Branch if lower eight bits have even parity
BNOV    ;Branch if higher eight bits have odd parity
BOV     ;Branch if higher eight bits have even parity
```

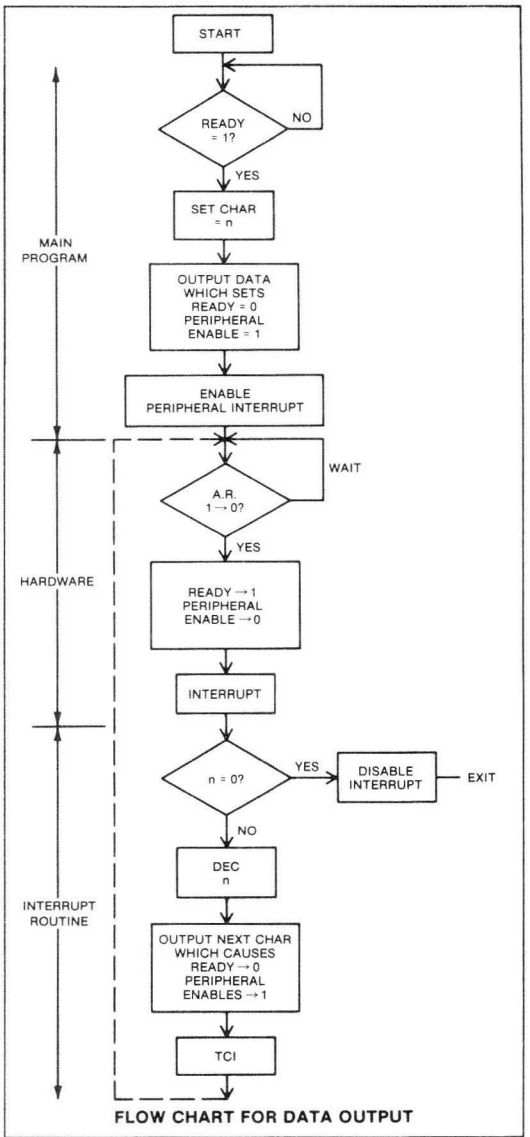
The IOB1680 as an Output Device

The power clear reset logic of the IOB1680 sets the Ready bit of the Control Register to a '1', causing the Peripheral Enable/Ready output to go to a '0', a condition that requires no activity from the peripheral. This power clear reset logic also disables the IOB1680's ability to request an interrupt on the status of the peripheral by resetting the Peripheral Interrupt Enable bit of the Control Register to a '0'.

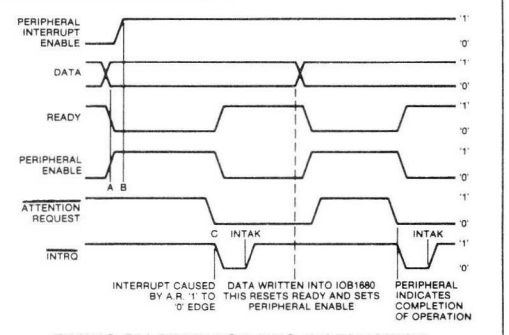
A flow chart for a typical output operation is shown to the right; the waveform diagram corresponding to this operation is also shown to the right.

The main program setting up the output operation would go through the following sequence of operations.

1. The Ready bit of the Control Register would be tested to ensure that the peripheral was indeed inactive. This would be so initially after power clear.
2. If condition (1) above is met, memory location CHAR of the CP1600 would be set to the number of output operations required. This is shown as 'SET CHAR = n'.
3. Send data from CP1600 to IOB1680 using MVO instruct. This operation resets the Ready bit to a '0' causing the Peripheral Enable/Ready output to go to a '1', requesting an operation by the peripheral device. This is shown at A in the waveform diagram.
4. The Peripheral Interrupt Enable (PIE) bit of the Control Register is now set to a '1' by programmer allowing the IOB1680 to request interrupts from the CP1600 via the INTRQ* output. Enabling the PIE bit after sending the data to the peripheral ensures that no 'false' interrupts are generated.
5. After the data has been sent to the peripheral (3) above, the IOB1680 hardware monitors the status of the Attention Request input. A '1' to '0' edge on the input sets the Ready bit to a '1' and the Peripheral Enable/Ready output to a '0', stopping the peripheral activity. The PIE bit and the Ready bit both being set to a '1' causes an interrupt request to be generated via the INTRQ output, if no higher priority devices are interrupting. Refer to C in the waveform diagram.
6. When the CP1600 accepts the interrupt it starts the interrupt sequence by issuing the INTAK acknowledge signal which resets the INTRQ output to its inactive state. The subsequent IAB signal causes the Interrupt Vector Address for the peripheral device to be strobed onto the data bus and then used as the start address for its service routine.
   Once entered, the service routine might go through the following sequence.
7. Decrement n, the number of output operations required (buffer length).
8. Test the resulting value n.
   (a) If it is zero the output operations are completed. Reset the PIE bit to disable the interrupt capability of the IOB1680 and EXIT.
   (b) If n is not zero output the next data to the IOB1680. This resets Ready to a '0' and Peripheral Interrupt Enable/Ready to a '1', re-enabling the peripheral activity automatically.
   The peripheral acknowledges this operation by returning the Attention Request input to a '1', the timing of this signal is not too critical as the it edge triggers the Ready bit of the control register by a 1-0 transition.
9. The interrupt is terminated by TCI instruction which resets the acknowledge flip flop in the IOB1680 interface logic.



FLOW CHART FOR DATA OUTPUT



TIMING DIAGRAM FOR MVO INSTRUCTION (Data from CP1600 to IOB1680)

The IOB1680 as an Input Device

The power clear status of the IOB1680 for input is the same as for output which is described under the section 'The IOB1680 as an Output Device'.

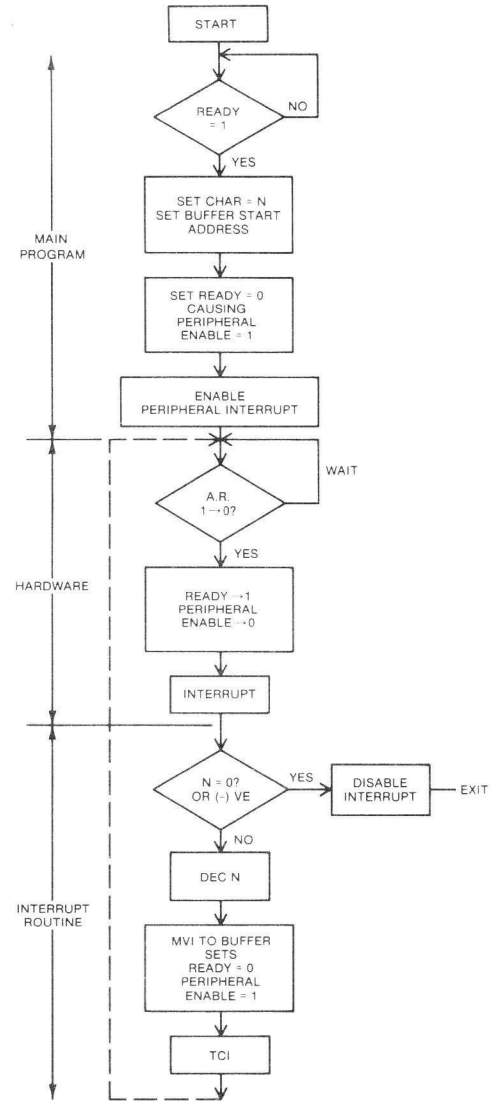
A flow chart for a typical input operation and the corresponding waveform diagram is shown to the right.

The main program setting up the input operation would probably go through the following sequence:

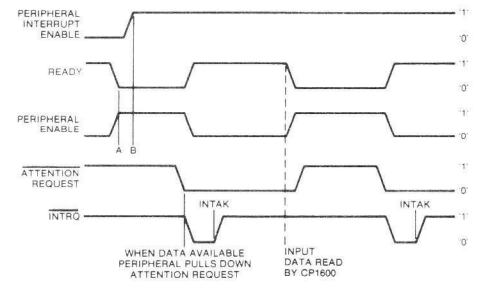
1. Test the Ready bit of the Control Register to ensure that the peripheral device is inactive. After power clear this will be its condition, i.e. set to '1'.
2. If condition (1) is true a CP1600 memory location will be set to contain the number of input operations required. Another memory location will be set to the input buffer start address. This is shown as 'SET CHAR = N, SET BUFFER START ADDRESS'.
3. The Ready bit of the Control Register should now be reset to a '0' by program. This causes the Peripheral Enable/$\overline{\text{Ready}}$ output to go to a '1', requesting an operation from the peripheral device. On the waveform diagram, this is point A.
4. The Peripheral Interrupt Enable bit, PIE, of the Control Register is now set to a '1' by program. This allows the IOB1680 to request interrupts from the CP1600 via the $\overline{\text{INTRQ}}$ output (see point B). Enabling the PIE bit after the Ready Bit ensures that initially no false interrupts are generated.
5. After the Ready bit has been reset by program, (3) above, hardware on the IOB1680 monitors the Attention Request input. A '1' to '0' edge on this input causes the Ready bit to be set to a '1' and the Peripheral Enable/$\overline{\text{Ready}}$ output to go to a '0'. The change in state of the output stops the peripheral operation. As both the PIE bit and Ready bit of the Control Register are set an interrupt request will be generated via the $\overline{\text{INTRQ}}$ output if no higher priority devices are interrupting.
6. When this interrupt is accepted by the CP1600 the acknowledge signal, INTAK, will reset the $\overline{\text{INTRQ}}$ output to its inactive state. The subsequent IAB signal will cause the Interrupt Vector Address associated with the peripheral to be strobed onto the data bus. This address will be used as the start address for the peripheral's interrupt service routine.

   A typical service routine for the peripheral could be:

7. Test value of N. the number of input operations required
   (a) if it is zero all the required input operations have been completed. Reset the PIE bit of the Control Register to a '0' to disable the interrupt capability of the IOB1680 and EXIT.
   (b) if not zero increment the buffer address and decrement N.
8. Move data from the IOB1680 and CP1600 by a MVI instruction. This resets the Ready bit to a '0' and sets the Peripheral Enable/$\overline{\text{Ready}}$ output to a '1', re-enabling the peripheral. The handshake from the peripheral in response to this action is to return the Attention Request input high to a '1'. This timing, however, is not too critical as the input edge triggers the Ready bit.
9. The interrupt is terminated by a TCI instruction which resets the acknowledge flip flop in the IOB1680 interface.



FLOW CHART FOR DATA INPUT



TIMING DIAGRAM FOR MVI INSTRUCTION (DATA FROM IOB1680 TO CP1600)

18 Channel Analog Multiplexer

FEATURES

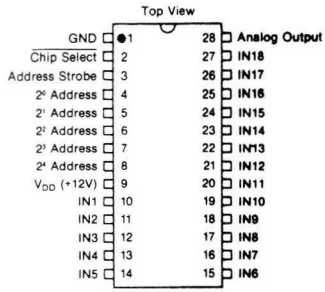
- Connects 1 of 18 analog inputs to analog output pin
- Address latch on-chip
- 0 to 6 volt input range
- Single +12V supply
- Analog output controlled by chip select signal

DESCRIPTION

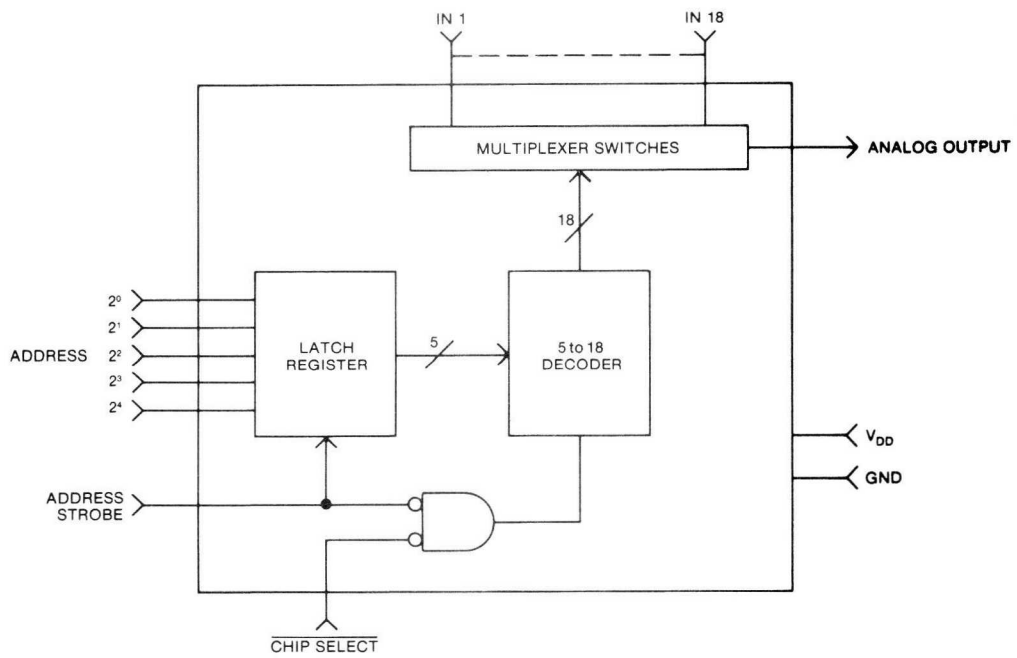
The MUX1600 is a binary addressed 18 channel analog multiplexer fabricated in General Instrument's advanced N-channel Ion Implant process. Featuring on-chip address latches and separate address strobe and chip select signals, the MUX1600 operates from a single +12 Volt supply.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and all other input/output voltages with respect to GND ..... -0.3V to +18V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... 0°C to +70°C

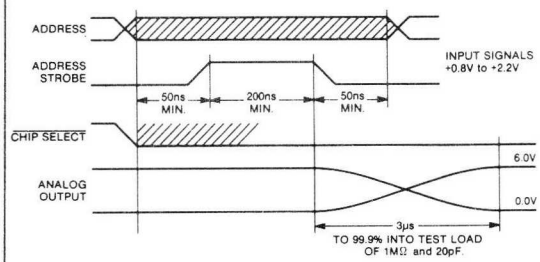
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

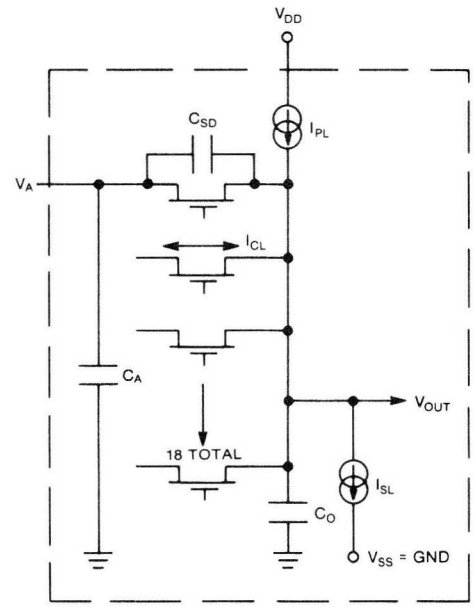
All voltages referenced to GND
V_{DD} = +12V ± 5%
Operating Temperature (T_A) = 0°C to +75°C

Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Input Load Current (all digital inputs)	I_{IN}	—	—	±10	µA	V_{IN} = 0V to 5.25V
Power Supply Current	I_{DD}	—	—	8	mA	All digital inputs = 5.25V
Input Low Voltage	V_{IL}	-0.5	—	0.80	V	
Input High Voltage	V_{IH}	2.2	—	V_{DD}	V	
Analog Input Voltage	V_A	0.0	—	6.0	V	
Channel on Resistance	R_{ON}	—	—	600	Ω	V_A = 0V to 6V
Channel leakage (each channel)	I_{CL}	—	—	5	nA	V_A - V_{OUT} = 6V
V_{DD} Leakage	I_{PL}	—	—	10	nA	V_{DD} - V_{OUT} = 17V
Source to Drain Capacitance	C_{SD}	—	—	5	pF	f = 1 MHz
Analog Input Cap.	C_A	—	—	5	pF	f = 1 MHz
Analog Output Cap.	C_O	—	—	20	pF	f = 1 MHz
Digital Input Cap.	C_D	—	—	5	pF	f = 1 MHz
Substrate Leakage	I_{SL}	—	—	410	nA	V_O - V_{SS} = 6V
18 I_{CL} + I_{PL} + I_{SL}	I_{LT}	—	—	500	nA	V_O - V_{SS} = 6V

SWITCHING CHARACTERISTICS



LEAKAGE CURRENT DIAGRAM



20480 Bit Static Read Only Memories

FEATURES

- 2048 × 10 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 1K of external RAM (RO-3-9501) or up to 65K of external RAM (RO-3-9502).
- Internal address status and data bits latched
- 300 ns typical data access time
- 1.8μs complete cycle time
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION: RO-3-9501

The RO-3-9501 is a unique 20,480 bit ROM employing a single 16 bit address and data tristate buss. The RO-3-9501 increases the power of single buss microprocessors or microcontrollers by providing separate latched address and control lines for static RAM chips. The RO-3-9501 internally decodes ROM and external RAM control codes. ROM addressing is via an 11-bit word address and a 5-bit chip select code. Ten bit data is outputted on the lower 10 bits of the I/O buss. In addition there are two programmable 16-bit interrupt response codes, one for the first interrupt after master clear and one for all other interrupts. These codes are output to the I/O bus in response to control codes, which do not require a chip select code. The RO-3-9501 contains a 10 bit latch and address output port; the 10-bit address appearing at this port may be used to control an external RAM. The address is latched by a control code on the three mode control lines, and the RAM enable signal which consists of all zeros on data bits 11 through 15. The stored address is copied from bits 0 through 9 on the data buss.

The RO-3-9501 has two programmable features, in addition to the 2048 word by 10-bit ROM. A five bit chip select code decodes data bits 11 through 15 in order to generate the internal chip enable signal. Second, the two 16-bit interrupt response codes are programmable.

DESCRIPTION: RO-3-9502

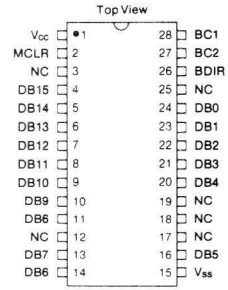
The RO-3-9502 has all the features of the RO-3-9501 described above except that it has a full 16-bit latch and address port for external RAM.

DESCRIPTION: RO-3-9500

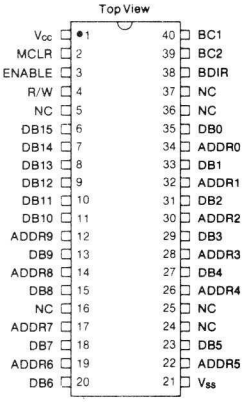
The RO-3-9500 does not provide address facilities for external RAM allowing for its packaging is a 28 lead DIP.

PIN CONFIGURATIONS

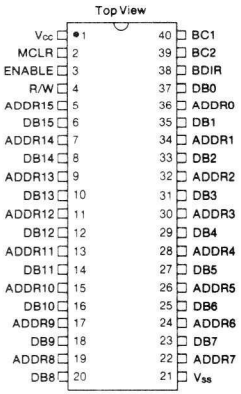
28 LEAD DUAL IN LINE
RO-3-9500



40 LEAD DUAL IN LINE
RO-3-9501



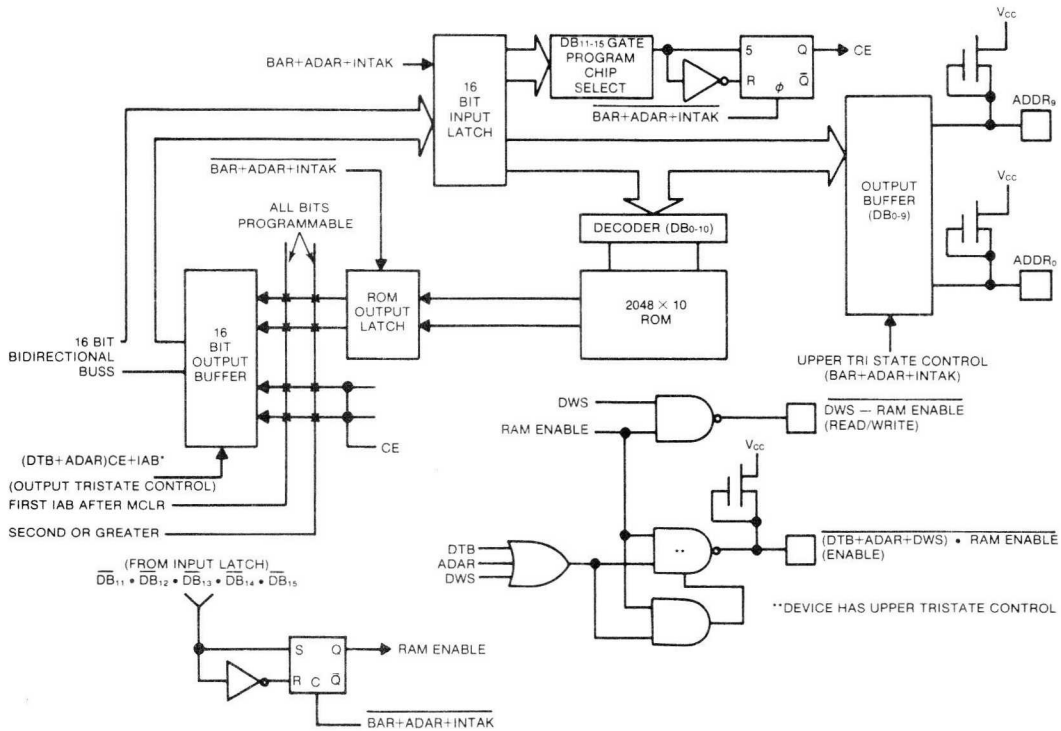
RO-3-9502



PIN FUNCTIONS

Enable (RO-3-9501/02)	An ouput pin to select external RAM (low = true)
R/W (RO-3-9501/02)	An output pin for read/write control of external RAM, a positive pulse controls the write cycle.
ADDR0-9 (RO-3-9501) ADDR0-15 (RO-3-9502)	Output address lines to external RAMs.
DB0-DB15	Bidirectional, tristate data and address buss, high output impedance for NACT control code.
BC1, BC2 BDIR	Buss control 1 and 2, and buss direction control signals determine chip mode control
V_{CC}	+5 volts
V_{SS}	Ground
MCLR	Master clear, sets all outputs to high impedance state when low.

BLOCK DIAGRAM: RO-3-9501



NOTES:

1. Input data and internal chip enable latched by control codes = BAR + ADAR + INTAK
2. Internal chip enable signal cleared by = BAR + ADAR + INTAR
3. Internal RAM enable signal flip flop set by PB11-15 all zeros, cleared by = BAR + ADAR + INTAK
4. RAM enable plus DWS creates low on Read/Write line.
5. RAM enable plus DTB, ADAR or DWS creates enable output signal.
6. DTB or ADAR plus internal chip enable puts output ROM data to tristate buss.
7. Maximum skew time between control code transitions is 40 nsec to avoid false states.
8. Enable R/W and ADDRO — 9 lines normally high impedance outputs. When circuits are enabled, active pull up transistors turned on to allow wired or connection to other chips. RAM control signals and output addresses revert to high impedance state in 2 and 0 - 3μsec respectively. After master clear, chip enable and RAM enable flip-flops turned off and all outputs in high impedance states.

OPERATING MODES

The RO-3-9501 is designed to enhance the system operation of 16-bit Microprocessors that use a single multiplexed buss for data and memory addresses, such as the GI CP1600, the Intel 8085 and the Fairchild 9440. The state diagram shows recommended sequences for initialization, program storage with RAM addressing, and interrupt handling.

The three mode control lines BC1, BC2 and BDIR create 8 functions. As shown in figure one, these functions are chosen to simplify program and data storage in the ROM. Functionally the RO-3-9501 performs the following functions in a microprocessor system:

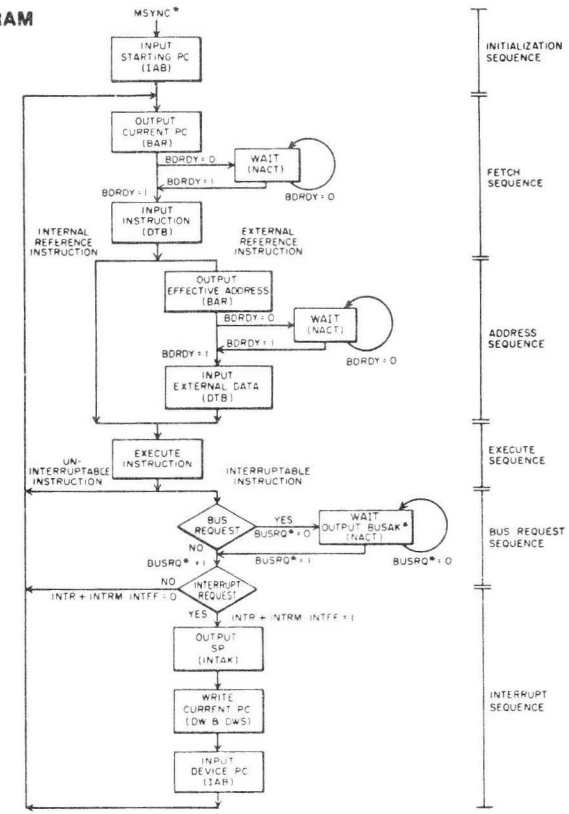
A. When the CPU generates a 5 chip select and seven bits of ROM address, the RO-3-9501 generates a 10-bit response from the 2048 × 10 bit ROM.

B. The ROM output data can be used to create a ten-bit immediate or indexed RAM address, which is then stored in the RO-3-9501 ten output latches and the RAM control lines. In addition the RAM enable and R/W control lines are generated by inernal logic.

C. In response to initial clear and the first interrupt, the RO-3-9501 can be programmed to place a 16-bit trap address on the I/O buss for restarting a chosen program sequence. The RO-3-9501 can additionally be programmed to generate a different 16-bit trap address in response to subsequent IAB's.

For the IAB (Interrupt Address to Buss) commands to work properly, an address must first be loaded into the chip to disable the internally latched chip enable code.

SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and all other input/output voltages with respect to GND .....−0.3V to +18V
Storage Temperature ..... −55°C to 150°C
Operating Temperature ..... 0°C to +70°C

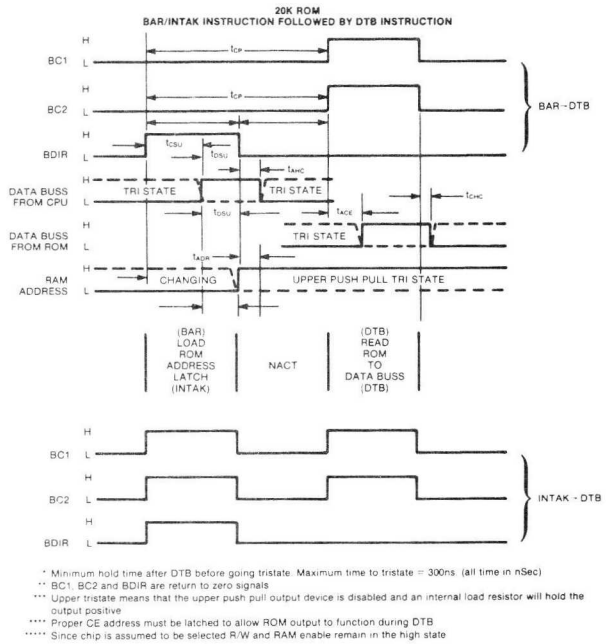
*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

All voltages referenced to GND
V_{DD} = +12V ±5%
Operating Temperature (T_A) = 0°C to +75°C

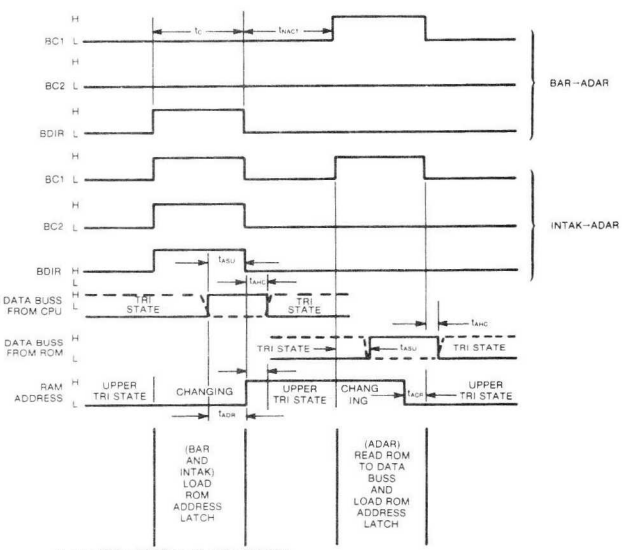
Standard Conditions (V_{CC} = 5±10%; t = 0°, 70°C)

Characteristic	Symbol	Min.	Typ.*	Max.	Units	Conditions
DC CHARACTERISTICS						
Logic '0' Input	V_{IL}	0	—	0.6	V	
Logic 'I' Input	V_{IH}	1.4	—	V_{CC}	V	
Logic '0' Output	V_{OL}	0	—	0.4	V	I_{sink} = 1mA
Logic 'I' Output	V_{OH}	2.2	—	V_{CC}	V	I_{source} = 100μA
Input leakage	I_L	—	—	10	μA	
Power Supply Current	I_{CC}	60	—	70	mA	V_{CC} = 5.0V
AC CHARACTERISTICS						
ROM Data Access	t_{ACC}	250	—	350	ns	Fig. 1,5
ROM Data Hold	t_{AHC}	50	—	300	ns	Fig. 1,5
RAM Address Setup	t_{ADR}	150	—	250	ns	Fig. 1, 2, 3, 4
Control Setup	t_{CSU}	500	—	—	ns	Fig. 1
Address Setup	t_{ASU}	300	—	—	ns	Fig. 1
Control Hold Time	t_{OHC}	50	—	—	ns	Fig. 1
No Action Time	t_{NACT}	0	—	2000	ns	Fig. 1
Control Period	t_C	800	—	—	ns	Fig. 1, 2, 3, 4, 5
Code Time	t_{CP}	1600	—	2800	ns	Fig. 1, 2, 3, 4
No Action Time	t_{NACT}	500	—	2000	ns	Fig. 2, 3, 5
Data Setup	t_{DSU}	—	—	300	ns	Fig. 1, 2
RAM Address Hold	t_{AHR}	300	—	2000	ns	Fig. 2, 3, 4
RAM Access Time	t_{ACR}	150	—	300	ns	Fig. 2, 3
Master Clear	t_{MC}	100	—	10,000	ns	Fig. 5



* Minimum hold time after DTB before going tristate. Maximum time to tristate = 300ns. (all time in nSec)
** BC1, BC2 and BDIR are return to zero signals
*** Upper tristate means that the upper push pull output device is disabled and an internal load resistor will hold the output positive
**** Proper CE address must be latched to allow ROM output to function during DTB
***** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 1



** BC1, BC2 and BDIR are return to zero signals
*** Proper CE address must be latched to allow ROM output to function during DTB
**** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 2

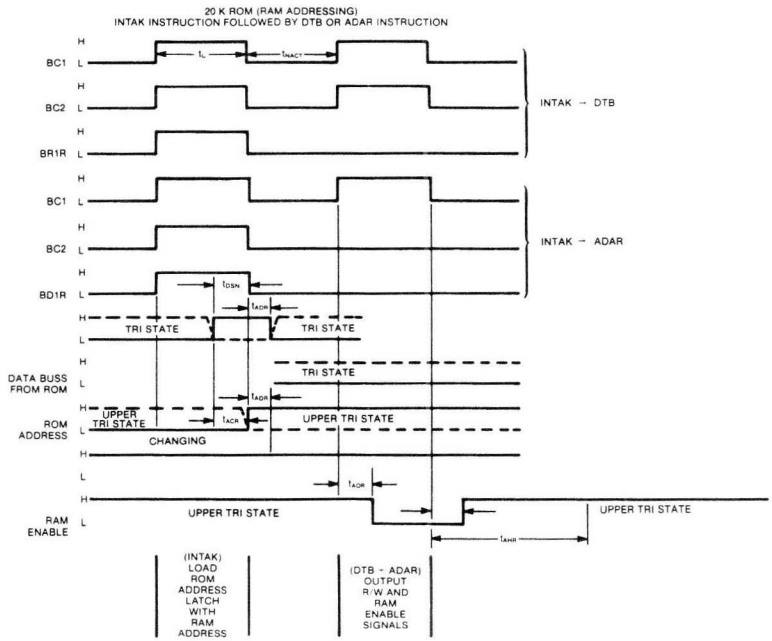
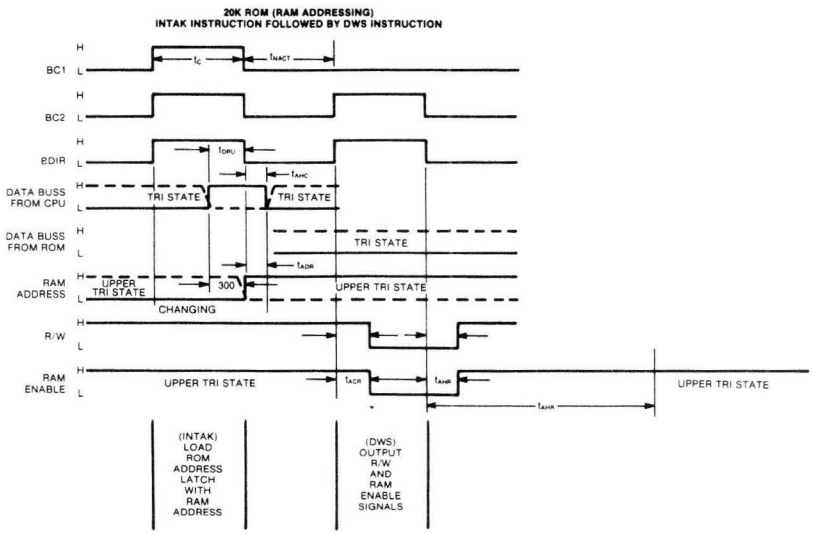
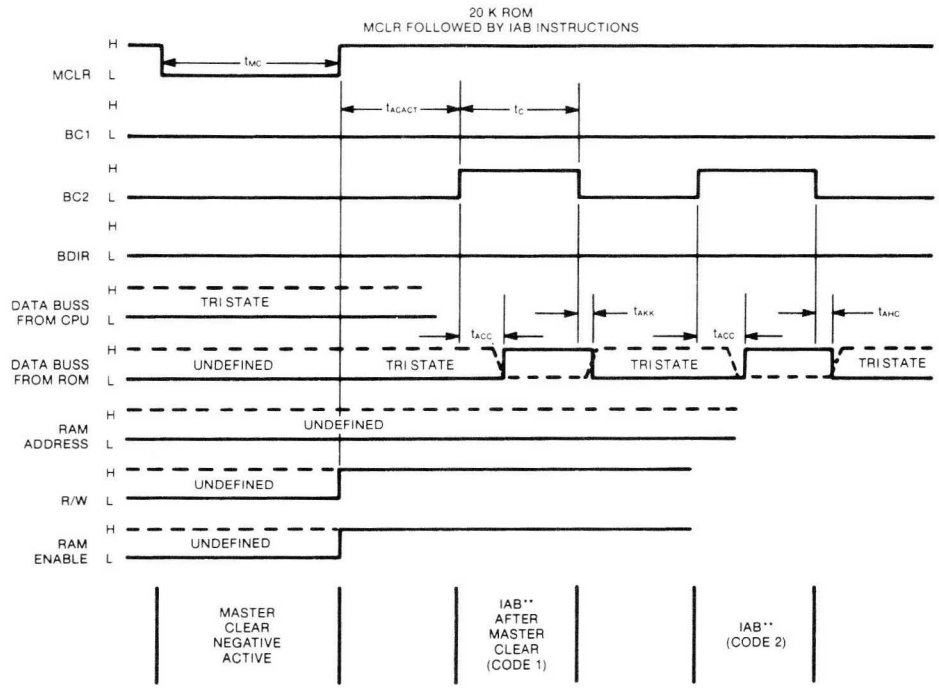


Fig. 3



* Maximum time to upper tri state condition
** RAM address has DB_{11} thru DB_{15} = Logic '0'
*** BAR or ADAR can be used instead of INTAK to load RAM address. If ADAR is used remember RAM address will be provided from ROM output to data buss if chip previously enabled.
(All time in nSec)

Fig. 4



* Minimum hold time after IAB before going tri state. Maximum time to tri state = 300 ns

** The first IAB after master clear will present a 16 bit programmable code to the data buss. Subsequent IAB instructions will output a second code that is gate programmable on ROM chip.

(All time in nsec)

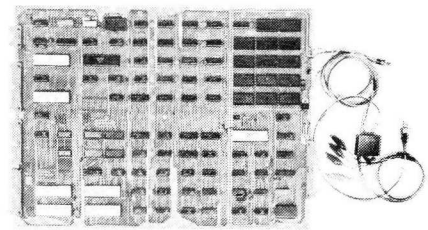
Fig. 5

SC1600: GIMINI Single Card Microcomputer Module

FEATURES

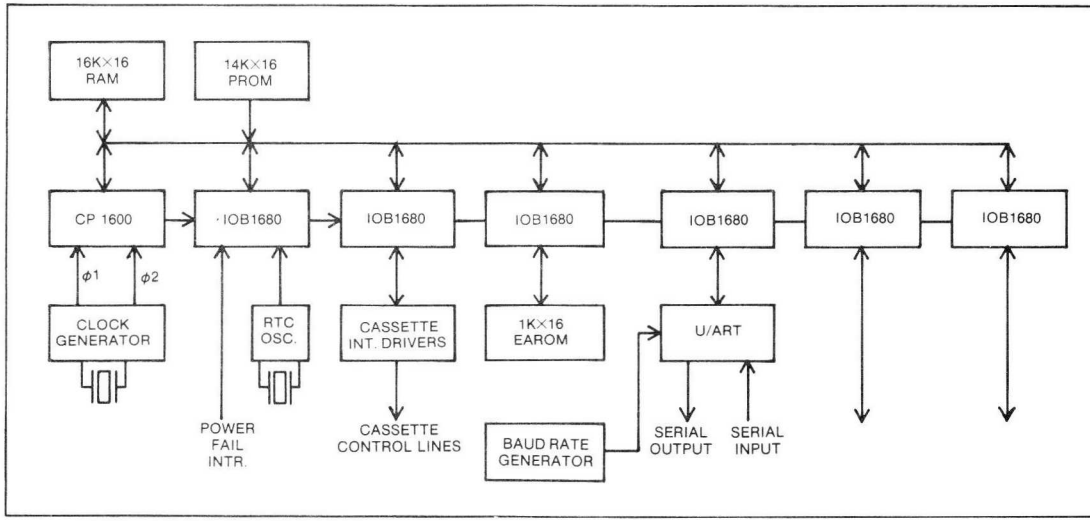
- CP1600 with multi-level priority interrupt structure and DMA channel for floppy disc
- 16K words of RAM
- 14K words of PROM sockets
- 1K words of EAROM (non-volatile electrically alterable read-only memory).
- Real Time Clock—crystal controlled with 4 strap selectable frequencies
- Power Down Interrupt Input
- Dual Cassette Interface
- UART-RS232 compatible Serial I/O Channel with program selectable baud rate
- Up to 16 Digital Output Lines with interrupt capability (IOB1680)
- Up to 16 Digital Input Lines with interrupt capability (IOB1680)
- Up to 5 Programmable 16-bit Timers
- Resident Operating Systems in PROM
- Resident Drivers for all I/O Functions

GIMINI SINGLE CARD MICROCOMPUTER



The SC1600 Single Card Computer is a complete microcomputer system on one P.C.B. and includes RAM, PROM, and EAROM memory, Cassette Interface, Real Time Clock, and 32 general purpose I/O lines. The RAM memory is constructed with 16K-bit dynamic RAMs and contains a complete refresh controller that is totally transparent to the processor. The PROM memory is constructed with 16K-bit ultra-violet erasable PROMs that are totally compatible with full processor speed. The EAROM memory is constructed with G.I.'s exclusive Electrically Alterable Memory that can be erased and reprogrammed on line by the processor without removal from the board. The I/O section of the board utilizes the IOB1680 input/output buffer chip to the CP1600 processor to implement the real time clock, power fail interrupt, dual Cassette Interface, U/ART Serial Communication Channel with both RS232 & current loop capability, and the 32 general purpose user controllable input/output lines. In addition, these IOB 1680 chips provide the programmable timers for customer use.

The SC1600 Single Card Microcomputer Module is a 12½" x 17" printed circuit card.

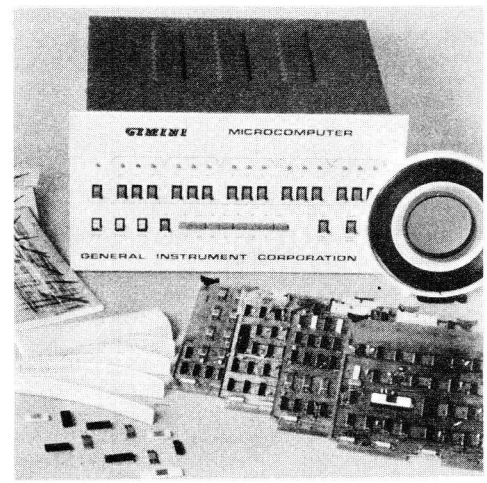


16-Bit Microcomputer Systems

FEATURES

- Built around the General Instrument's CP1600 MOS N-Channel Microprocessor.
- Complete microcomputer system to enable rapid program development.
- Separate Data, Address and Control Buses.
- Up to 65K memory space.
- Unlimited DMA channels.
- Nested interrupt system with full priority resolution.
- Includes— MC1600 Microcomputer Module
  RM1602 8K RAM Memory Module
  I/O1600 TTY High Speed Reader Punch Interface Module
  CC1600 Control Console (Operator's Front Panel) and Control Console Module
  CF1600 Card File
  CA1600 TTY/EIA Cable Assembly
  CA1601 Reader/Punch Cable Assembly
  A full set of Software necessary to prepare and debug programs.

GIMINI MICROCOMPUTER



DESCRIPTION

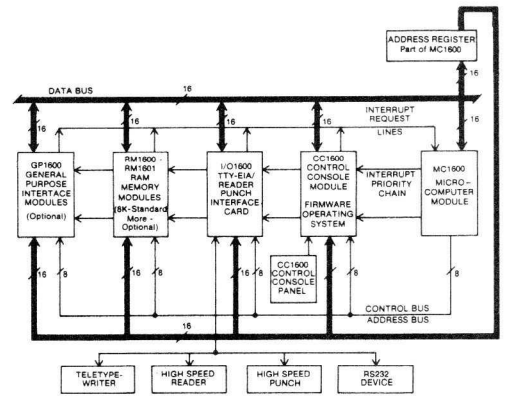
To simplify microprocessor hardware and software development, speed the product design cycle, and support product prototyping, a microcomputer development system and its associated components are a must. The Series 1600 family fills these requirements with the GIMINI Microcomputer—a versatile, general purpose, stand alone computer system built with the Series 1600 Semiconductor Components.

The GIMINI utilizes a totally modular design allowing the system designer maximum configurability. The system provides direct addressing to 65K words, unlimited DMA channels, and a multi-line/multi-level nested interrupt system with full priority resolution and self-identifying addresses. All control and timing signals as well as data and address buses are fully buffered and available for use in expanding memory or designing specialized I/O interfaces.

The basic hardware includes a card cage, front panel, and four printed circuit boards: the MC1600 Microcomputer Module, the RM1602 8K×16 RAM Memory Module, the CC1600 Control Console and Control Console Module, and the I/O1600 TTY-EIA/High Speed Reader Punch Interface Module. Up to 9 additional cards of any type can be added as required. With the addition of a TTY and a high speed reader/punch, the GIMINI becomes a test bed for customer designed interfaces and related hardware as well as a full program preparation facility. Its resident On-Line Debug Program allows testing of hardware and software directly on the system in real time and also totally eliminates the annoying bootstrap procedure. The On-Line Software Package provides the necessary program preparation aids, such as the Assembler, Super Assembler, Text Editor, the Relocating/Linking Loader and the Object Module Linker.

All of the card level modules of the GIMINI are available on an OEM basis for further system integration.

BLOCK DIAGRAM



GIMINI Accessories

FEATURES

CF1600 CARD FILE
- 13-position
- P.C. backplane with wirewrap capability
- Rack-mountable
- Cards are keyed to connectors
- 10.5" high x 19.0" wide x 12.0" deep

EX1600 EXTENDER CARD
- For use with all GIMINI cards
- Two 70-pin connectors

WW1600 WIREWRAP CARD
- 126 16-pin positions
- Power and ground planes provided
- 10 Test points on edge of card

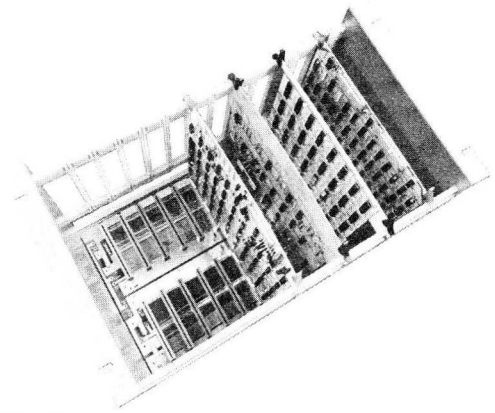
PS1600/PS1601 POWER SUPPLIES
- Provides all required voltages for the GIMINI Microcomputer System.
- PS1600 (115V, 60Hz): +5V at 12A; +12V at 2A; -12 V at 2A capability.
- PS1601 (200/250V, 50Hz): +5 at 15A; +12 at 2A; -12V at 2A capability.
- 1% line and load regulation.
- Remote sensing capability.

CA1600 TTY/EIA CABLE ASSEMBLY
- 6-ft. cable for connecting I/O1600 Interface Module to TTY or EIA compatible device.

CA1601 READER PUNCH CABLE ASSEMBLY
- 6-ft. Cable for connecting I/O1600 Interface Module with high speed reader-punch.

CA1602 GP1600 MODULE CABLE ASSEMBLY
- 6-ft. cable for connecting GP1600 Interface Module with external device.

CARD FILE



CF1600 CARD FILE

SLOT	CARD
1	MC1600 Microcomputer Module
2	CC1600 Control Console Module
3-12	Memory or I/O Cards
13	I/01600 TTY-EIA/Reader-Punch Interface Module

DESCRIPTION

The CF1600 Card File is designed to house up to 13 cards of the GIMINI family. The MC1600 Microcomputer Module, the CC1600 Control Console Module, and the I/O1600 TTY-EIA/Reader-Punch Interface Module each have one assigned position. The 10 remaining positions are available for memory modules, general purpose input-output cards, or special interface cards.

The printed circuit backplane parallels the power supply rails and the data, address and control buses for all 13 cards. There are separate voltage and voltage sense lines on the P.C. backplane for the +12V, -12V and +5V supplies. The bus system can be extended to another card file by wirewrapping or soldering a ribbon cable to one of the rear connectors.

The EX1600 Extender Card can be used with any other card of the GIC1600 family.

The WW1600 Wirewrap Card contains 126 16-pin sockets for prototyping special interface cards. Power and ground planes are provided.

The PS1600/PS1601 Power Supply provides all the power necessary to run the GIMINI Microcomputer System. The user has 2A of +12V and 2A of -12V available for extra memories and interfaces.

Also available is 9A of +5V if the system uses only one 8K RAM Memory Module. Special power supply configurations are available upon request.

The CA1600 TTY/EIA Cable Assembly is a 6' cable that has a 10-pin 3M connector to interface with the I/O1600 TTY-EIA/Reader-Punch Interface Module on one end. The other end is split into two sections: one is left unterminated for connection to a TTY; the other is terminated in a 25-pin data connector for connection to an EIA device.

The CA1601 Reader/Punch Cable Assembly is a 6' cable that has a 34-pin 3M connector to interface with the I/O1600 TTY-EIA/Reader-Punch Interface Module on one end. The other end is split into two sections: both are terminated in 25-pin data connectors, one for connection to the reader and the other for connection to the punch.

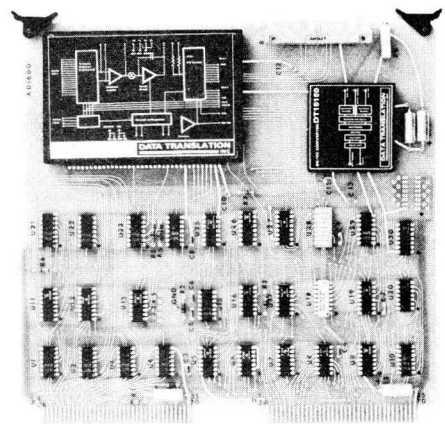
The CA1602 GP1600 Module Cable Assembly is a 6' cable that has a 34-pin 3M connector to interface with the GP1600 General Purpose Interface Module on one end. The other end is unterminated.

Analog to Digital Module

FEATURES

- 12-bit Analog to Digital Conversion
- ±10 volt inputs.
- 25KHz Standard Throughput Rate, Option 35KHz, 50KHz, 100KHz.
- 16 Channel Input.
- Plugs directly into GIMINI System.
- Operates from +5V DC source.
- Program controlled.
- Interrupt capability.
- Interfaces directly with MC1600 Module.

ANALOG TO DIGITAL MODULE



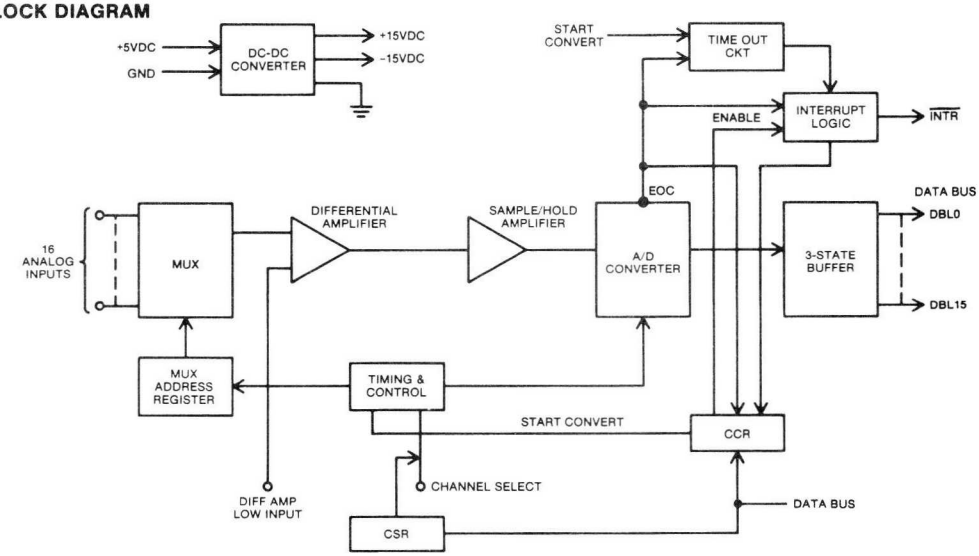
DESCRIPTION

The AD1600 is a multichannel analog data acquisition module which interfaces directly to General Instrument GIMINI microcomputers. The AD1600 provides 16 channels of ±10 Volt Analog to 12-bit 2's complement digital data with a standard conversion rate of 25KHz. Conversion rates of 35KHz, 50KHz and 100KHz are available.

The AD1600 is controlled via three operational registers which are used to select a specific analog input channel, start data conversion, determine when conversion is complete and input the resultant digital data. These registers are cleared initially when a console master clear is issued and set under program control.

The AD1600 is operated by first setting an analog input channel address (0-17) in the Channel Select Register (CSR). Analog to digital conversion is started by setting the Start Conversion bit in the Conversion Control Register (CCR). When the analog to digital conversion is complete the End Conversion bit in the CCR becomes a "1". This bit may be sampled under program control or if the CCR Interrupt Enable bit is set, an interrupt is generated when end of conversion occurs. If after a start convert signal is generated an end of conversion doesn't occur, the CCR Error bit is set instead of the End Conversion bit. This bit may also be sampled under program control or if the CCR Interrupt Enable bit is set, an interrupt is generated when the error bit becomes a "1".

BLOCK DIAGRAM

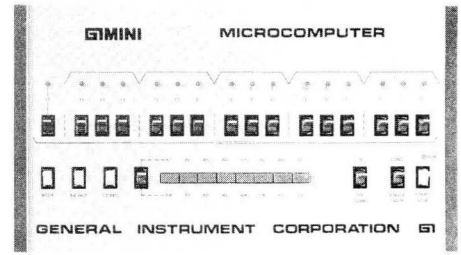


Control Console and Control Console Module

FEATURES

- 16-bit Data/Address Display
- 16-bit Switch Register
- Easy to use Control Panel:
  Display/Modify all 8 internal registers.
  Display/Modify the CPU Status Word.
  Display/Modify all 65K Memory Space.
  Single Instruction operation.
  Program Counter Inhibit capability
- ROM based Operating System:
  Conversational Monitor
  On-Line Debug Program/Software Breakpoints
  Relocating Loader (Eliminates Bootstrap)
  Memory Dump Program
  General Utilities/Input-Output Drivers
- Standard 19" × 10½" rack mountable Control Panel

CONTROL CONSOLE



DESCRIPTION

The CC1600 Control Console and Control Console Module is designed to provide a convenient method of controlling and monitoring the GIMINI System. The CC1600 consists of a front panel and a printed circuit module that are connected with two 34 pin flexible cables. The module contains the control logic to handle all front panel commands as well as the required interrupt logic to interface with the Microcomputer Module.

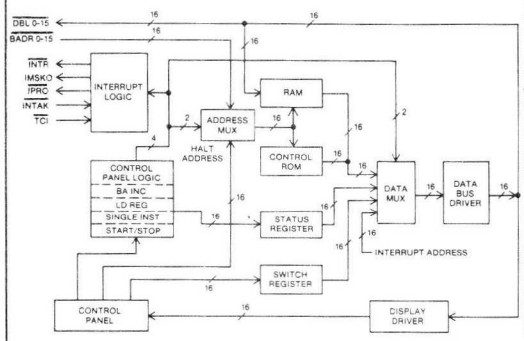
The Control Console Module consists of six control ROMs, scratch pad memory (256x16), a 16-bit Switch Register, a 16-bit Display Register, and the control logic to service any front panel request.

All functional operations for the Control Console are performed by the execution of program stored in the control ROMs. Pressing any action switch on the Control Console results in an interrupt request to the CP1600. After this interrupt is acknowledged, the CC1600 supplies the starting address of the Control Console service routine which performs the required function. In addition, the program automatically stores all CP1600 register in the scratch pad memory which is accessible via front panel selection. Consequently, whenever the CP1600 is in the HALT mode, the Control Console has direct access to all updated CP1600 information.

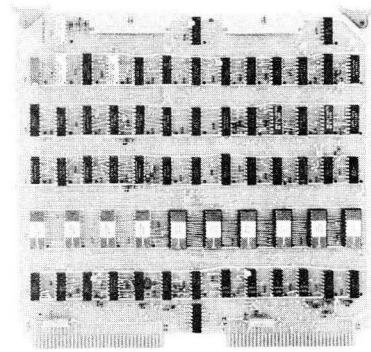
The control ROMs also contain all the firmware necessary for the development of micro-processor based systems. An On-Line Debug program is included so that software breakpoints and memory search routines may be executed. The system monitor allows the user to maintain conversational control via teletype interaction. The Relocating Loader can be used to input data from either a TTY or High Speed Reader, while the Memory Dump program allows any block of memory to be punched onto paper tape.

The Control Console Module is packaged on a 9.75" x 9.25" P.C. board, which mates with a dual 70-pin connector. It also interfaces with two 34-pin connectors for connection to the control console. Its operating temperature is 0° C to 55° C. It requires +5V +5% at 1.0A.

BLOCK DIAGRAM



CONTROL CONSOLE MODULE



DA1600: Digital to Analog Module

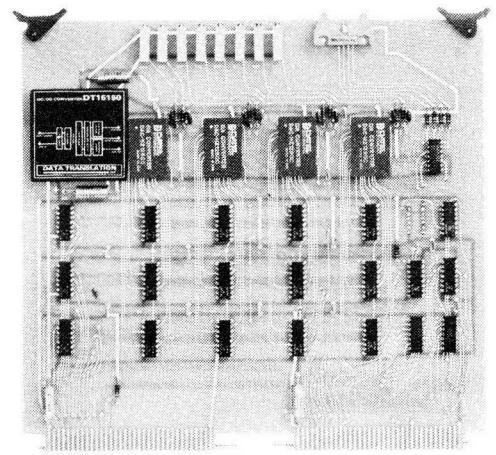
FEATURES

- 4 D/A's on One Card
- 12-Bit Resolution
- ± 10 Volt Outputs

DESCRIPTION

The DA1600 is a multichannel digital to analog data output module which interfaces directly to GI's GIMINI Microcomputers. The DA1600 provides four separate 12-bit 2's complement digital to ± 10 Volt analog outputs. Each of the four analog outputs is controlled by a corresponding Analog Data Register (ADR) which has a unique bus address. A stabilized analog output signal is generated in a maximum of 3μs after a 12-bit digital quantity is placed in the corresponding ADR. The four analog outputs are initially set to zero Volts when a console master clear is issued and are under program control thereafter. The DA1600 Digital to Analog Module is contained on a 9.75"×9.25" PC board which mates with a dual 70 pin connector.

DIGITAL TO ANALOG MODULE



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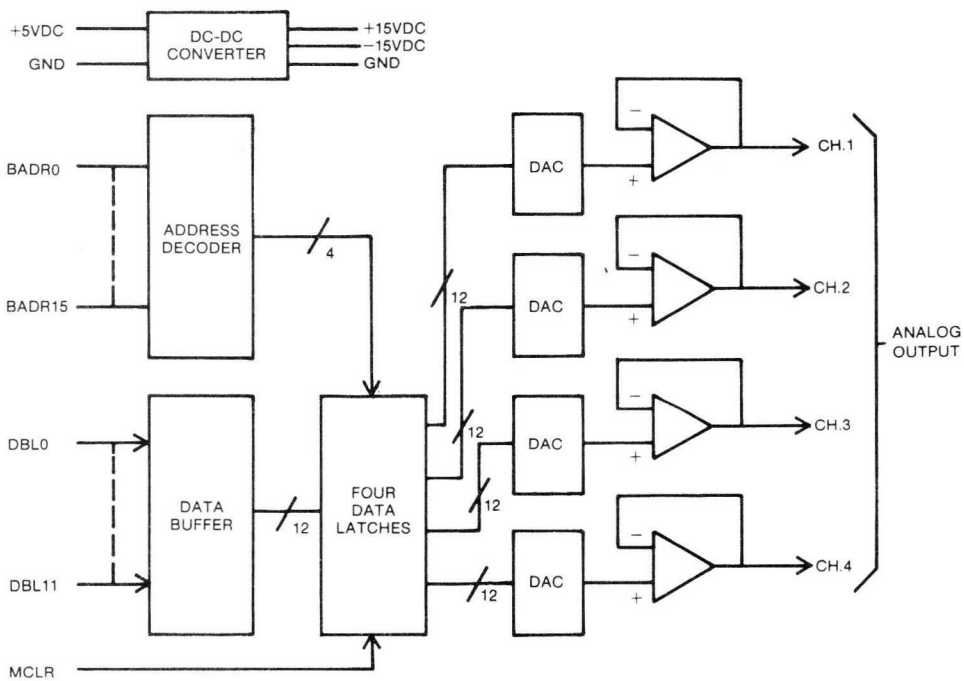


General Purpose Interface Module

FEATURES

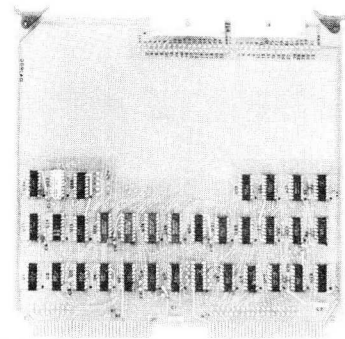
- 1 16-bit Addressable Input Port
- 1 16-bit Addressable Output Port
- 2 Addressable Status Registers
- Interfaces directly with MC1600 Module
- Space provided for sockets for I/O Control Logic
- Full Interrupt Capability.

DESCRIPTION

The GP1600 General Purpose Interface Module has two software addressable ports: one 16-bit input port and one 16-bit output port. Each port has an associated 4-bit status register that is addressable via program control. Provision is made so that the peripheral device can be operated on an interrupt or polling basis. Address decoding for the module is provided on the card although specific port assignments are determined by backplane selection. It is therefore possible to use up to eight GP1600 in a given system.

Connection to a given peripheral device is accomplished by a flat ribbon cable. Dual 34 pin connectors are mounted at the top end of the module. Space has been provided to accommodate wire wrap sockets so that specific interface circuitry may be incorporated on the module. Control and data signals have been brought out to wire wrap pins to facilitate prototype development.

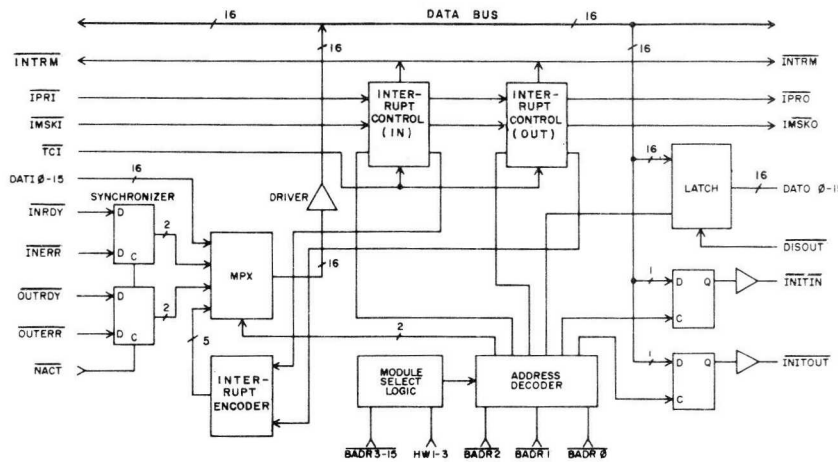
GENERAL PURPOSE INTERFACE MODULE



The module will accept dual-in-line package components mounted in standard wire wrap sockets. Locations for 14, 16, 22, 24 pin sockets are available.

The GP1600 General Purpose I/O Module is a 9.75" x 9.25" printed circuit card. Its operating temperature range is 0° C to 55° C.

BLOCK DIAGRAM



TTY-EIA/Reader-Punch Interface Module

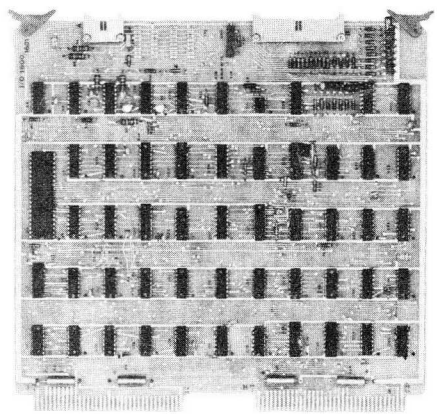
FEATURES

- Teletype Asynchronous Transmitter-Receiver and Control (UAR/T)
- High Speed Reader/Punch Controller
- EIA (RS-232C) Interface
- Interfaces directly with MC1600 Microcomputer Module
- TTL Compatible to I/O Peripherals

DESCRIPTION

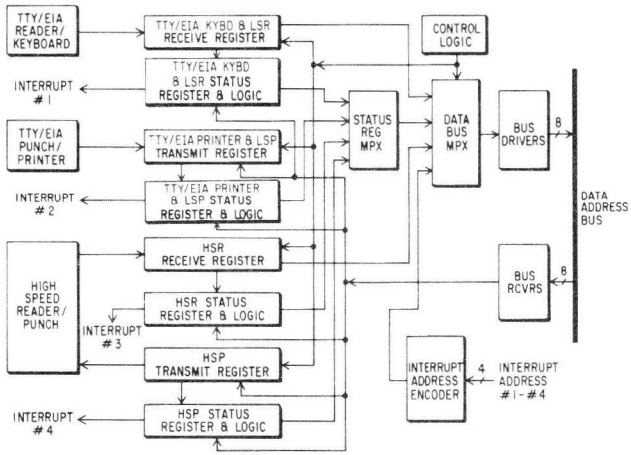
The I/O1600 TTY-EIA/Reader-Punch Interface Module handles full duplex communication between a Teletype, High Speed Reader/Punch combination or any RS-232C compatible device and the MC1600 Microcomputer Module. The I/O1600 Module has complete interrupt capability with four separate channels: two for the receiver section, High Speed Reader and TTY Reader/Keyboard; and two for the transmitter section, High Speed Punch and TTY Punch/Printer. These four interrupt channels operate independently with the receiver sections taking priority over the transmitter sections on simultaneous interrupts. The High Speed Reader/Punch has a higher priority than the TTY. Electrically, the I/O1600 Module has a 20 mA current loop for TTY operation and a TTY reader control line which allows the microprocessor to control the Teletype reader during on-line operation. The High Speed Reader/Punch interface controls a high speed Reader/Punch combination capable of reading paper tape at 300 characters per second and punching tape at 60 characters per second. The I/O1600 module also provides the additional capability of interfacing with any RS-232C compatible terminal.

TTY-EIA/READER-PUNCH INTERFACE MODULE



The I/O Module is a 9.75" × 9.25" P.C. board, which mates with a dual 70 pin connector. It also interfaces with a 10 pin connector for the TTY and a 34 pin connector for the high speed reader/punch. Its operating temperature is 0°C to 55°C. It requires +5V±5% at .5A, +12V±5% at .2A and -12V±5% at .2A.

BLOCK DIAGRAM



PRELIMINARY INFORMATION

Floppy Disc Interface Module

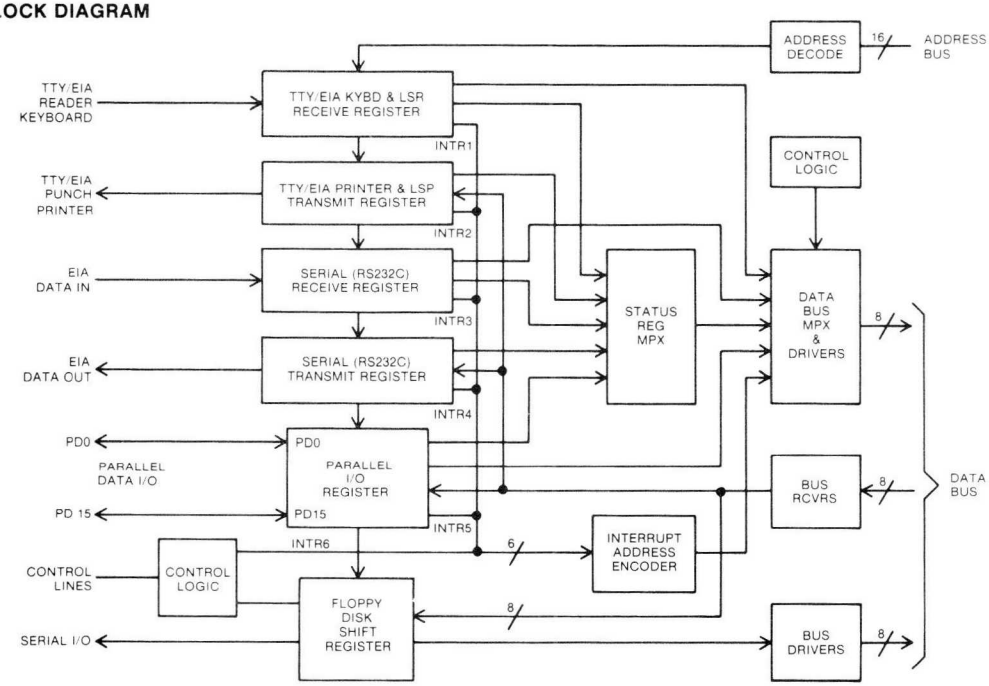
FEATURES

- Two EIA (RS-232C) Asynchronous Transmitter-Receiver and Control ports (UAR/T).
- One 16-bit port or dual 8-bit ports for bi-directional input/output (IOB 1680).
- Floppy disc interface.
- Complete interrupt capability.

FLOPPY DISC INTERFACE MODULE

Under Development

BLOCK DIAGRAM



MC1600

Microcomputer Module

FEATURES

- Complete microcomputer module with system clocks, memory interface, and fully buffered Address, Data, and Control Buses
- Built with General Instrument's CP1600 MOS N-Channel microprocessor
- Two Phase CPU Clock
- Direct and Register Addressing up to 65K memory space
- Memory stack pointer
- Two Programmable Interrupt Lines/Multi-Level and Self Identifying
- DMA Channel Capability
- 16 External Sense Conditions for Conditional Branching
- Generalized Initialization Logic
- Real Time Clock Interrupt
- Power Fail Interrupt

DESCRIPTION

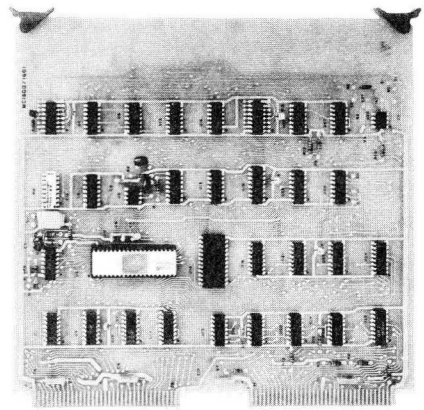
The MC1600 Microcomputer Module is a complete 16-bit parallel processing unit. It contains the hardware necessary to interface with memory and I/O. This is the main module in the GIMINI System.

The Microcomputer Module is designed around the CP1600, a 16-bit microprocessor on a chip. The MC1600 contains a 16-bit wide Bidirectional Bus Driver, Address Register and Driver, Bus Control Decoder-Driver, Crystal Oscillator, Clock Driver, an External Branch Multiplexer, A Real Time Clock Interrupt and a Power Fail Interrupt.

Two line, multi-level interrupt capability and Direct Memory Access are provided on this module. In response to an interrupt, the microcomputer automatically saves the current Program Counter on the Memory Stack, resolves interrupt priority and vectors to the device's interrupt service address. The direct memory access capability allows an alternate source to access memory or I/O while temporarily suspending processor operation. At the completion of a DMA operation, normal program execution continues in normal fashion.

The Microcomputer Module is a 9.75" × 9.25" P.C. board, which mates with a dual 70 pin connector. Its operating temperature range is 0°C to 55°C. It requires +5V±5% at .5A, +12V±5% at .1A and −12V±5% at 4 ma.

MICROCOMPUTER MODULE



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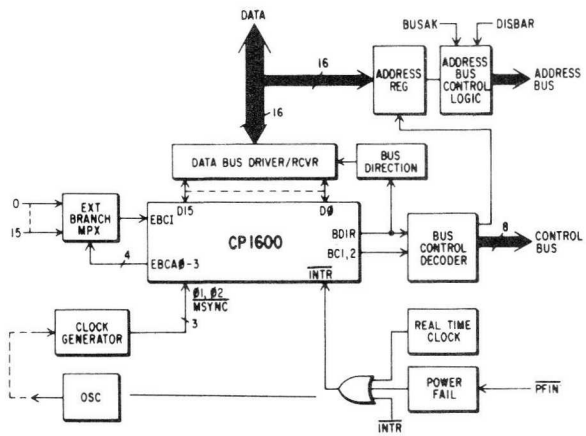


Microcomputer Module

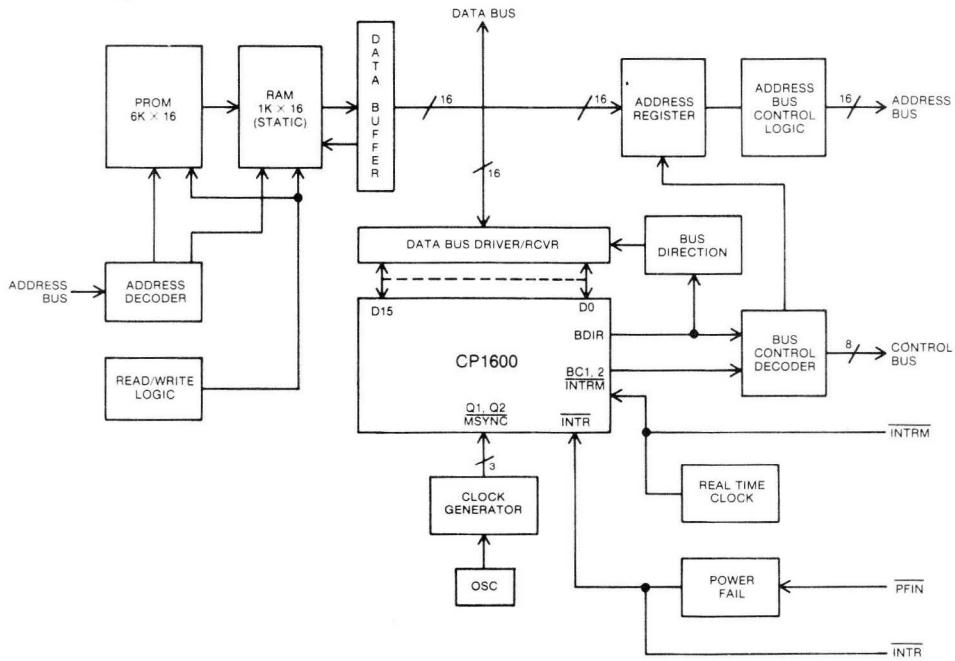
FEATURES

- All features of the MC1600 plus the following additional features.
- PROM based operating system.
- Conversational monitor.
- On-line debug program/software breakpoints.
- Relocating loader (eliminates bootstrap).
- Memory dump program.
- General utilities.

MICROCOMPUTER MODULE

Under Development

BLOCK DIAGRAM



PROM Memory Module

FEATURES

- Provides sockets for up to sixteen PROMs (4096×16)
- Static Memory - no clocks required
- Field programmable
- Erasable with short wave ultra-violet light
- 1 μs max. access time
- Buffered TTL inputs - 1 load
- Open collector TTL output - 30 loads
- Module decoding for 65K memory expansion

DESCRIPTION

The PM1600 PROM Memory Module is a standard 4096×16 memory module for use in the GIMINI Microcomputer System.

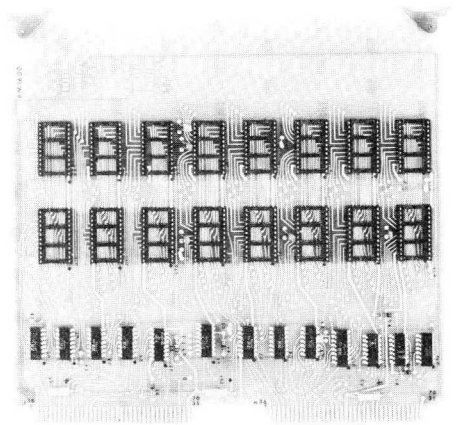
It is useful during the initial product design phase before freezing the program for a production quantity of lower cost masked ROMs, such as General Instrument's 16K RO-3-8316A(2K×8).

This memory module has sixteen sockets for 4096-bit static read-only memories. Each row of 8 rows will provide 512 16-bit words of memory. Each row contains 2 PROMs.

The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the PROMs. The sixteen data outputs from the PROMs are buffered onto the Data bus of the GIMINI System. For memories larger than 4K×16, decoding on the module allows addressing for a total of 65K memory.

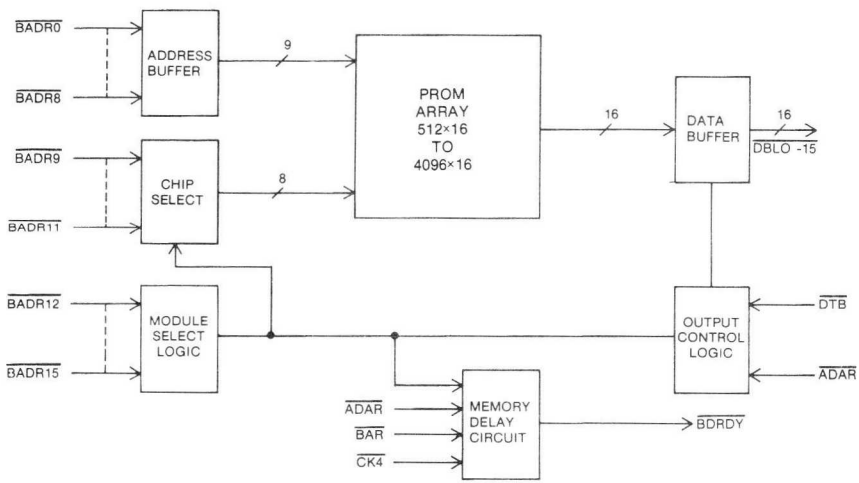
A special memory delay circuit is also provided on the board and is used to insure that the CP1600 microprocessor waits until stable data is available from the PROMs.

PROM MEMORY MODULE



The PM1600 PROM Memory Module is a 9.75"×9.25" P.C. board, which mates with a dual 70 pin connector. Its operating temperature range is 0° to 55°C. A board fully loaded with all 16 PROMs will require +5±5% at .5A and -12±5% at .5A.

BLOCK DIAGRAM



PROM Programmer Module

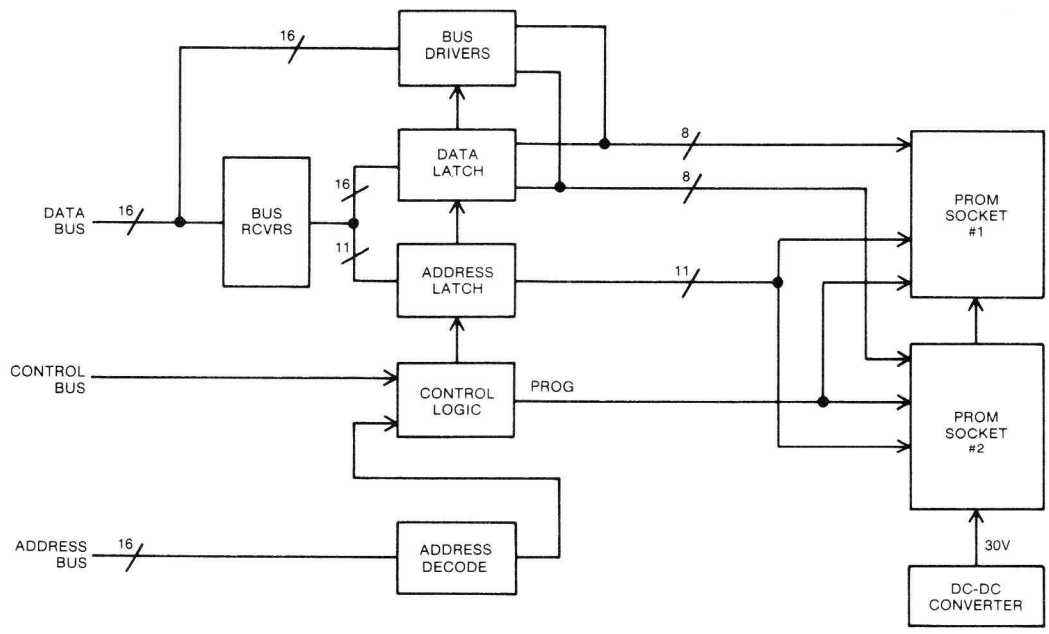
FEATURES

- Programs two 2708's or two 2716's simultaneously (16-bit word programming).
- Verification feature.
- Copy feature.

PROM PROGRAMMER MODULE

Under Development

BLOCK DIAGRAM



8K×16 Static Memory Module

FEATURES

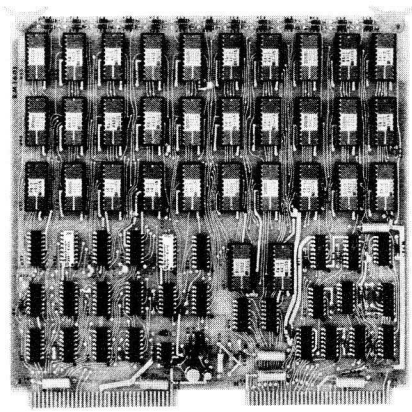
- 8192 — 16-bit words per module.
- Static memory, no clocks required.
- Byte or Word Capability.
- Module decoding for 65K memory expansion.
- 400 ns Read Time.
- 500 ns Cycle Time.
- Open Collector TTL Outputs—30 Loads
- Buffered TTL Inputs—1 Load

DESCRIPTION

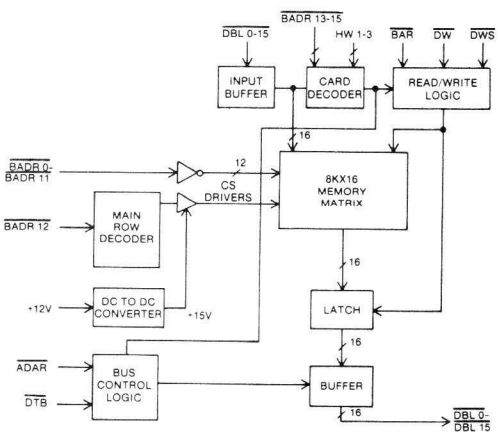
The RM1601 Memory Card is a standard 8Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, low or high byte word selection logic, and is implemented with General Instrument's RA-3-4402 4096 bit static Random Access Memory. There are thirty-two 22 pin 4Kx1 static RAM's packaged on a 9.75" x 9.25" x .062 printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0° C to 55° C. It requires +5V ±5% at 0.5A typical, +12V ±5% at 0.5A typical and -12V ±5% at 0.1A typical. The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System.

If more than one 8K memory card is used in the GIMINI System, provisions are provided for proper selection of 8K increments, up to 65K (8 modules) memory space.

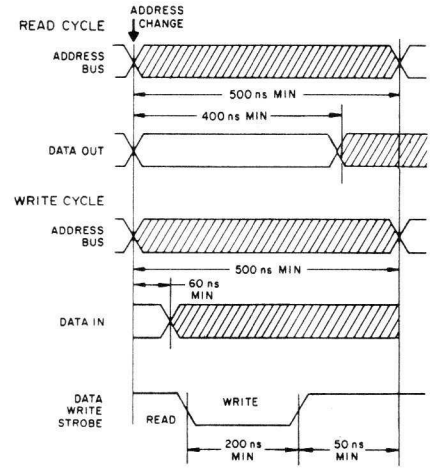
8K×16 STATIC RAM MEMORY MODULE



8K×16 MEMORY CARD



TIMING DIAGRAMS



8K×16 Dynamic RAM Memory Module

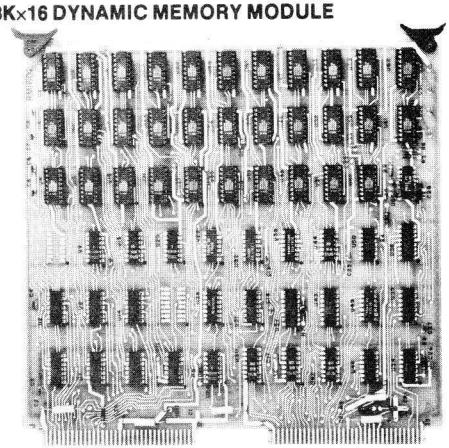
FEATURES

- 8192 — 16-bit words per module.
- Dynamic memory with Refresh logic (Refresh during no-action state of CP 1600).
- Byte or Word Capability
- Module decoding for 65K memory expansion
- 400ns Read time
- 500ns Cycle time
- Open collector TTL outputs - 30 loads
- Buffered TTL Inputs — 1 Load

DESCRIPTION

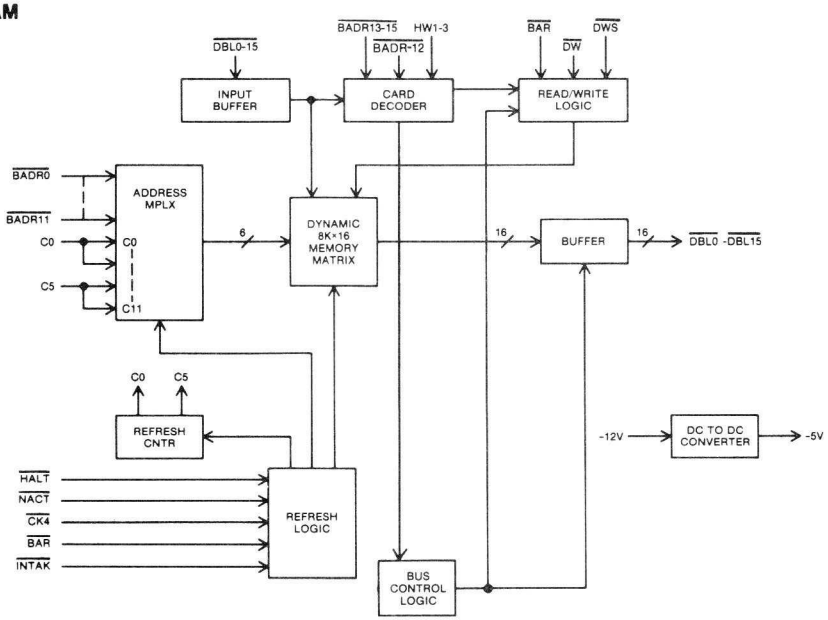
The RM 1602 Memory Card is a standard 8Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, refresh logic, address multiplexer, low or high byte word selection logic. There are thirty-two 16-pin 4Kx1 dynamic RAM's packaged on a 9.75"x9.25"x.062 printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0° C to 55° C. It requires +5V ±5% at .2A, +12V ±5% at .5A, typical, and -12V ±5% at 0.02A typical. The address bus inputs from the GIMINI to the memory card are buffered and multiplexed to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System.

8K×16 DYNAMIC MEMORY MODULE



If more than one 8K memory card is used in the GIMINI system, provisions are provided for proper selection of 8K increments, up to 65K (8 modules) memory space.

BLOCK DIAGRAM



RM1610

PRELIMINARY INFORMATION

8K/16K/32Kx16 Dynamic RAM Memory Module

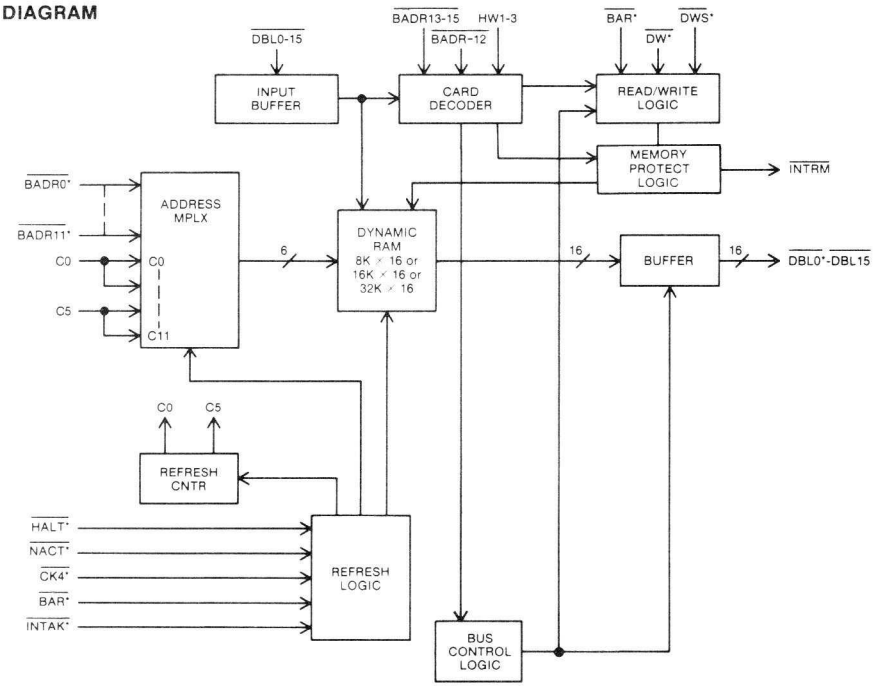
FEATURES

- 8K/16K/32K - 16-bit words per module.
- Dynamic memory with refresh logic (refresh during NO-ACTION state of CP1600).
- Byte or word capability.
- Module decoding for 65K memory expansion.
- Memory protect.
- Open collector TTL outputs-30 loads
- Buffered TTL inputs - 1 load.

8K/16K/32Kx16 RAM MEMORY MODULE

Under Development

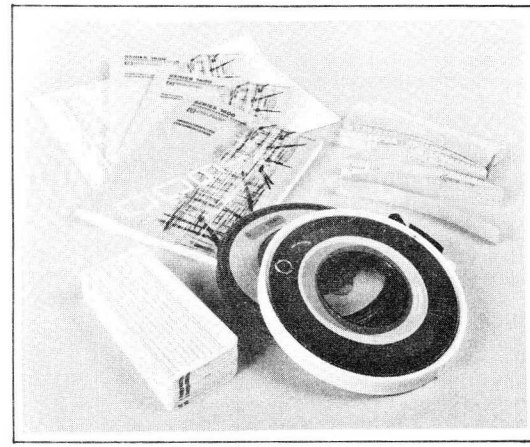
BLOCK DIAGRAM



Software

FEATURES

- Cross Software Package including Assembler/Simulator programs.
- On-Line Software Package for Program Preparation on Microcomputer.
- Resident Firmware in ROMS on Control Console Module in GIMINI Microcomputer allows conversational debugging of programs.
- Subroutine Library: Math packages, Code Conversion routines, String Operators, etc.



DESCRIPTION

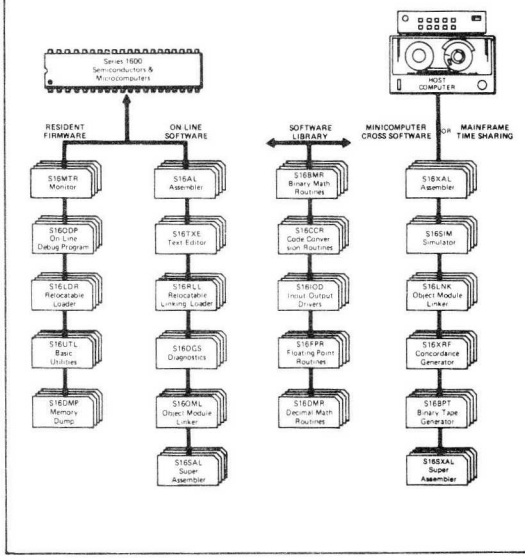
Software is fundamental to making every microprocessor come alive and the Series 1600 is no exception. The entire product family is supported by an extensive software system designed to make program development fast and efficient. Most important, the software structure is designed to grow with the hardware to insure a long term product continuity.

The Series 1600 Cross Software Package contains a versatile set of program preparation tools including compatible Assembler/Simulator programs operating at two different computer system levels—large machine or time share, or popular minicomputer systems. Each accepts Series 1600 assembly language statements as input and produce relocatable, linkable object code as output. In addition, the full microprocessor environment, including I/O operations, is simulated on the host machine so that complete program debugging and testing can be performed before committing to hardware. The combination of these features along with the ability to use a minicomputer as a host processor results in the lowest cost, easiest to use, Cross Software Package in the industry.

The GIMINI Microcomputer System also serves as a program preparation and hardware debug facility with the aid of its resident firmware and the On-Line Software Package. The resident firmware consists of a basic operating system containing a Monitor, the On-Line Debug Program, the Relocating Loader, the Memory Dump Program, and a number of other basic utility routines. The firmware also supports the system I/O with generalized routines for input/output from a TTY, high speed paper tape reader/punch, or any RS232 compatible device.

The On-Line Software Package includes the Symbolic Assembler, the Text Editor and the Relocating/Linking Loader, the Object Module Linker and the Super Assembler. The Object Module Linker provides the same features as S16LNK allowing generation of relocatable or absolute load modules on-line. The Super Assembler allows programs to be coded using high level procedure oriented statements while providing all the flexibility of basic assembly language.

SOFTWARE LINEUP



S16XSFT CROSS SOFTWARE PACKAGE

The Series 1600 Cross Software Package is coded in low level Fortran IV and is specifically designed to operate in a 16-bit minicomputer environment. The Cross Software package has been installed on many popular minicomputer systems such as DGC NOVA and DEC PDP11. The Cross Software package has also been installed on many popular time-sharing computer systems.

S16XAL CROSS ASSEMBLER
Symbolic representation of all instructions
User defined six character symbols
Octal, decimal, hexadecimal and ASCII literals
Expression evaluation
Extensive assembly directives
Absolute, Relocatable or Relocatable/Linkable assembly
Full program and sorted symbol listing
Extensive error detection

S16XRF CONCORDANCE GENERATOR
Assembly symbol cross reference map

S16LNK OBJECT MODULE LINKER
Resolves global/external symbol linkages
Relocates and merges object modules
Produces relocatable/absolute load module
Produces load module map

S16SIM SIMULATOR
Full Series 1600 Instruction set simulation
Full 65K word memory simulation
I/O and interrupt simulation
Memory and/or Register breakpoints
Memory and/or Register traces
Simulated program execution time accumulation
Program execution time and stack size limits
Inspection and modification of memory and registers
Symbolic memory addressing

S16BPT BINARY PAPER TAPE GENERATOR

S16RTG ROM PATTERN TAPE GENERATOR

S16SXAL SUPER ASSEMBLER
High level procedure oriented instructions plus all features of S16XAL.

GIMINI RESIDENT FIRMWARE

The resident firmware in the GIMINI Microcomputer System creates an efficient, easy to use, prototyping tool for the development of microprocessor based products. The firmware performs all front panel functions as well as creating a terminal driven operating environment. Features include the following:

S16MTR MONITOR
Conversational system control
TTY communications

S160DP ON-LINE DEBUG PROGRAM
Eight program breakpoints
Register/Memory display and modify
Memory search and initialize
Single step/Execute commands
Modify Branch and Jump destinations
Module Relocation Origins

S16LDR RELOCATING LOADER
Full relocation capability
TTY or H.S. Paper Tape Reader input

S16MDP MEMORY DUMP PROGRAM
Punches in S16LDR format
TTY or H.S. Paper Tape Punch output
Generalized Code Conversions
TTY input/output driver
H.S. Paper Tape Reader/Punch driver

SERIES 1600 ON-LINE SOFTWARE PACKAGE

The Series 1600 On-Line Software Package is written in assembly language and runs on the GIMINI Microcomputer System. All programs are designed to be directly input/output compatible with the S16XSFT Cross Software Package so that either means of program preparation can be used interchangeably.

S16AL ASSEMBLER
Same features as S16XAL

S16TXE TEXT EDITOR
Multiple line buffering
Symbol search
Character, line, string editing

S16RLL RELOCATING/LINKING LOADER
Global and external symbol resolution
Full relocation capability
Loads and links multiple object modules
Memory map

S16DGS DIAGNOSTICS
Memory diagnostic
Instruction test
I/O Controller exerciser

S16OML OBJECT MODULE LINKER
Same features as S16LNK

S16SAL SUPER ASSEMBLER
High level procedure oriented instructions plus
All features of S16AL.

SERIES 1600 SUBROUTINE LIBRARY

The Series 1600 Microprocessor System is supported by an extensive and growing library of useful subroutines designed to relieve the user of many time consuming software chores. All of Subroutine Library programs are written in Series 1600 Assembly Language making them both fast and efficient. They are compatible with both the Series 1600 Symbolic Cross Assembler (S16XAL) and the Series 1600 On-Line Assembler (S16AL). In addition, all library programs are designed to be directly compatible with hardware extensions to the Series 1600 product family so that increased performance can be achieved without software complications.

S16BMR BINARY MATH ROUTINES
Signed Multiply/Divide
Square Root
Double Precision Multiply/Divide
Double Precision Square Root

S16CCR CODE CONVERSION ROUTINES
Binary to BCD—BCD to Binary
Binary to ASCII—ASCII to Binary
Binary to HEX—HEX to Binary
Binary to OCTAL—OCTAL to Binary
Fixed to Floating—Floating to Fixed

S16IOD INPUT/OUTPUT DRIVERS
TTY Input/Output
H.S. Paper Tape Reader/Punch Input/Output
Byte Table Pack—Byte Table Unpack

S16FPR FLOATING POINT ROUTINES
Floating Add/Subtract
Floating Multiply/Divide
I/O Conversion

S16DMR DECIMAL MATH ROUTINES
Decimal Add/Subtract
Decimal Multiply/Divide
Decimal Square Root
Decimal Compare

Super Assembly Language

FEATURES

- High level operations: LET, GOTO, GO@, CALL, IF, IF-THEN, IF-THEN-ELSE, DO, DO-FOR, DO-WHILE.
- Array subscripting
- Literal representation in Binary, Octal, Decimal, Hexadecimal and character notation.
- Symbolic representation of all CP1600 instructions.
- Directives for:
  - Controlling register utilization of high level operations
  - Controlling storage allocation
  - Initializing storage
  - Specifying character strings
  - Declaring a program entry point
  - Declaring global and external symbols
  - Declaring a program entry point
  - Specifying assembly output form
  - Controlling conditional assemblies
- Absolute and Relocatable load module output
- Absolute and Relocatable linkable object module output
- Program listing
- Extensive error diagnostics

DESCRIPTION

The General Instrument Super Assembly Language enables the CP1600 user to implement programs at a procedural level using FORTRAN-like statements rather than at the machine level of conventional assembly languages. Super Assembly Language includes LET, IF, CALL, DO, GOTO, and GO@ high level operations as well as all the instruction mnemonics and assembly directives of basic CP1600 assembly language. Super Assembly Language provides both the novice and the experienced programmer with the convenience and efficiency of procedural level programming while retaining the flexibility and economy of basic assembly language. Many applications can be completely coded using the high level operations, but when required, basic assembly statements can be intermixed freely with high level statements. The CP1600 Super Assembly Language is based on the popular high level programming languages, FORTRAN and BASIC.

The Super Assembler Program converts source programs written in CP1600 Super Assembly Language into binary machine code. This conversion process is accomplished by making two passes through a source program. The Super Assembler Program also produces a listing of the assembled program; the full instruction expansion into machine assembly language for each high level statement may be printed on the listing, if the expanded listing option is selected by the user.

HIGH LEVEL STATEMENTS

GOTO

The GOTO statement is used to transfer program control unconditionally to a specified destination.

```
Ex.: GOTO     SCAN
```

GO@

The GO@ statement is used to transfer program control unconditionally indirectly through a specified storage designator to a destination. The destination is defined by the current contents of the storage designator.

```
Ex.: GO@      TABLE (I)
```

CALL

The CALL statement is used to transfer program control to a subroutine. Arguments, i.e., parameters to be passed to the subroutine, follow the subroutine name enclosed in parenthesis and separated by commas.

```
EX.: CALL     SQRT(I,J)
```

LET

The LET statement is used to perform data transfers, arithmetic computations and logical operations involving constants, variables and subscripted variables. Addition, subtraction, multiplication, division, negation and logical NOT, AND, exclusive OR and inclusive OR operations may be performed using the LET statements.

```
EX.: LET X = .NOT.Y .AND. Z * 5
```

IF

The IF statement is used to perform tests on single quantities and make comparisons between two quantities. The quantities may be constants, variables, assembly expressions and subscripted variables. An IF statement may be of three types: arithmetic, conditional or relational. The arithmetic IF is used to test a quantity for negative, zero and positive and directly transfer to a corresponding destination. The conditional IF is used to test a quantity for positive, negative, zero and non-zero and the relational IF is used to compare two quantities. The conditional and relational IF statements may execute a GOTO statement if true. They may also cause a THEN-ELSE (THEN, if true and ELSE, if false) sequence of instructions to be executed. The THEN-ELSE capability is a feature not found in FORTRAN or BASIC and is similar to the IF-THEN-ELSE facilities in more powerful languages such as ALGOL, COBOL and PL/I.

```
EX.: IF ANSWR .ZERO. GO TO NEXT
     IF QUANT .EQ. LIMIT THEN
     CALL SQRT(A)
     END
```

```
EX.: IF A .EQ. 2 THEN
     LET B=5
     ELSE
     LET B=6
     END
```

DO

The DO statement is used to perform looping and iterative operations by causing a sequence of statements between the DO statement and a corresponding CONT (CONTinue) statement to be executed repeatedly. Such a statement sequence is known as a DO loop. DO loops may be nested i.e., contain other DO loops up to a depth of four levels. When DO loops are nested, inner loops terminate before outer loops. DO loops may be controlled by FOR or WHILE conditions.

```
EX.: ABC  DO ABC FOR I=INIT, MAX, INCR
          IF (TBL (I) .EQ. QTY) GO TO GETOUT
          CONT
```

```
EX.: XYZ  DO XYZ WHILE QTY .GT. LIM
          LET K=K .AND. MASK
          LET QTY=K + INCR
          CONT
```

MICRO ELECTRONICS

SERIES 8000 MICROPROCESSOR

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
8 BIT MICRO-PROCESSOR SYSTEM	The LP8000 Logic Processor is a complete 8-bit single chip microprocessor with 48 general purpose internal registers. The 8-bit data bus is supplemented by a 6-bit address bus to give a 14-bit address capability.	LP8000	2-52
		LP6000	2-52
		LP1030	2-52
		LP1010	2-52
		LP1000	2-52

8-Bit Microprocessor System

FEATURES

- 2 Chip Minimum System (plus clock)
- 48 Accessible 8 Bit Internal Registers
- 48 Basic Instructions
- Binary and Decimal Arithmetic Capability
- Direct and Indirect Input Output Capability
- Automatic subroutine nesting on memory devices
- Family of development devices

DESCRIPTION

The Series 8000 Logic Processor System is designed to perform any digital function using far fewer packages than a TTL or CMOS implementation. Typically a 100 package system can be reduced to a three chip solution of LP8000 Processor, LP6000 Program Memory and LP1030 Clock Generator (two 40 lead DIP plus one 8 lead DIP). The consequent savings in development and production costs and increased reliability give the user many of the advantages of a customized LSI solution but without the restriction that it must be a high volume product.

The System is fabricated with General Instrument's P-channel Nitride Process which has a proven reliability and production history. All members of the Series 8000 family including Read Only Memories, General Purpose Input Output and Memory interface parts are fully compatible with each other.

The LP8000 Logic Processor Unit itself is a complete 8-bit single chip MOS-LSI Microprocessor. It has a modern computer architecture with forty eight general purpose internal registers. This, coupled with a binary and decimal capability arithmetic unit, allows a versatile and sophisticated implementation of a microcomputer system. The 8-bit Data highway is supplemented by a 6-bit Address bus to give a 14-bit address capability which permits access to 16,384 words in combination of program memory, data memory or peripheral devices. The address space consists of 64 "modules" which can be either 256 words of memory or one 8-bit bidirectional I/O port.

LOGIC PROCESSOR - LP (Part number LP8000)

The logic processor (LP) is the heart of the Series 8000 system. It performs all of the arithmetic and logical functions required and also controls all activities occurring in the Series 8000 system. It has 48×8 bit working registers and an 8 bit input/output interface to which external peripherals may be attached directly.

PROGRAM MEMORY - PM (Part number LP 6000)

The program memory PM contains a 1K x 8 bit memory which stores the user's program. This chip also includes the program counter which points to the current address. It is arranged at the top of a four word hardware stack which is controlled by the LP for subroutine nesting. Two directly addressable 8 bit I/O interfaces are included, so that a minimum system consisting of one LP and one PM has 24 I/O leads. Extra PMs can be connected to the main system bus, up to a maximum of 16K words. Each PM and I/O interface can be addressed by the LP, the module addresses being programmed at the same time as the customer's program.

MEMORY INTERFACE CHIP - MIC (Part number LP 1000)

The memory interface chip consists of an 11 bit program counter at the top of four word hardware stack. The address output are TTL compatible and enable any external 2K×8 bit memory to be addressed. Other circuits allow the MIC to interface directly to the Series 8000 system without any external components. It is intended for use when breadboarding systems or when using non-standard memory, e.g. diode matrix, core, etc.

The memory area can be extended by using several MIC/external memory combinations. The addresses are selected by hardwiring pins to V_{GG} or V_{CC}.

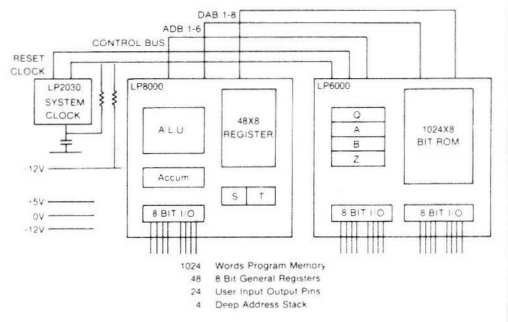
INPUT/OUTPUT BUFFER - IOB (Part number LP 1010)

The input/output buffer consists of two addressable 8 bit I/O interfaces. The addresses are selected by hardwiring pins to V_{GG} or V_{CC}.

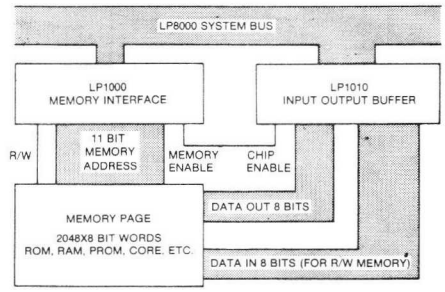
CLOCK GENERATOR - CG (Part Number LP1030)

The Series 8000 needs only an 800kHz clock, a power-on-reset signal to clear and synchronize the system and two power supplies. Virtually all external components may be eliminated by using the clock generator (CG). The frequency of the built in oscillator is determined by an external resistor or can be optionally over-ridden by an input from an external oscillator. A data synchronizing signal ϕ_{3N} is provided to act as an oscilloscope trigger and as a Data Valid signal for external hardware.

COMPLETE MINIMUM SYSTEM



MEMORY IMPLEMENTATION FOR DEVELOPMENT SYSTEMS



PIN FUNCTIONS

Processor Signals

DAB 1-8
Bidirectional 8-lead precharged data bus, used in conjunction with address bus to implement 14-bit address word.
ADB 1-6
Push pull 6-lead address bus. This 6-bit word specifies the memory 'module' address and the 8-bit data bus specifies the 1 of 256 'intra module address .

Processor Control Signals

CIO
Indicates direction of data flow on data bus.
CDA
Indicates if data bus is carrying data or address information.
CQZ
Used to select the Q counter or Z register for memory addressing.
CRA
Used to control the internal address stack.

Peripheral Signals

PEB 1-8
This is a bidirectional 8-bit latched input/output port with an open drain output configuration. In the case of the LP8000 chip the 8-bit port is organized such that only bits 5-8 are bidirectional, bits 1-4 are only available as inputs. For all other chips in the family the peripheral interfaces are 8-bit all bidirectional.

Drive Requirements

CLOCK
A single phase high level clock is required by the system and this would normally be provided by the LP1030 Clock Generator. The clock frequency used can be selected between 500 and 800kHz. With an 800kHz clock the machine provides a 5μsec machine cycle time.
RESET
This is a clock synchronized high level signal, normally provided by the LP1030 Clock Generator.
POWER
V_{CC} +5 Volt supply
V_{GI} 0 Volt (GND) supply
V_{GG} −12 Volt supply

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE
LP8000 LOGIC PROCESSOR*

Top View

V_{CC}	1	40	V_{GI}
Power on Reset	2	39	V_{GG}
Clock	3	38	CRA
Not Used	4	37	CQZ
Not Used	5	36	CDA
Data Bus 8	6	35	CIO
Data Bus 7	7	34	Not Used
Data Bus 6	8	33	Not Used
Data Bus 5	9	32	Not Used
Data Bus 4	10	31	Not Used
Data Bus 3	11	30	Not Used
Data Bus 2	12	29	Not Used
Data Bus 1	13	28	Not Used
Peripheral Bus 8	14	27	Address Bus 6
Peripheral Bus 7	15	26	Address Bus 5
Peripheral Bus 6	16	25	Address Bus 4
Peripheral Bus 5	17	24	Address Bus 3
Peripheral Bux 4	18	23	Address Bus 2
Peripheral Bus 3	19	22	Address Bus 1
Peripheral Bus 2	20	21	Peripheral Bus 1

40 LEAD DUAL IN LINE
LP6000 PROGRAM MEMORY

Top View

V_{CC}	1	40	Peripheral Bus A1
Data Bus 1	2	39	Peripheral Bus A2
Data Bus 2	3	38	Peripheral Bus A3
Data Bus 3	4	37	Peripheral Bus A4
Data Bus 4	5	36	Peripheral Bus A5
Data Bus 5	6	35	Peripheral Bus A6
Data Bus 6	7	34	Peripheral Bus A7
Data Bus 7	8	33	Peripheral Bus A8
Data Bus 8	9	32	Peripheral Bus B1
Not Used	10	31	Peripheral Bus B2
Power on Reset	11	30	Peripheral Bus B3
Address Bus 1	12	29	Peripheral Bus B4
Address Bus 2	13	28	Peripheral Bus B5
Address Bus 3	14	27	Peripheral Bus B6
Address Bus 4	15	26	Peripheral Bus B7
Address Bus 5	16	25	Peripheral Bus B8
Address Bus 6	17	24	V_{GI}
Clock	18	23	V_{GG}
CDA	19	22	CRA
CIO	20	21	CQZ

8 LEAD DUAL IN LINE
LP1030 CLOCK GENERATOR

Top View

V_{CC}	1	8	Reset Output
Timing Input	2	7	ϕ_{3N} Output
Synchronizing Input	3	6	Clock Output
Reset Input	4	5	V_{GG}

40 LEAD DUAL IN LINE
LP1010 INPUT/OUTPUT BUFFER

Top View

V_{CC}	1	40	Peripheral Bus A1
Data Bus 1	2	39	Peripheral Bus A2
Data Bus 2	3	38	Peripheral Bus A3
Data Bus 3	4	37	Peripheral Bus A4
Data Bus 4	5	36	Peripheral Bus A5
Data Bus 5	6	35	Peripheral Bus A6
Data Bus 6	7	34	Peripheral Bus A7
Data Bus 7	8	33	Peripheral Bus A8
Data Bus8	9	32	Peripheral Bus B1
Chip Select	10	31	Peripheral Bus B2
Power on Reset	11	30	Peripheral Bus B3
Address Bus 1	12	29	Peripheral Bus B4
Address Bus 2	13	28	Peripheral Bus B5
Address Bus 3	14	27	Peripheral Bus B6
Address Bus 4	15	26	Peripheral Bus B7
Address Bus 5	16	25	Peripheral Bus B8
Address Bus 6	17	24	PAD 4
Clock	18	23	V_{GG}
CDA	19	22	PAD 3
CIO	20	21	PAD 2

A pair of adjacent addresses is selected by PAD 4, PAD 3 and PAD 2 in the range 48 to 63, e.g. 011 selects peripheral addresses 54 and 55.

40 LEAD DUAL IN LINE
LP1000 MEMORY INTERFACE

Top View

V_{CC}	1	40	V_{GI}
Data Bus 8	2	39	V_{GG}
Data Bus 7	3	38	Address Bit 11
Data Bus 6	4	37	Address Bit 10
Data Bus 5	5	36	Address Bit 9
Data Bus 4	6	35	Address Bit 8
Data Bus 3	7	34	Address Bit 7
Data Bus 2	8	33	Address Bit 6
Data Bus 1	9	32	Address Bit 5
Power on Reset	10	31	Address Bit 4
Address Bus 1	11	30	Address Bit 3
Address Bus 2	12	29	Address Bit 2
Address Bus 3	13	28	Address Bit 1
Address Bus 4	14	27	Clock
Address Bus 5	15	26	R/W
Address Bus 6	16	25	Memory Enable
PAD 4	17	24	MIC Enable
PAD 5	18	23	CRA
PAD 6	19	22	CQZ
CIO	20	21	CDA

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All pins with respect to V_{cc} . . . . . −20V to +0.3V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

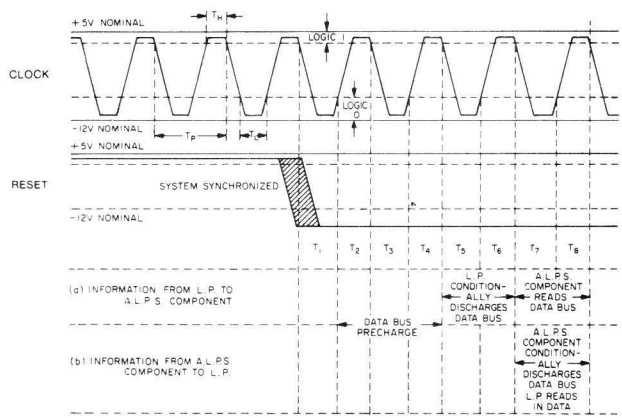
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±0.25V
V_{GI} = GND (substrate at V_{CC})
V_{GG} = −12V ±1V

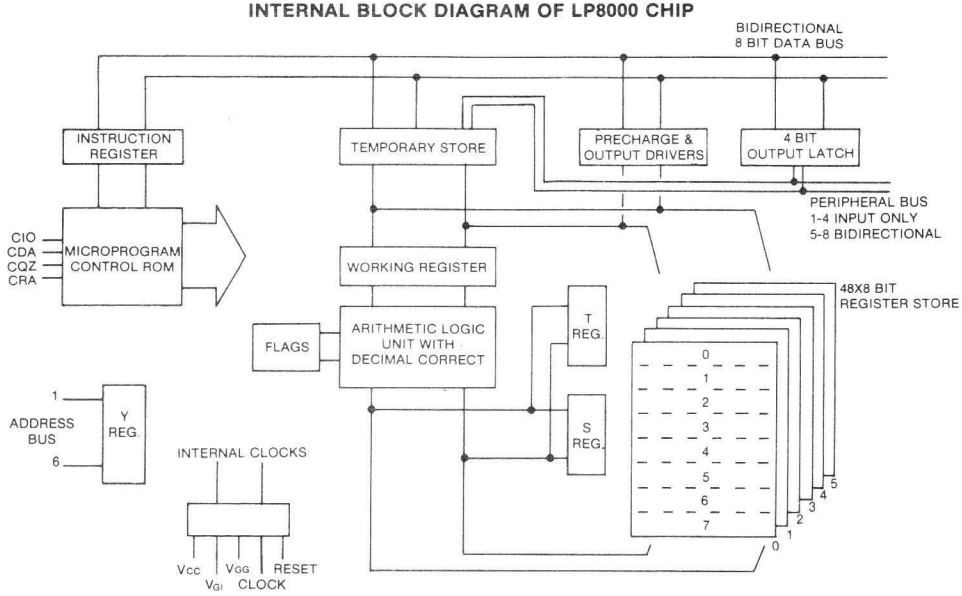
Characteristic	Min	Max	Units	Conditions
Clock Frequency	400	600	kHz	
Machine Cycle Time	6.7	10	µs	
Clock and Reset Input				
Logic '1'	V_{CC} -1.5	—	Volts	
Logic '0'	—	-9.5	Volts	
Data Bus				
Input Conditions				
Logic '1'	V_{cc} -1.5	—	Volts	
Logic '0'	—	+0.8	Volts	
Output Conditions				
Logic '1'	V_{CC} -1.0	—	Volts	Capacitive load
Logic '0'	—	+0.4	Volts	only, maximum 275pF
Control & Address Bus				
Input Conditions				
Logic '0'	V_{CC} -1.5	—	Volts	
Logic '1'	—	+0.8	Volts	
Output Conditions				
Logic '0'	V_{CC} -1.0	—	Volts	Capacitive load
Logic '1'	—	-7.0	Volts	200 pF
Peripheral Bus				
Input Conditions				
Logic '1'	V_{CC} -1.5	—	Volts	
Logic '0'	—	+0.8	Volts	
Output Conditions				
ON Current: LP1010	2	—	mA	$V_{OUT} = V_{CC}$ -1V
Other Devices	1	—	mA	$V_{OUT} = V_{CC}$ -1V
OFF Current: All Devices	—	1	µA	Vin = V_{GG} at 25°C
LP1000 Memory Controls (Address, $\overline{R}$/W, Enable)				
Logic '1'	V_{CC}-1.0	—	Volts	I_{OH} = 100µA
Logic "0"	—	+0.4	Volts	I_{OL} = 0.5mA
Power Consumption: LP 8000	—	1000	mW	
All other devices	—	500	mW	

TIMING DIAGRAMS

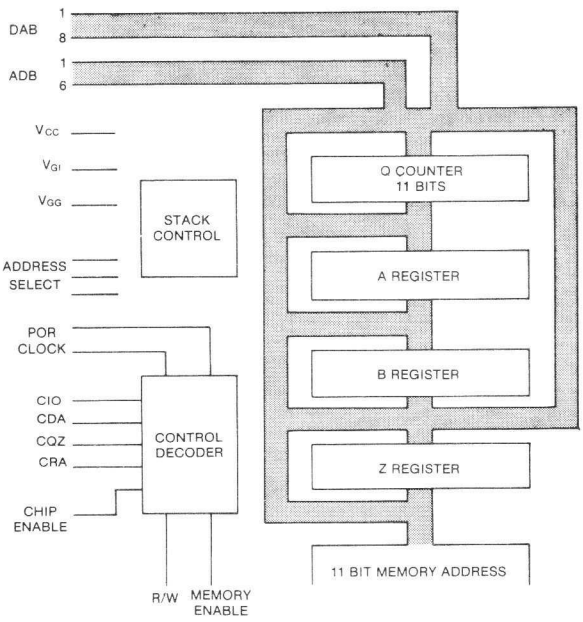


	Mnemonics	Operation	Cycles	Comments
INTERNAL REGISTER INSTRUCTION	LAR	Load Accumulator from Register	1	These instructions are used to manipulate the contents of the accumulator with one of the 48 internal registers. They have a four bit argument and direct addressing is assumed for 0-11 but indirect for 12, 13, and 14. For indirect addressing the register address is held in S,T. Argument 12 gives register pointed to by S & T; 13 gives the same then S is decremented. 14 also addresses via S & T and then S is incremented.
	SAR	Store Accumulator in Register	1	
	DEC	Decrement Register by one *	1	
	ADR	BCD Add Accumulator with Register *	2	
	BAD	Binary Add Accumulator with Register	1	
	AND	Logical AND Accumulator with Register	1	
	EOR	Exclusive OR Accumulator with Register	1	
		*The results of these operations are stored in the respective register. The result of all other operations is stored in the accumulator.		
REGISTERS S&T	LSS	Load S with Short (3-bit) Literal	1	
	LST	Load T with Short (3-bit) Literal	1	
	SAT	Store Accumulator in Register T	1	Lower order bits (1-3) of accumulator are copied in register T.
	SST	Store Accumulator in Registers S & T	1	Bits (1-3) of accumulator copied in register S, bits (4-6) copied in register T.
EXTERNAL REFERENCE INSTRUCTIONS	LAL	Load Accumulator with 8-bit Literal	2	
	LAS	Load Accumulator with 4-bit Literal	1	
	ALL	Logical AND, Accumulator with 8-bit Literal	2	
	ORL	Logical OR, Accumulator with 8-bit Literal	2	
	EOL	Exclusive OR, Accumulator with 8-bit Literal	2	
	ALA	Add Accumulator with 8-bit Literal	2	
	CMP	Compare Accumulator with 8-bit Literal	2	
	LIX	Load Accumulator Indirect Module X	4	The lower six bits of the X and Y registers are used to address 256-bit modules of data and program respectively. The 8-bit data bus is used to provide the intra-module address. These three instructions respectively fetch or store data using the address in the register to specify the module.
	LIY	Load Accumulator Indirect Module Y	4	
	SIX	Store Accumulator Indirect Module X	3	
SIMULATOR & ADDRESS CONTROL REGISTERS	SAX	Store Accumulator in Register X	1	Used in normal register operation and also for setting up module addresses for program and data manipulation.
	SAY	Store Accumulator in Register Y	1	
	LAX	Load Accumulator from Register X	1	
	LAY	Load Accumulator from Register Y	1	
	SZX	Store Accumulator in Z Register Module X	3	Used to set Q Counter or Z register of required module.
	SZY	Store Accumulator in Z Register Module Y	3	
	SQX	Store Accumulator in Q Counter Module X	3	The Y register points to the active program module, the X register points to an alternative module or a data space.
	SQY	Store Accumulator in Q Counter Module Y	3	
	SAV	Store Accumulator in Register V	1	These four instructions allow direct access to the internal registers which are masked by the operand code used for indirect addressing i.e. 12, 13,
	SAW	Store Accumulator in Register W	1	
	LAV	Load Accumulator in Register V	1	
	LAW	Load Accumulator in Register W	1	
	CLA	Clear Accumulator to Zeros	1	
SHIFT	LSA	Shift Accumulator Left 1-bit	1	Carry Flag set unconditionally
	RSA	Shift Accumulator Right 1-bit	1	Carry Flag cleared unconditionally
	LSN	Shift Accumulator Left 4-bits	1	
	RSN	Shift Accumulator Right 4-bits	1	
INPUT/OUTPUT INSTRUCTIONS	LAM	Load Accumulator from Module Direct	2	The indirect I/O operations use the X register for module addressing. The SAX instruction is used to set up the system for the indirect mode.
	SAM	Store Accumulator in Module Direct	3	
	LIM	Load Accumulator from Module Indirect	4	
	SIM	Store Accumulator in Module Indirect	3	
JUMP WITHIN 2K PAGE	JMP	Jump Unconditional	3	
	JIZ	Jump if all Zeros	3/2	3 if true, 2 if false
	JNZ	Jump if not all zeros	3/2	
	JIP	Jump if sign bit positive	3/2	
	JRS	Jump if Register S not equal to seven	3/2	Used to sequence through a 'page' of internal registers.
	JCS	Jump if carry bit set	3/2	
	JCN	Jump if carry bit not set	3/2	
SUBROUTINE INSTRUCTIONS	GOS	Go to Subroutine	3	Program counter automatically stored in memory chip stack.
	RET	Return from Subroutine	2	

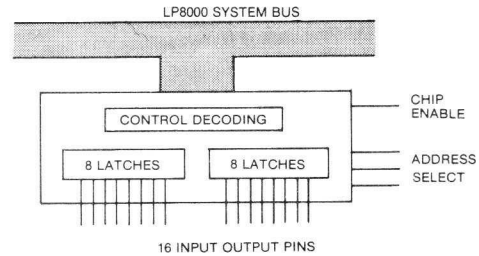
INTERNAL BLOCK DIAGRAM OF LP8000 CHIP



LP1000 MEMORY INTERFACE CHIP



LP1010 INPUT/OUTPUT BUFFER



(Open Drain Configuration
TTL Compatible with Pull
Down Resistors)

DEVELOPMENT FAMILY

A production system may consist of only a Logic Processor, LP8000, and ROM, LP6000, (plus Clock Generator, LP1030). However, the practical development family which complements the LP8000 allows the user to implement his hardware and software in a real time replacement mode for his final mask programmed product. LP1000 and LP1010 parts, plus PROM, can directly replace the LP6000 ROM. Indeed the development family may well be used as the complete solution for short run multi-variety systems.

DEVELOPMENT SUPPORT

Circuits

LP 8000 systems use only a small number of integrated circuits for cost effective implementation. For development and pre-production LP 1000 (Memory Interface Circuit) and LP 1010 (Input-Output Buffer) can be used with PROM, EAROM or RAM to replace the final mask-programmed ROM (see diagram). The system using PROM or EAROM behaves identically with the final mask-programmed ROM version. When the program has been proved, the LP1000, LP1010, and PROM/EAROM can all be replaced by LP 6000 to give the final low-cost system using perhaps as few as two 40 lead DIPs (LP 8000 + LP 6000), and one 8 lead DIP (LP 1030). Small production runs, or systems needing extensive RAM memory can remain with LP 1000 and LP 1010.

Prototype System

To simplify hardware and software development and help speed the users product design cycle time, a complete hardware prototype development system is available to support the Series 8000 family. The GIC 8000 Microcomputer System provides a test bed for user designed interfaces and related hardware as well as a program preparation facility with resident, on-line hardware and software debug aids. The users program can be tested and modified under real time operating conditions. To make program development fast and efficient, peripheral interfaces and their related software including TTY high speed reader, high speed punch and serial line printer are included on the prototype system. In addition, all of the card level modules of this system, ranging from complete microcomputers to memory or I/O modules, are available on an OEM basis for further system integration.

Software

For pure program development to check the flow of instructions, a complete assembler and simulator written in FORTRAN IV is available for operation on minicomputer systems or on internal or external time share networks.

Manual

A manual describing complete hardware aspects of Series 8000, and details of the program preparation software is available from all General Instrument Microelectronics Sales Offices, Agencies, and Distributors.

Series 8000 Cross Assembler — Program Specification

INTRODUCTION

The Symbolic Cross Assembler is capable of converting programs written in Series 8000 symbolic assembly language into a tape format suitable for loading into the prototyping system. The program runs on a General Instrument GIMINI prototyping system with 8K of 16 bit RAM memory using either a teletype or reader/punch for input/output operations. The symbolic assembly language used by this cross-assembler is an extension of the original specification and closely resembles the language format of the Series 1600 Assembler.

FEATURES

The Symbolic Cross Assembler provides the following major features:

- Symbolic language representation of all instructions and data.
- Up to 250 user defined names for variables/registers.
- Binary, octal, decimal, hex and character representations for literals.
- Arithmetic evaluation of operand expressions.
- Assembly directives for
  - — Controlling memory allocation
  - — Defining character strings
  - — Specifying input/output options
  - — Establishing and controlling conditional assemblies.
- Program listings - which are optional.
- Comprehensive error detection and diagnostics.

OPERATION

The Symbolic Cross Assembler converts symbolic source programs into machine code format in a two pass process. During the first pass through the source file, all user specified symbols are placed in a symbol table containing the symbol, its value, and several other attributes. During the second pass through the source file, symbolic instruction mnemonics are translated, symbol references resolved, errors diagnosed, a machine code file generated, and an optional program listing produced.

The machine code file produced by the Cross Assembler is an absolute load module that can be punched on paper tape for subsequent loading in a GIC8000 microcomputer system by the resident loader. Both standard and modified hexadecimal codes can be generated.

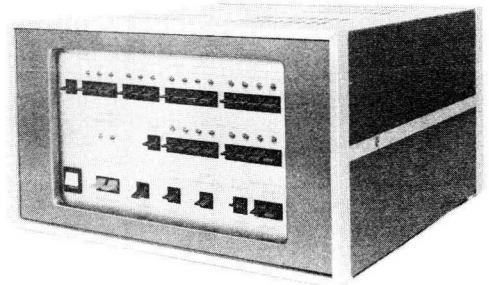
GIC8000

8-Bit Microcomputer System

FEATURES

- Built around the General Instrument LP8000 Microprocessor
- Complete microcomputer system to enable rapid program development
- Up to 16K × 8 of memory space
- PROM resident system monitor
- Load and dump routines for Teletype, Reader, Punch, V.D.U. and Line Printer
- Examine/Store all 48 internal CPU registers, user memory locations and user I/O ports
- Auto increment for examining and storing in sequential locations.
- 'Breakpoint' facility for halting execution of user program at specified address
- 'Start from address' facility for starting execution of user program at any specified address
- Up to 6K × 8 of user RAM or PROM memory
- Up to 15 8-bit user I/O ports
- 8-bit data and 14-bit address displays
- Internal power supplies

GIC8000 MICROCOMPUTER



DESCRIPTION

The GIC8000 Microcomputer System is a complete development system designed to support the General Instrument Series 8000 family. It provides a test bed for user designed interfaces and related hardware as well as a program preparation facility with resident, on-line hardware and software de-bug aids. It also allows the user program to be tested and modified under real time operating conditions. To make program development fast and efficient, peripheral interfaces and their related software including TTY, high speed reader, high speed punch and serial line printer are included. In addition all the cards of the system, ranging from complete microcomputers to memory or I/O modules are available on an OEM basis for further system integration.

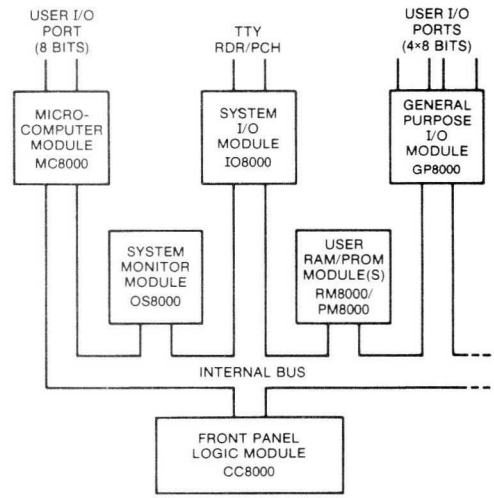
The GIC8000 is of modular design, the basic hardware consisting of a steel cabinet, 12 position card file, front panel control console, power supply and 5 plug-in cards:

MC8000 MICROCOMPUTER MODULE (INCLUDING USER IOB)
OS8000 SYSTEM MONITOR MODULE
IO8000 TTY/RDR-PCH MODULE
RM8000 2K × 8 USER RAM MODULE
CC8000 FRONT PANEL DRIVER MODULE

In addition, the following modules are also available:

GP8000 GENERAL PURPOSE I/O MODULE
EX8000 EXTENDER CARD
PM8000 2K × 8 USER PROM MODULE

BLOCK DIAGRAM



OPERATING MODES

The machine can operate in either SYSTEM or USER mode. In SYSTEM mode, the PROM resident System Monitor program controls all the operational features of the machine and provides a wide range of monitoring and editing facilities which can be used to rapidly develop user programs. In USER mode, the machine is under the exclusive control of the user program and can therefore be used as a test bed for user defined interfaces and related hardware as well as testing the program itself.

OPERATIONAL FACILITIES

Load and Dump Tapes

Load and dump routines allow user program tapes to be read and dumped from a standard teletype, teletype compatible V.D.U., high speed reader, high speed punch or serial line printer. Ready and fault lamps on the front panel indicate the status of the machine during these operations. In dump mode, the whole or only certain specified areas of user memory can be punched out.

Examine Memory, I/O Modules and CPU Registers

The user area of memory (up to 6K × 8), all user I/O modules and all 48 internal CPU registers can be examined from the front panel. A 14 bit address register and an 8 bit data register are used to set and display address and data information respectively. To allow sequential locations to be rapidly examined, a special increment key has also been provided.

Start Execution at Specified Address

Normally, execution of the user program starts from line zero. However in certain circumstances this may not be convenient and so a start from address facility has been incorporated. This allows the user to start execution of his program at any specified address in it and is controlled by a special key on the front panel.

Store In Memory, I/O Modules and CPU Registers

Data can also be written into user memory, user I/O modules and CPU registers via the same address and data registers. Again, the auto increment facility is available to rapidly store data in sequential locations.

Stop Execution at Specified Address

Execution of the user program can be stopped by operating MASTER RESET to return control of the machine to the System Monitor Program. However as it is not possible to define exactly where execution ceases using this method, a 'Breakpoint' facility has been provided. This allows the user to execute his program up to a specified point and then automatically switch into Monitor mode where the full range of monitoring and editing facilities can be used.

USER MEMORY MODULES

The total memory area of 16K is divided into 8 pages of 2K and each page is further sub-divided into 8 modules of 256 words. The bottom three pages, 0, 1 and 2, are available to the user and can consist of up to 3, plug-in static RAM or UV Erasable PROM cards or any combination of the two. To prevent accidental corruption of the RAM modules during development, each card is provided with a Memory Freeze switch which effectively converts them to volatile ROM memory. One 2K × 8 RAM module is normally supplied with the basic kit.

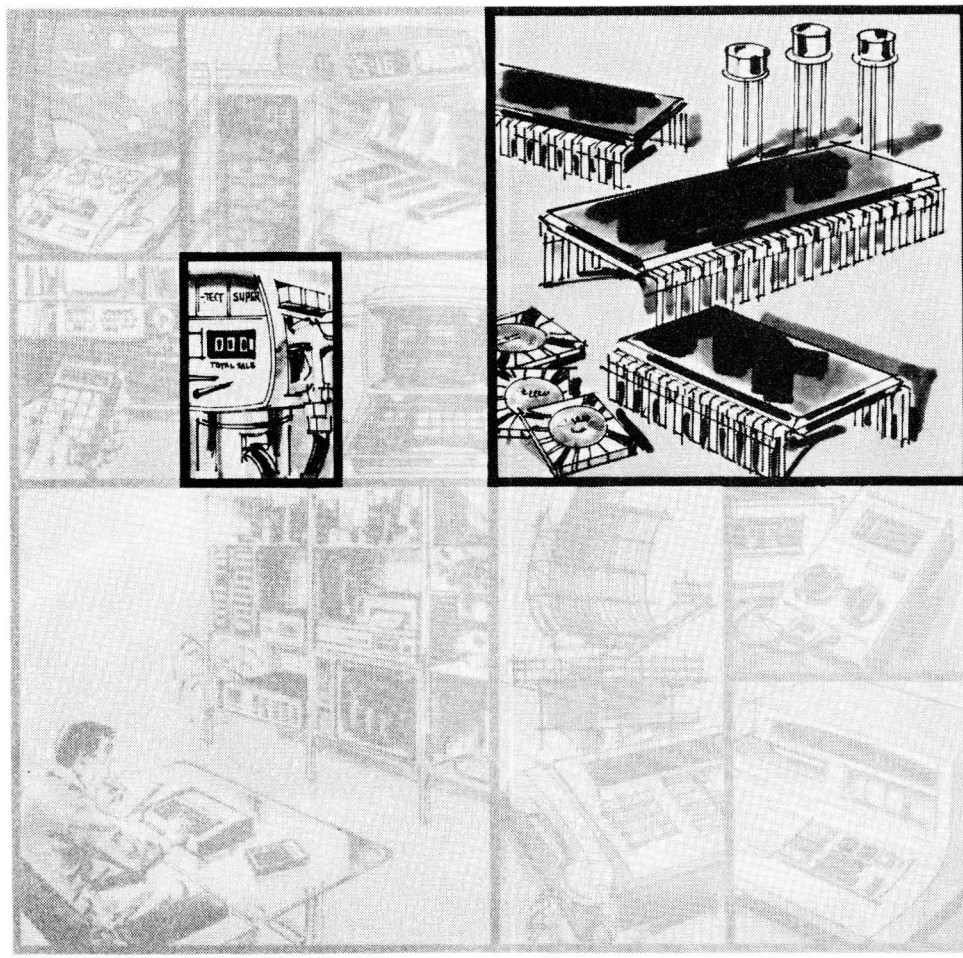
USER I/O MODULES

The top 15 modules in memory are allocated for user as user I/O ports. Each port is 8 bits wide and occupies one module address. The microcomputer module has two IOB's, one of which is used by the LP8000 microcomputer chip but the other is available to the user. If the user requires additional I/O ports, then General Purpose I/O Modules can be added as necessary.

Each General Purpose I/O Module supports two, dual 8 bit IOB's giving the user four, individually addressable 8 bit I/O ports, i.e. 32 bi-directional lines. Pull-down resistors fitted on the card make the I/O lines TTL compatible (one load). In addition up to eight 16 pin DIL packages can be added to the cards for user designed circuitry. All I/O lines enter the machine via sockets on the rear panel.

MICROCOMPUTER 3

PIC Series 3- 3
SBA Series 3-29



MICRO ELECTRONICS

PIC SERIES MICROCOMPUTER

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
LSI CIRCUITS			
8 BIT SINGLE CHIP MICRO-COMPUTER	The PIC 1650 series of single chip microcomputers contain RAM, I/O, and a central processing unit as well as a customer defined ROM to specify the overall functional characteristics of the device.	**PIC 1650**	**3-4**
		PIC 1645	**3-13**
		PIC 1655	**3-14**
		PIC 1670	**3-15**
SINGLE CHIP DEVELOPMENT MICRO-COMPUTER	PIC 1650 microcomputer without ROM and with the addition of a HALT pin.	**PIC 1664**	**3-16**
HARDWARE			
PIC DEVELOPMENT SYSTEM	Contains a pre-programmed PIC 1650, a PIC 1664, 512 x 12 RAM, a TTY interface, and a cabled 40 pin DIP plug.	**DB1650**	**3-19**
PIC FIELD DEMO SYSTEM	Contains a PIC 1664 and sockets for external PROMs. Provision for an on-board RC oscillator or external clock.	**FD1664**	**3-20**
SOFTWARE			
PIC ASSEMBLER	Converts symbolic source programs for the PIC 1650 into suitable code.	**PICAL**	**3-21**
PIC SIMULATOR	Simulates all PIC instructions for program debug and verification.	**PICSIM**	**3-24**

Single Chip Microcomputer

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit Registers
- 512 × 12-Bit ROM for Program
- Arithmetic Logic Unit
- 4 Sets of 8 User Defined TTL-compatible Input/Output Lines.
- Real Time Clock Counter
- Self contained Oscillator
- Access to RAM Registers inherent in instruction.
- Single +5V power supply

DESCRIPTION

The PIC1650 is an MOS/LSI circuit array containing RAM, I/O, and a central processing unit as well as a customer defined ROM on a single chip. This combination produces a low cost solution for cost sensitive applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning and display driving can be done at the same time due to the power of the 8 bit ALU.

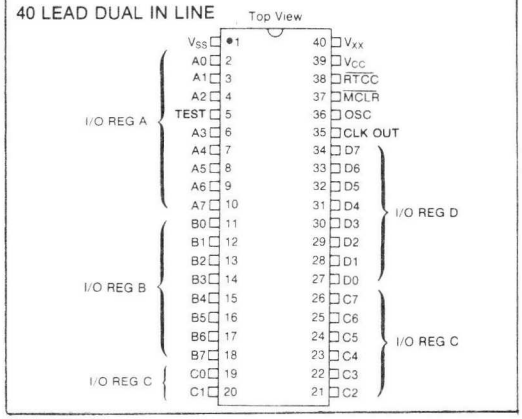
The internal ROM contains a customer defined program using the PIC1650's powerful instruction set to specify the overall functional characteristics of the device. The four 8-bit input/output registers provide 32 latched lines for interfacing to a limitless variety of applications. The PIC1650 can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, gasoline pumps, consumer appliances, industrial timing and control applications. The 12 bit instruction word format provides a powerful yet easy to use instruction repetoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1650 is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and Production history. Only a single +5 volt power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external R/C network to establish the frequency. Inputs and outputs are TTL compatible. The PIC1650 is supplied in a 40-pin dual-in-line package.

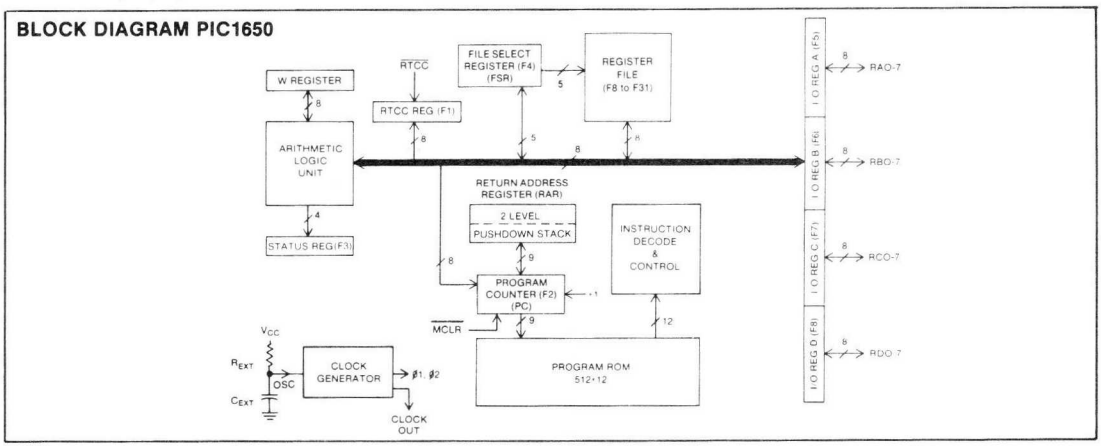
Extensive hardware and software support is available to aid the user in developing his application program and to verify performance before committing to mask tooling. Application notes and sample programs are used to develop programs which can then be assembled into machine language using PICAL eliminating the burden of coding with ones and zeros. PICAL is provided with the GIMINI microcomputer system and a FORTRAN IV version is available for popular minicomputers as well as larger computers and time sharing systems. Once the application program is developed several options are available to insure proper performance. PICSIM is a software program which simulates the PIC1650's operation. Program errors can be easily detected, corrected, and verified before any hardware implementation is needed. The PIC1650's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is identical to the PIC1650 except the ROM is removed and additional pins are added to connect external PROM or RAM. The FD1664 Field Demo Module is available containing a PIC1664 with sockets for standard or UV erasable PROM. Finally the DB1650 PIC Development System provides the user with complete hardware verification of the PIC1650 in its application combined with easy program debugging and changing because the users program is stored in RAM. With these development tools the user can quickly and confidently order the masking of the PIC1650's ROM and bring his application into the market.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM PIC1650



PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external R/C network can be used to set the frequency of operation of the internal clock generator. The maximum oscillator frequency is 1MHz.
$\overline{\text{RTCC}}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The maximum $\overline{\text{RTCC}}$ frequency is 250kHz. This register can be loaded and read by the program.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{\text{MCLR}}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O registers high. Should be held low at least 20μs past the time when the power supply is valid.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1650 microcomputer is based on a register file concept with very simple, low level, commands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC1650 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user defined Control ROM composed of 512 program words each 12 bits in width.

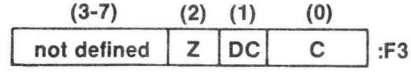
The Register File is divided into two functional groups: operational registers and general registers. The operational registers are addressed as F0 to F8 (the first 9 of the total of 32 file registers) and include, among others, the Real Time Clock Counter Register, the Status Register, the Program Counter (PC), and I/O Registers A, B, C and D (RA, RB, RC and RD). The general registers are addressed as F9 to F31 and are used for data and control information under command of the instructions.

The Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Control ROM contains the operational program for the rest of the logic within the controller. Sequencing of a microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, call instructions, or loading computed addresses into the PC. In addition, an on-chip two level pushdown stack is employed with the return address register serving as the top element of the stack. This permits easy to use subroutine nesting. Application of the +5V power supply initializes the ROM microprogram to address 777_8.

REGISTER FILE ARRANGEMENT

File	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0 → W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W. Bits 5-7 are always ones.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. Clock keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{\text{RTCC}}$.
F2	Program Counter (PC). The PC is automatically incremented and can be written into; e.g., MOVWF F2. If cannot be read, however.
F3	Status Word Register. The bits in this register can be set or cleared by the Bit Set and Bit Clear instructions; they cannot be altered by other commands operating on F3.



C (Carry): Stores the carry out on arithmetic operations, and acts as a bit link on rotate operations. This bit is set high on an SUBWF instruction if the addition of f, the one's complement of W, and a 1 results in a carry.

DC (Digit Carry): Stores the carry out of low order digit (4 Ls Bs) on arithmetic operation. This bit is set high on a SUBWF instruction if the addition of f, and the two's complement of W, results in a carry from the low order digit.

Z (Zero): Set if the result of the arithmetic operations is zero.

Bits: 3-7 Reserved for future use. Not defined when read.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits read as a logic "1".
F5	I/O Register A A0-A7
F6	I/O Register B B0-B7
F7	I/O Register C C0-C7
F8	I/O Register D D0-D7
F9-F31	General Purpose Registers

Instruction Set Summary

For an oscillator frequency of 1MHz, the instruction execution time is 4 μsec, except if a conditional test is true or if the PC register is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

In the following PIC instruction descriptions "k" represents an eight bit constant or literal value, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register, if "d" is one, the result is returned to the file register specified in the instruction. If the "d" operand is omitted, the f register is assumed as the destination. "f" and "d" may be numbers, characters, or symbols as described in the PIC Assembler and PIC Simulator instructions. "C" represents the carry bit, "Z" represents the zero bit, and "DC" represents the digit carry bit.

GENERAL FILE REGISTER OPERATIONS

(6)	(1)	(5)
OP CODE	d	f (FILE #)

for d = 0, f→W
d = 1, f→f

Instruction (Octal)				Name	Syntax			Operation	Status
000000	0	00000	(0000)	No Operation	NOP	—	—		—
000000	1	fffff	(0040)	Move W to f *	MOVWF	f		W→f	—
000001	0	fffff	(0100)	Clear W	CLRW	—		O→W	Z
000001	1	fffff	(0140)	Clear f	CLRF	f		O→f	Z
000010	d	fffff	(0200)	Subtract W from f	SUBWF	f, d		f - W→d	C,DC,Z
000011	d	fffff	(0300)	Decrement f	DECF	f, d		f - 1→d	Z
000100	d	fffff	(0400)	Inclusive OR W and f	IORWF	f, d		W∨f→d	Z
000101	d	fffff	(0500)	AND W and f	ANDWF	f, d		W∧f→d	Z
000110	d	fffff	(0600)	Exclusive OR W and f	XORWF	f, d		W∀f→d	Z
000111	d	fffff	(0700)	Add W and f	ADDWF	f, d		W+f→d	C,DC,Z
001000	d	fffff	(1000)	Move f	MOVF	f, d		f→d	Z
001001	d	fffff	(1100)	Complement f	COMF	f, d		$\bar{f}$→d	Z
001010	d	fffff	(1200)	Increment f	INCF	f, d		f+1→d	Z
001011	d	fffff	(1300)	Decrement f, Skip if Zero	DECFSZ	f, d		f - 1→d, skip if Zero	—
001100	d	fffff	(1400)	Rotate Right f	RRF	f, d		f(n)→d(n-1), f(0)→C, C→d(7)	C
001101	d	fffff	(1500)	Rotate Left f	RLF	f, d		f(n)→d(n+1), f(7)→C, C→d(0)	C
001110	d	fffff	(1600)	Swap halves f	SWAPF	f, d		f(0-3)⇄f(4-7)→d	—
001111	d	fffff	(1700)	Increment f, Skip if Zero	INCFSZ	f, d		f+1→d, skip if zero	—

BIT LEVEL FILE REGISTER OPERATIONS

(4)	(3)	(5)
OP CODE	b (BIT #)	f (FILE #)

Instruction (Octal)				Name	Syntax			Operation	Status
0100	bbb	fffff	(2000)	Bit Clear f	BCF	f, b		0→f(b)	—
0101	bbb	fffff	(2400)	Bit Set f	BSF	f, b		1→f(b)	—
0110	bbb	fffff	(3000)	Bit Test f, Skip if Clear	BTFSC	f, b		Bit Test f(b); skip if clear	—
0111	bbb	fffff	(3400)	Bit Test f, Skip if Set	BTFSS	f, b		Bit Test f(b); skip if set	—

LITERAL AND CONTROL OPERATIONS

(4)	(8)
OP CODE	I (LITERAL)

Instruction (Octal)				Name	Syntax			Operation	Status
1000	k k k k k k k k		(4000)	Return	RET	—		0 → W, RAR → PC	—
1000	k k k k k k k k		(4000)	Return and place Literal in W	RETLW	k		k → W, RAR → PC	—
1001	k k k k k k k k		(4400)	Call subroutine *	CALL	k		PC → RAR, k → PC	—
101x	k k k k k k k k		(5X00)**	Go To address	GOTO	k		k → PC	—
1100	k k k k k k k k		(6000)	Move Literal to W	MOVLW	k		k→W	—
1101	k k k k k k k k		(6400)	Inclusive OR Literal and W	IORLW	k		k∨W→W	Z
1110	k k k k k k k k		(7000)	AND Literal and W	ANDLW	k		k∧W→W	Z
1111	k k k k k k k k		(7400)	Exclusive OR Literal and W	XORLW	k		k∀W→W	Z

*The 9th bit of the program counter in the PIC1650 is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in page 0. However, subroutines can be called from page 0 or page 1 since the RAR is 9 bits wide. (Page 0: 0-255. Page 1: 256-511).

**If X = 0, the address is in page 0; if X = 1, the address is in page 1. The PIC assembler takes care of assigning the correct op codes.

OTHER INSTRUCTION MNEMONICS RECOGNIZED BY THE PIC1650 ASSEMBLER

Instruction (Octal)	Name	Syntax	Equivalent Operation(s)	Status
0100 000 00011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
0101 000 00011 (2403)	Set Carry	SETC	BSF 3, 0	—
0100 001 00011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
0101 001 00011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
0100 010 00011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
0101 010 00011 (2503)	Set Zero	SETZ	BSF 3, 2	—
0111 000 00011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
0110 000 00011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
0111 001 00011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
0110 001 00011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
0111 010 00011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
0110 010 00011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001000 1 f f f f f (1040)	Test File	TSTF f	MOVF f, 1	Z
001000 0 f f f f f (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001001 1 f f f f f (1140) 001010 d f f f f f (1200)	Negate File	NEGF, f,d	COMF f, 1 INCF f, d	Z
011000 0 00011 (3003) 001010 d f f f f f (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011000 0 00011 (3003) 000011 d f f f f f (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011000 1 00011 (3043) 001010 d f f f f f (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011000 1 00011 (3043) 000011 d f f f f f (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101× kkkkkkkk (5×00)	Branch	B K	GO TO K	—
0110 00000011 (3003) 101× kkkkkkkk (5×00)	Branch on Carry	BC K	BTFSC 3,0 GO TO K	—
0111 00000011 (3403) 101× kkkkkkkk (5×00)	Branch on No Carry	BNC K	BTFSS 3,0 GO TO K	—
0110 00100011 (3043) 101× kkkkkkkk (5×00)	Branch on Digit Carry	BDC K	BTFSG 3,1 GO TO K	—
0111 00100011 (3443) 101× kkkkkkkk (5×00)	Branch on No Digit Carry	BNDC K	BTFSS 3,1 GO TO K	—
0110 01000011 (3103) 101× kkkkkkkk (5×00)	Branch on Zero	BZ K	BTFSC 3,2 GO TO K	—
0111 01000011 (3503) 101× kkkkkkkk (5×00)	Branch on No Zero	BNZ K	BTFSS 3,2 GO TO K	—

if × = 0, address is in page 0.
if × = 1, address is in page 1.

Sample Programs

In the following program steps, .dddd means literals, in decimal form, otherwise they are in octal form.

I OBJECTIVE: To display the file pointed to by F31 via I/O post A (F5). Assume .20 in F31 and .100 in F20.

Hence, the following program will display .100 via F5.

Program steps	Description
MOVF .31, W	Move the contents of F31 to the working register W. After execution W contains .20.
MOVWF 4	Move the contents of W to FSR (F4). After execution F4 contains .20.
MOVF 0, W	Move the contents of the file pointed to by FSR, that is, the contents of F20, to W. Thus W contains .100 after execution.
MOVWF 5	Move the contents of W to F5. Hence .100 is in F5 now. Note that the transfer to F5 latches the data to the external pins where it is accessible to other circuits in the application.

II OBJECTIVE: To compare F31 to a constant, if equal GOTO OK. if not equal GOTO NO.

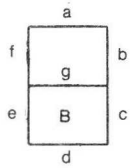
Program Steps	Description
MOVF .31, W	Move the contents of F31 to the working register W
XORLW CONST	Exclusive Oring, bit by bit, the contents of W and the literal CONSTANT. If they are equal, all zero bits will result in W and the second bit in the status register (F3) will be set. Although the SUBWF instruction could be used, the XORLW instruction saves one instruction and does not alter the carry flag.
BTFSS 3,2	If bit 2 in F3 is one, skip the next step. This is the zero status bit.
GO TO NO	They are not equal.
GO TO OK	They are equal.

III OBJECTIVE: To clear files F5 to F31. This program illustrates the use of the File Select. Register (F4) and the indirect addressing mode using F0.

Program Steps	Description
MOVLW 5	Move the literal 5 to the working register W.
MOVWF 4	Move the literal 5 to the File Status Register (F4). These two steps initialize the FSR to 5.
LOOP: CLRF 0	Clear the contents of the file pointed to by the FSR
INCFSZ 4, 1*	Increment the FSR. The PC counter will skip after File 31 is cleared.
GOTO LOOP	Repeat the steps beginning at loop to clear the next file
END	Files F5 to F31 are cleared.

* The upper three bits of the FSR are always read as ones. When the FSR points to F31 (= octal 37) all bits of the FSR are ones. The INCFSZ 4 instructions reads this value into the ALU, increments it, the result of the increment equals zero causing a skip. If the FSR is read after this operation, however, the result will be 340_8.

IV OBJECTIVE: Convert a BCD held in the 4 LSBs of F20 (the 4 MSBs are assumed zero) to a 7-Segment Code. The 7-Segment Code is output via I/O port F5 which is directly tied thru current limiting resistors to a 7-Segment LED display. This program illustrates the use of a computed GOTO instruction.

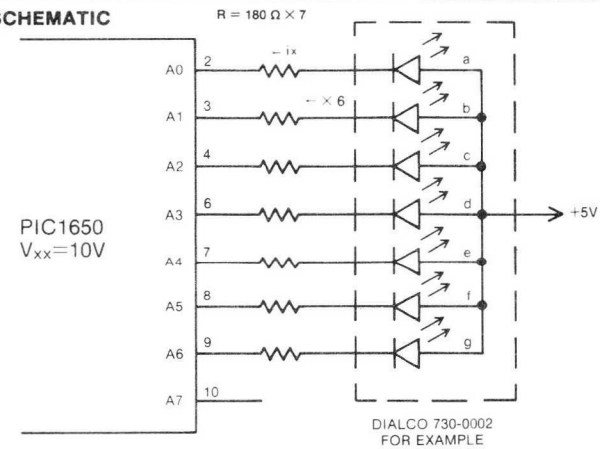


Typical 7-Segment bar position. The PIC assembler recognizes the format B'bbbbbbbb' as an eight-bit binary data word where b is 0 or 1. The LED bar positions are thus B'0abcdefg'.

	Program Steps			Description
	MOVLW	TBLSTR	;	Starting address of table
	ADDWF	20, W	;	Add BCD number as offset to Tablestart
	CALL	CONVRT	;	Call the conversion subroutine. The program counter executes the next instruction at CONVRT.
	MOVWF	5	;	Output the 7-segment code via I/O port F5. The 7-segment display will now show the BCD number and this output will remain stable until F5 is set to a new value.
	END			
CONVRT:	MOVWF	2	;	MOVE the compute address into PC. This is a computed GOTO. Because the ninth bit of PC is set to zero by a MOVWF 2 the TBLSTR routine must be located in the page 0.
TBLSTR:	RETLW	B'00000001	;	complement of 0 in 7-segment code
	RETLW	B'01001111	;	complement of 1 in 7-segment code
	RETLW	B'00010010	;	complement of 2 in 7-segment code
	RETLW	B'00000110	;	complement of 3 in 7-segment code
	RETLW	B'01001100	;	complement of 4 in 7-segment code
	RETLW	B'00100100	;	complement of 5 in 7-segment code
	RETLW	B'01100000	;	complement of 6 in 7-segment code
	RETLW	B'00001111	;	complement of 7 in 7-segment code
	RETLW	B'00000000	;	complement of 8 in 7-segment code
	RETLW	B'00001100	;	complement of 9 in 7-segment code

NOTE: The RETLW instruction loads the W register with the specified literal value and returns to the instruction following the CALL instruction (MOVWF 5). The complement of the 7-segment code is used because the LED display unit is common anode thus a bar is activated when the output is set low. This is used to make use of the large current sinking capabilities of the PIC1650.

OUTPUT SCHEMATIC

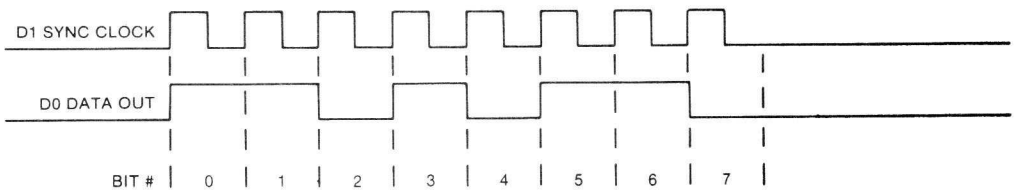


NOTES:
V_{xx} = 10V
V_{CL} = 1.0V and diode drop = 1.8V
5V = 1.0V + 1.8V + 180Ω I_X
I_X = 12.2mA (See LED direct drive in electrical specifications)

V OBJECTIVE: Serially output the 8 bits in register F20 via I/O line D0 (pin 27). I/O line D1 (pin 28) is used to synchronize the output using the rising edge.

	Program Steps		Description
	MOVLW .8	;	LOAD the decimal 8 into W
	MOVWF 9	;	Put decimal 8 into F9
LOOP	BCF 8, 1	;	Clear the sync output
	RRF 20, 1	;	Rotate F20 one bit right. Bit 0 to carry
	BTFSS 3, 0	;	Test carry, skip if set
	GOTO A	;	Carry clear, go to A
	BSF 8, 0	;	Carry set, set D0
	GOTO B	;	Go to B
A:	BCF 8, 0	;	Carry clear, clear D0
B:	BSF 8, 1	;	Raise sync line
	DECFSZ 9	;	Have output all eight bits?
	GOTO LOOP	;	No, output next bit
	BCF 8, 1	;	Yes, clear sync output
	END		

If File Register F20 contains 153 (octal) then the output will be as follows:



VI OBJECTIVE: Generate a 3 ms pulse on I/O line C5 (pin 24).

	Program Steps		Description
	MOVLW .250	;	LOAD decimal 250 into W
	MOVWF 9	;	Transfer 250 to F9
	BSF 7, 5	;	Set C5 high
A:	DECFSZ 9, 1	;	Decrement F9 skip if zero
	GOTO A	;	This GOTO instruction will cause F9
		;	to be decremented 250 times. The
		;	decrement executes in 4μsec while the
		;	GOTO takes 8μsec. Therefore the
		;	loop executes in (4+8) μsec $\times$ 250 = 3 ms.
	BCF 7, 5	;	terminate pulse on C5.

NOTE: For precise timing generation an external crystal oscillator must be used. Otherwise the actual timing is dependent on the tolerances of the external RC components.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C
V_{CC}, V_{XX}, and all other input/output voltages with respect to V_{SS} ..... −0.3V to +12.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

STANDARD CONDITIONS (unless otherwise noted)

V_{CC}: +5V ± 5%
V_{XX}: +4.75V to 10.0V

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Power Supply Currents	I_{CC}	—	35	60	mA	
	I_{XX}	—	1	5	mA	
Logic Inputs						
Low	V_{IL}	0	—	.65	V	
High	V_{IH}	2.4	—	V_{CC}	V	
Logic Outputs						
Low	V_{OL}	—	0.4	0.5	V	V_{XX}=5V @ I_{OL}=1.6mA
High	V_{OH}	2.4	—	V_{CC}	V	I_{OH}=100μA min.
AC CHARACTERISTICS						
OSC Frequency	f_{IN}	.2	—	1	MHz	
RTCC Frequency	—	DC	—	250	kHz	
CLKOUT Frequency	—	.25 fin	—	—	—	
CLK OUT						
Rise Time	t_r	—	—	200	ns	1 TTL load and 100 pF
Fall Time	t_f	—	—	200	ns	
I/O Registers A, B, C, D						
Output Mode:						
Delay From CLKOUT	t_{DD}	—	—	500	ns	1 TTL load and 100 pF
Input Mode						
Set-Up	t_{IS}	0	—	—	ns	
hold	t_{IH}	100	—	—	ns	

**Typical values are at +25°C and nominal voltages.

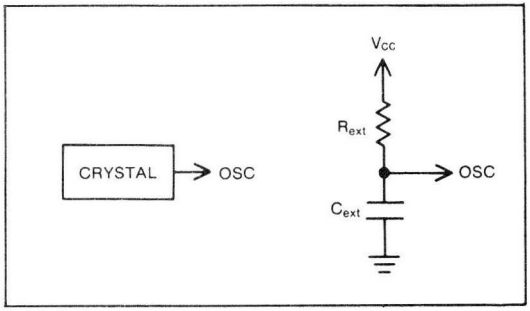
LED Direct Drive

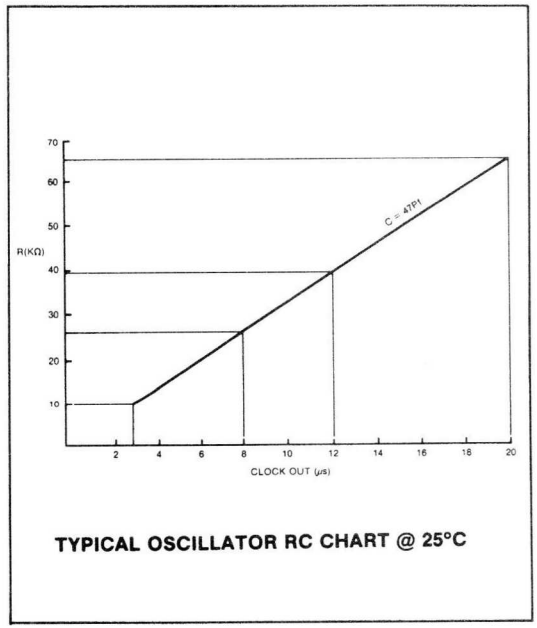
V_{XX} drives the gate of the output buffer, allowing adjustment of LED drive capability:

V_{XX}	V_{OUT}	I_{SINK} (typ.)
5V	0.4V	2.5mA
5V	0.7V	4.2mA
10V	0.4V	5.8mA
10V	0.7V	10.0mA
10V	1.0V	14.1mA

OSCILLATOR INPUT

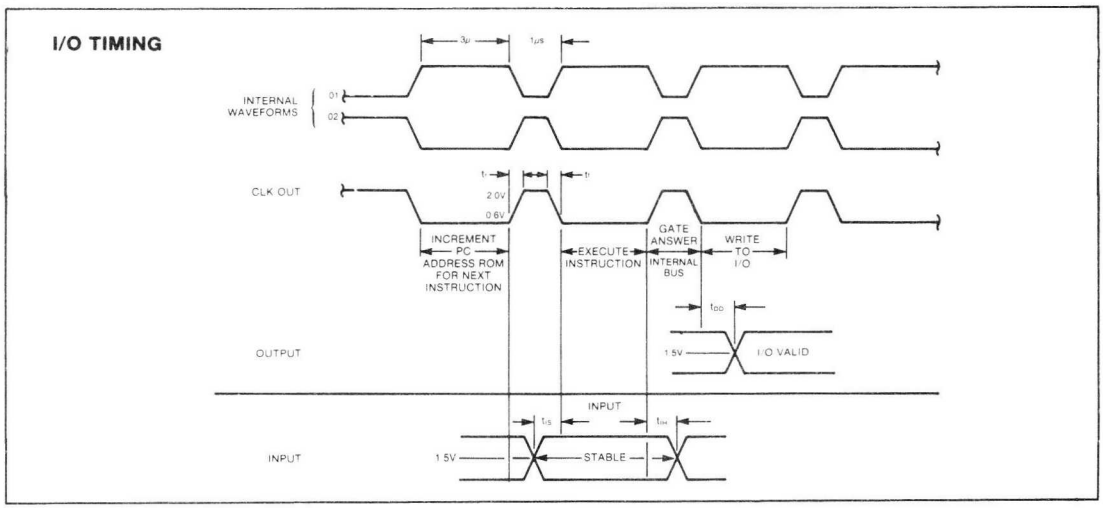
The oscillator input (OSC) can be driven directly by a crystal with compatible output or by an external RC network.





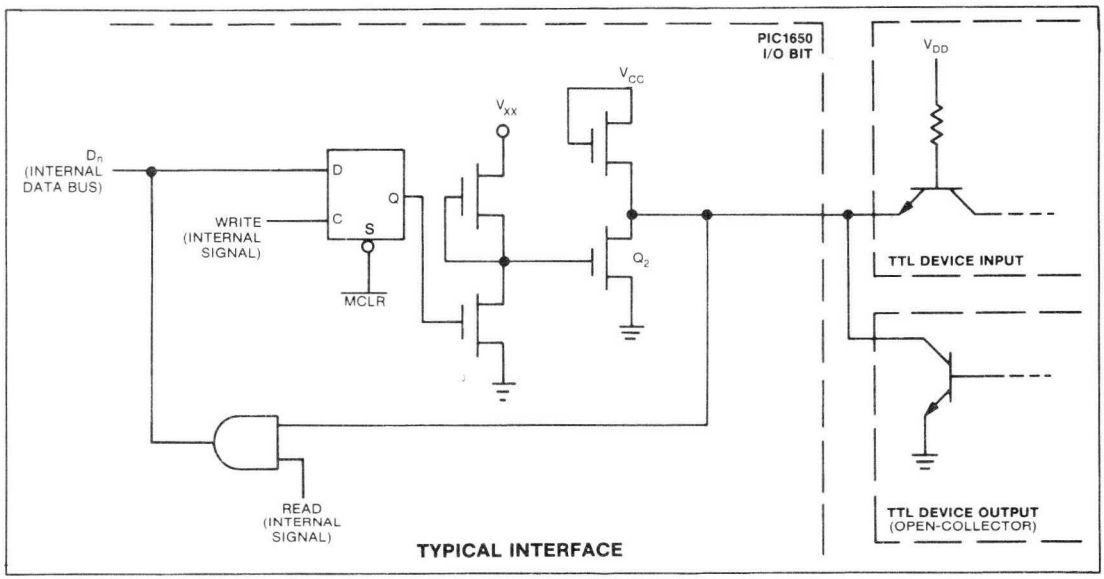
TYPICAL OSCILLATOR RC CHART @ 25°C

MICRO-COMPUTER



I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (CPU chip is outputting) or the output of an open collector TTL device (CPU chip is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a logic "1" level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source 200μA typical.



External Flag (Interrupt) Handling

By using the BTFSC and BTFSS instruction the I/O lines of the PIC1650 are easily used as vectored interrupt flags. If the design calls for I/O register D bits 0 to 3 to be interrupt flags with bit 0 having the highest priority then the general interrupt scanning code might be as follows (interrupts are active low):

```
SCAN    BTFSS 8, 0      ;  Skip if Reg. D bit 0 is set
        GOTO INT1       ;  Go to Interrupt 1
        BTFSS 8, 1      ;  Skip if Reg. D bit 1 is set
        GOTO INT2       ;  Go to Interrupt 2
        BTFSS 8, 2      ;  Skip if Reg. D bit 2 is set
        GOTO INT3       ;  Go to interrupt 3
        BTFSS 8, 3      ;  Skip if Reg. D bit 3 is set
        GOTO INT4       ;  Go to interrupt 4
        END             ;  No interrupts. Also return point
                        ;  for all interrupt routines.
```

PRELIMINARY INFORMATION

Single Chip Microcomputer

FEATURES

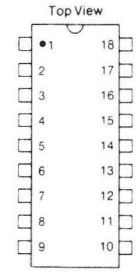
- Same architecture and instruction set as the PIC 1650
- 4 dedicated inputs, 4 dedicated outputs, 4 bi-directional I/O lines
- 24 8-bit registers
- 256×12 ROM for program
- Low current operation 30 mA I_{CC}
- 2μs instruction cycle time.

DESCRIPTION

The PIC 1645 is a single chip microcomputer designed for applications with a maximum of 12 I/O lines. The PIC 1645 maintains the same powerful instructions as the PIC 1650 with the additional features of interrupts and programmable prescaling of the event counter.

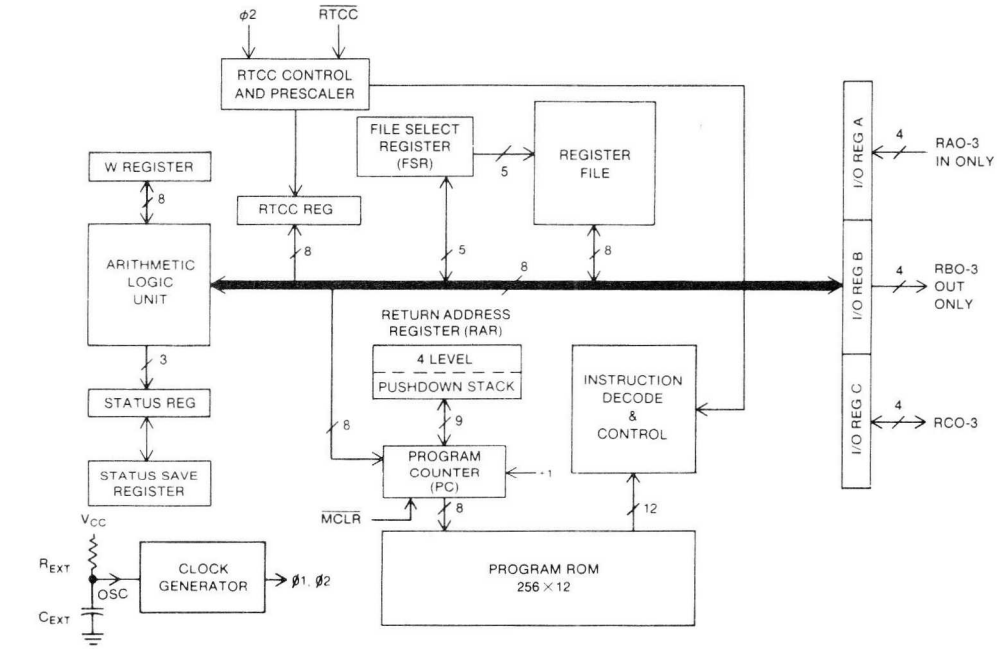
PIN CONFIGURATION

18 LEAD DUAL IN LINE



Not yet defined.

BLOCK DIAGRAM



Single Chip Microcomputer

FEATURES

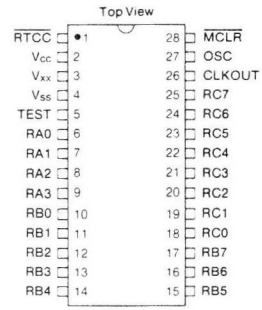
- Same architecture and instruction set as the PIC1650
- 4 dedicated inputs, 8 dedicated outputs, 8 bi-directional I/O lines
- 32 8-bit registers
- 512×12 bit ROM for program

DESCRIPTION

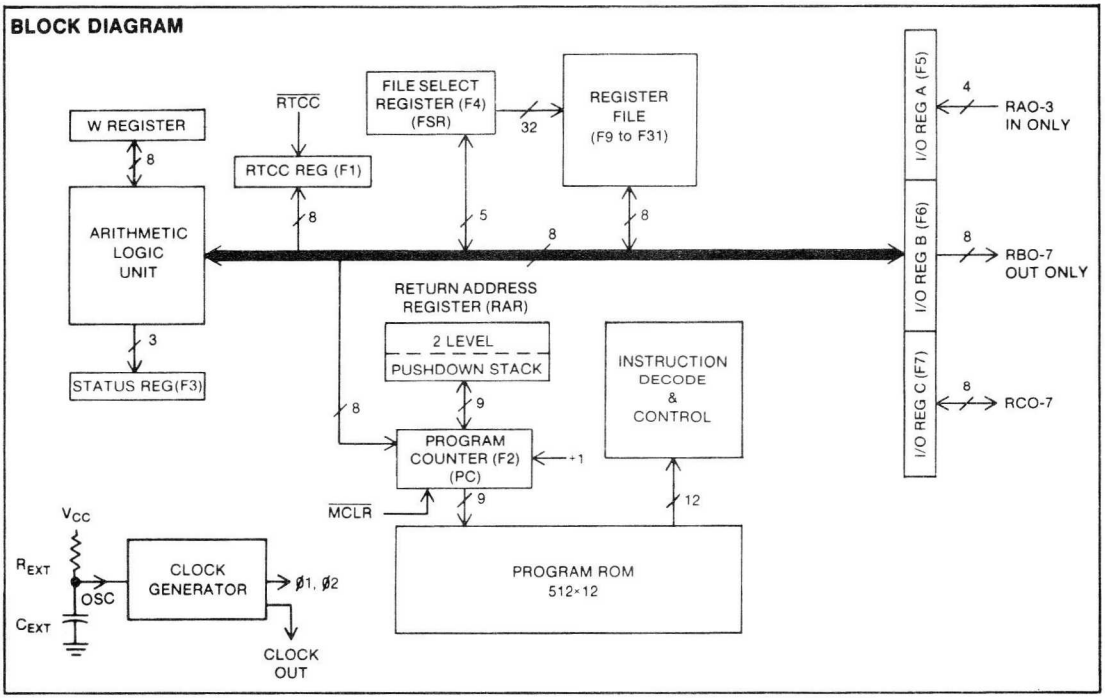
The PIC1655 is an MOS/LSI circuit array with all the architectural features of the PIC1650 but designed for those applications requiring only 20 I/O lines rather than the 32 lines of the PIC1650. The PIC1655 includes all the powerful instructions of the PIC1650 as well as the same electrical and timing characteristics. The 20 I/O lines are organized as two 8-bit registers and the 4 LSBs of a third register.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



Single Chip Microcomputer

FEATURES

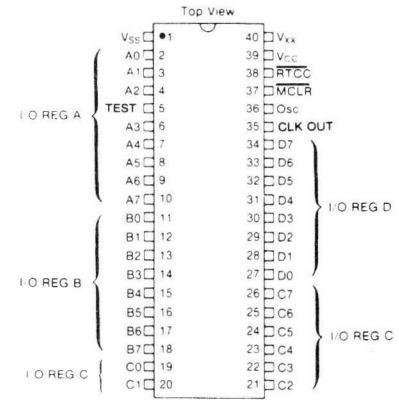
- Same architecture and instruction set as the PIC1650.
- 32 user defined TTL compatible I/O lines.
- 1024×12 bit ROM for program
- 4 level stack area for subroutine nesting.

DESCRIPTION

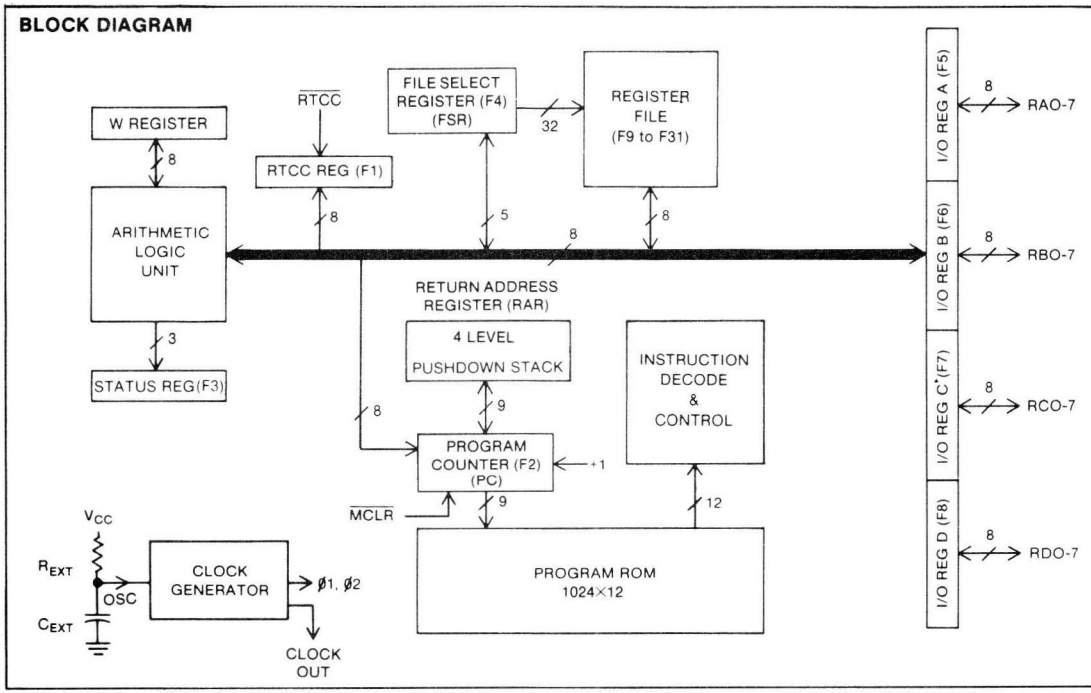
The PIC1670 is an MOS/LSI circuit array with all the architectural features of the PIC1650 but designed for those applications requiring up to 1024 words of program storage. The PIC1670 is pin compatible with the PIC1650 allowing easy upgrading of existing applications using the PIC1650. The electrical and timing characteristics of the PIC1650 are also the same as the PIC1670. To handle the complete programming needs of PIC1670 applications, the subroutine stack area has been expanded to four levels.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



Single Chip Development Microcomputer

FEATURES

- PIC1650 microcomputer with ROM removed
- Useful for engineering prototyping and field trial demonstrations
- PIC1650's ROM address & data lines brought out to pins
- PIC1650's ROM can be replaced by external RAM or PROM
- PIC1650 can be single stepped or stopped via the halt pin
- Fully TTL compatible

DESCRIPTION

The PIC1664 MOS/LSI circuit array is exactly the same as the PIC1650 except for the fact that the ROM is removed and that the ROM address and data lines are brought out, resulting in a 64 pin package. The addition of a halt pin has also been made to the 64 pin package. This pin gives the user the ability to stop as well as single-step the chip. The PIC1664 is designed as a useful tool for engineering prototyping and field trial demonstration.

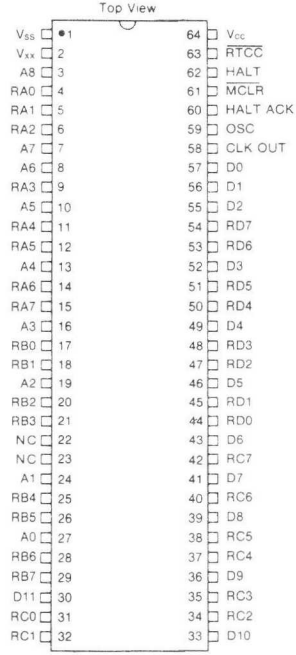
INSTRUCTION SET

The PIC1664 instruction set is exactly identical to the PIC1650. In addition the PIC1664 contains a HALT instruction (Octal code = 0001).

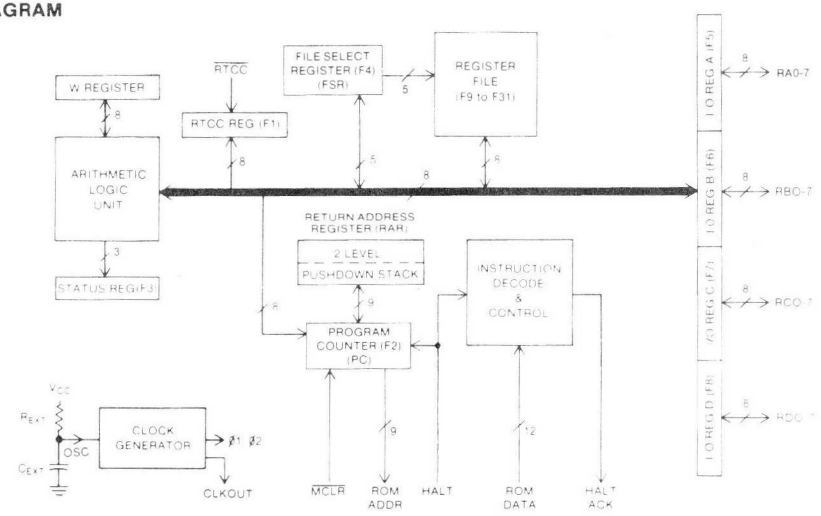
PIN CONFIGURATION

64 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C
V_{CC}, V_{XX}, and all other input/output voltages with respect to V_{SS} ..... −0.3V to +12.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

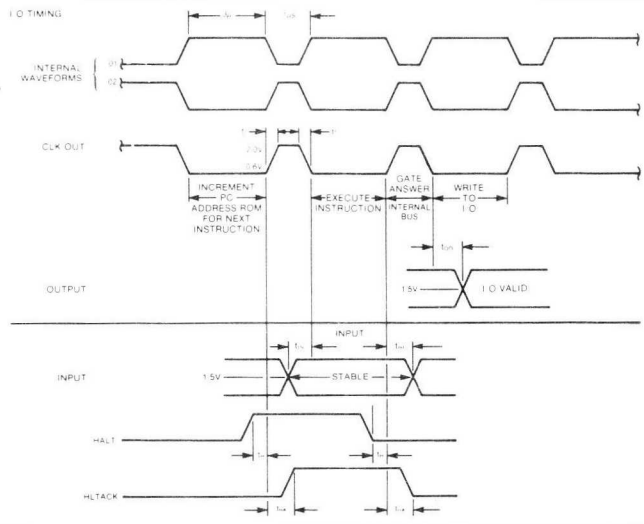
Standard Conditions (unless otherwise noted)
V_{CC}: +5V ± 5%
V_{XX}: +4.75V to 10.0V

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Power Supply Currents	I_{CC}	—	40	50	mA	
	I_{XX}	—	.5	5	mA	
Logic Inputs						
Low	V_{IL}	0	—	.65	V	
High	V_{IH}	2.4	—	V_{CC}	V	
Logic Outputs						
Low (See Note below)	V_{OL}	—	—	0.45	V	V_{XX}=5V @ I_{OL}=1.6mA
High	V_{OH}	2.4	—	V_{CC}	V	I_{OH}=100μA min.
Address A0-A8 Low	V_{ACL}	—	—	0.5	V	
AC CHARACTERISTICS						
OSC frequency	f_{IN}	.2	—	1	MHz	
RTCC frequency		DC	—	125	kHz	
CLKOUT frequency	—	.25 f_{IN}	—	—	—	
CLKOUT						
Rise Time	t_r	—	—	200	ns	1 TTL load and 100pF
Fall Time	t_f	—	—	200	ns	1 TTL load and 100pF
I/O Registers A, B, C, D Output Mode:						
Delay From CLKOUT	t_{DD}	—	—	500	ns	1 TTL load and 100pF
Input Mode						
Set-up	t_{IS}	0	—	—	ns	
hold	t_{IH}	100	—	—	ns	
Halt set-up	t_H	1	—	—	μs	
Halt Acknowledge	t_{HA}	—	—	500	ns	

**Typical values are at +25°C and nominal voltages.

NOTE: Output drive capability for I/O registers A, B, C, D may be customized to customers requirements. Internal pull resistors may be chosen to provide TTL compatibility or open drain to provide wired-or capability. Consult the factory for further information.

I/O TIMING



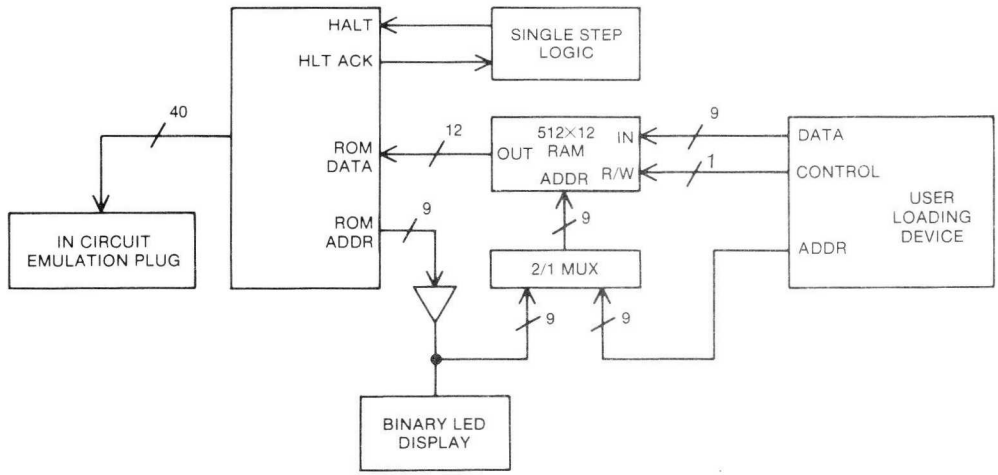
APPLICATIONS INFORMATION

The PIC1664 can be directly interfaced with external PROM (Programmable Read Only Memory) to duplicate the PIC1650 operation in the field. For added flexibility ultraviolet erasable PROM can also be used. A Field Demo Card is available (see next section) for this basic configuration or the user can design his own prototyping system.

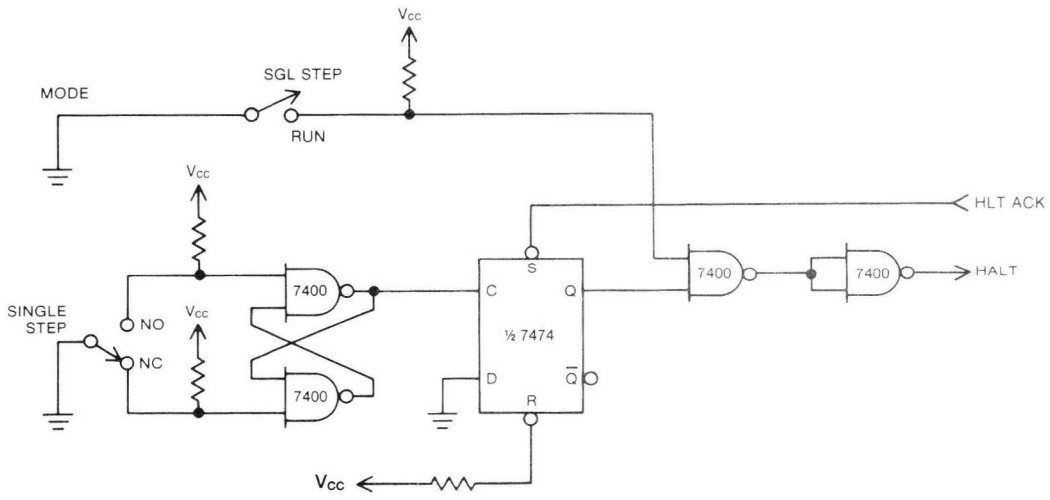
The PIC1664 is utilized in two prototyping modules offered by General Instruments. The FD1664 Field Demo Card replaces the PIC1650 circuit array with a PIC1664 and external PROM. The DB1650 Development Module is a full debug system providing both in circuit emulation and easy program changes via a TTY input.

A simple user designed prototyping system might include single step capability, program address display, and easy program changes using RAM rather than ROM for the PIC1664 program memory as shown in the following block diagram.

TYPICAL PROTOTYPING SYSTEM



SINGLE STEP CIRCUIT



PIC Development System

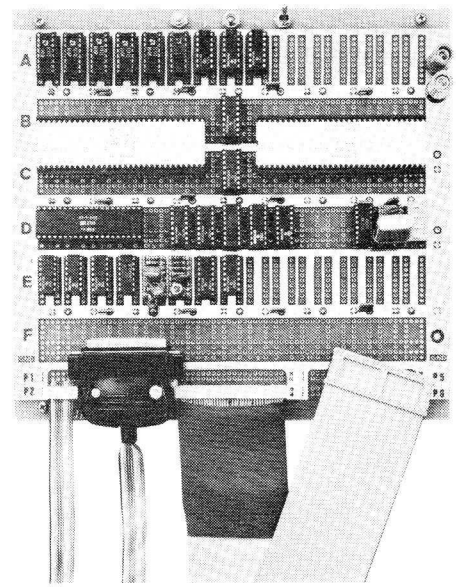
FEATURES

- Full debugging capability
- In circuit emulation
- Direct TTY interface

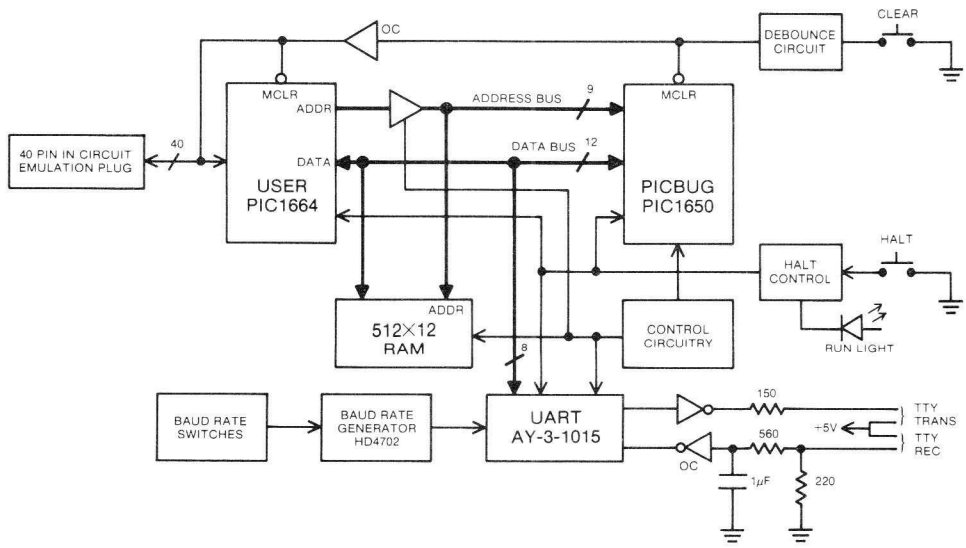
DESCRIPTION

The DB1650 allows the user to test his 1650 program in the actual environment of his hardware application. A powerful interactive debugger program is provided for easy troubleshooting and program corrections.

The DB1650 contains a PIC1650 programmed with PICBUG. PICBUG is a debug program (fully described later in this section) by which the user can load his PIC1650 program and execute in either a run or single step mode. PICBUG interacts with a PIC1664 and a 512×12 bit RAM which emulates the users PIC1650. A TTY terminal attaches to the DB1650 allowing the user to control and monitor the operation of his program. Execution can begin at any point in the program and all registers as well as program memory can be examined or modified through the TTY. When the complete program is fully debugged, PICBUG can punch the new object tape using the TTY paper tape punch unit. The DB1650 contains a 40 line ribbon cable which terminates in a 40 pin DIP plug which replaces the PIC1650 in the user's application thus providing a true in-circuit emulation capability. Dimensions: 8½"×8".



BLOCK DIAGRAM

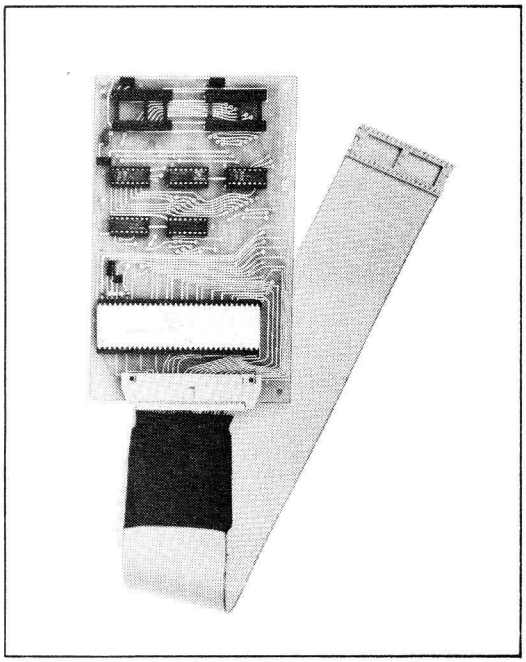


PIC Field Demo System

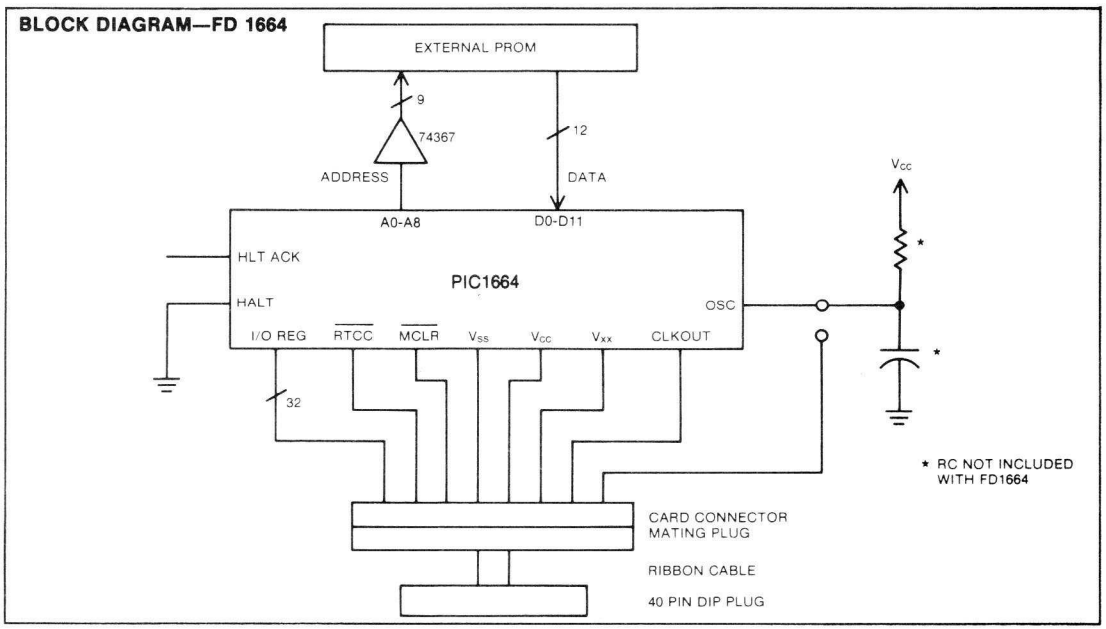
DESCRIPTION

The PIC Field Demo Card is used to demonstrate a PIC 1650's capability in the field before committing to a masked ROM. The card contains a PIC1664 and two 74367 driver circuits for the address lines. In addition there is provision for using 512×4 PROM IC's (eg. 82S131) or 512×8 ultraviolet erasable ROM (5204). The card is complete with sockets for the PIC1664, driver ICs, and external ROM. External ROMs are not provided. The card terminates in a 40 pin edge connector. A ribbon cable is supplied which connects to the FD1664 on one end and terminates to a PIC 1650 compatible 40 pin DIP plug on the other end.

Both V_{CC} and V_{XX} are input to the FD1664 through the card connector. If 5204 ultraviolet erasable ROMs are used then an external 12V supply must be connected to the FD1664. Provision is made for driving the OSC input of the PIC1664 either through the external connector or by placing the RC network on the FD1664. Dimensions: 6½"×4"



BLOCK DIAGRAM—FD 1664



PIC Assembler

FEATURES

- Symbolic representation of all instructions.
- User defined six character symbols.
- Octal decimal, hexadecimal and ASCII literals.
- Expression evaluation.
- Extensive assembly directives.
- Full program and sorted symbol listing.
- Extensive error detection.

DESCRIPTION

The PIC assembler converts symbolic source programs for the PIC1650 into suitable code. Programs for the PIC may be coded symbolically using methods and techniques common to assembly level coding for conventional stored program computers. The PIC assembler produces a binary paper tape output which may be loaded and executed by the PIC Development System or used to directly mask program a PIC chip.

The PIC assembler is available in two versions allowing execution on a wide variety of computers. One version, coded in FORTRAN IV is intended for use on popular mini-computer and larger computer systems and time sharing systems. The other version, coded in CP1600 assembly language executes on a GIMINI microcomputer with at least 6K words of 16-bit RAM storage.

USING PICAL ON THE GIMINI

The PIC Assembler (PICAL) requires GIMINI microcomputer with 8192 words of RAM and a ASR33 teletype terminal or equivalent for execution. A high speed paper tape reader/punch may be used for available. PICAL is loaded into the GIMINI by mounting the load module tape in either the low speed or high speed tape reader and entering "LL" (load via low speed reader) or "LH" (load via high speed reader) when at the monitor "$" level. Note that all user inputs must be terminated by a carriage return. When the load is completed, a loader summary is printed and the monitor returns to the "$" level. Execution of PICAL is started by entering "E0" when at the "$" level.

Upon initial start-up, PICAL identifies the version in use, indicates assembly pass 1 and requests source input device identification by printing "SCR?(H/L)". The user must respond with "L" (low speed reader) or "H" (high speed reader). If the source tape contains valid 7 level ASC11 data, i.e., was punched on a parity generating device, a "7" is entered immediately following the device indicator. If only a carriage return is entered in response to the "SRC?" request, control is returned to the resident monitor. Next, the user may select a separated tape mode by responding to "SEP TAPES?(Y/N)" with "Y". If this mode is selected, PICAL will pause (GIMINI halts) after each physical tape segment is read (indicated by text ending with a form feed character). When the next source tape segment is mounted in the appropriate reader, the GIMINI START/STOP switch is depressed, continuing the assembly process. Finally, "LST?(Y/N)" is printed allowing the user to select a pass 1 program listing if desired.

At the end of pass 1 "PASS 2?(Y/N)" is printed allowing the user to elect to rerun pass 1 or proceed to pass 2. Prior to running pass 2 the source tape must be repositioned at the beginning. If in the segmented tape mode, physical tape segments must be read in the same order as in pass 1. After the pass 2 listing option is selected, "DEV?(H/L/N)" is printed allowing the user to select object tape output on the high speed punch, low speed punch or specify no object output. If a pass 2 listing and object output on the low speed punch have been selected, "DEVCNFLCT" is printed and the options are requested again.

If object output is on the low speed punch "PUNCH ON" is printed to remind the user to manually enable the teletype punch. PICAL waits until the user enters a carriage return to indicate that the punch has been enabled. At the end of pass 2, "PASS 2?(Y/N)" is printed, allowing the user to rerun pass 2 or return to pass 1.

FORTRAN IV PICAL

PICAL can be used on a wide variety of computers with real time operating systems using the FORTRAN IV version. With this configuration PICAL will first ask for the source file name. The next PICAL question is for a listing of the assembly. N gives no listing, Y gives a listing on the terminal. Typing F = file name transfers the listing to a file which can be printed at a later time. The last PICAL question requests the user to give the file name for the object tape produced by PICAL. The formats and diagnostics are the same for both the FORTRAN and GIMINI versions of PICAL.

SOURCE PROGRAM FORMAT

A PIC source program is composed of a sequence of statements with each statement contained on a single line terminated by a carriage return character. A statement may contain up to four fields, identified from left to right as follows:

LABEL OPERATOR OPERAND COMMENT

The label and comment are optional, while the operator is always required. The presence and nature of the operand depends upon individual operators. Statements should not exceed approximately 50 characters so that assembled programs can be printed on a teletype or similar terminal.

LABEL

A label is a user defined character string, used to symbolically reference a specific location within a program. If a statement contains a label, the label must begin in the first character position in the statement. Labels may contain up to six characters, the first of which must be a letter (A-Z), a currency symbol ($), a question mark (?) or an ampersand (&). The remaining five optional characters may be any combination of A-Z, 0-9, $, ? or &.

OPERATOR

An operator follows the label field in a statement. A statement operator contains up to six characters and may be an instruction mnemonic or an assembly directive. Instruction mnemonics are symbolic character strings which represent the various PIC micro instructions. Assembly directives are symbolic character strings used to represent certain actions performed by the assembler. If a statement does not contain a label the operator must be preceded by at least one blank space. If the operator is the last field in a statement, it may be followed by a carriage return, otherwise it is followed by the comment field.

OPERAND

An operand follows the statement operator separated by at least one blank space. Operands may be blank space. Operands may be symbols, literals or expressions. When multiple operands are used, they are separated by commas. If an operand is the last field in a statement it is followed by a carriage return, otherwise it is followed by the comment field.

COMMENT

The comment field is optional in all statements and must be preceded by a semicolon (;). The contents of the comment field are printed on the program listing but have no effect on the assembled program. Entire lines may serve as comments if the first non-blank character is a semicolon. Blank lines may be used to separate statement lines in order to enhance program readability.

SYMBOLS

A symbol is a user defined character string which appears in an operand and is used to represent the value assigned to the symbol by the assembler. A symbol is given a value by direct assignment via an assembly directive or by appearing in the label field of a statement. Instruction labels are given the value of the assembly location counter associated with the instruction. The assembler recognizes the exclamation mark (!) as a special symbol for the current value of the program counter.

LITERALS

Literals are character strings which serve as sources of data, i.e., cannot be changed and are interpreted by the assembler as constants. Literals may be expressed as octal, decimal, hexadecimal, binary and character and may be preceded by a plus (+) or minus (-) to signify sign. Plus is assumed unless a minus is present.

Octal

soooo - s = optional + or –, + assumed
o = 0-7; 0 to 7777

Decimal

s.dddd - s = optional + or –, + assumed
= leading character
d = 0-9; 0 to ± 2047

Hexadecimal

sX'hhh' - s = optional + or –, + assumbed
X' = leading characters, ' = trailing character
h = 0-9, A-F; 0 to FFF

Binary

sB'bbbbbbbbbbbb' - s = optional + or –, + assumed
B' = leading characters, ' = trailing character
b = 0, 1; 0 to 111111111111

Character

s"C" or 'C' - s = optional + or –, + assumed
"or" = leading and trailing characters
C = any ASCII character

EXPRESSIONS

Arithmetic operators + and - may be used to form operand expressions containing up to six elements. An expression element may be a user defined symbol, the assembly location counter (!) or a literal. Expression elements are separated by + or - and an expression is terminated by a comma, carriage return or a semicolon (;). Expressions are evaluated from left to right with no parenthetical groupings allowed.

ASSEMBLY DIRECTIVES

	ORG	exp	Set the assembly location counter of the value of expression. Program assembly starts at zero by default.
Symbol	EQU	operand	Assign the value of the operand to the symbol. The operand may be a symbol, a literal or the assembly location counter symbol (!). If ! is specified it may be followed by + or - and a literal. Note that only one level of forward symbol reference is allowed.
Symbol	=	operand	
(Label)	ZERO	expression	Zero a block of storage whose length is specified by the expression. If a label is specified it is assigned a value equal to the address of the first word in the block.
(Label)	DATA	expr , [expr. . . .,expr]	Generate a data word for each operand expression. The contents of each word is set equal to the value of the respective expression. If a label is specified it is assigned a value equal to the address of the first word generated.
	END		End of the program, the assembly is terminated on the previous statement.
	PAGE		Advance the listing to the top of the next page.
	TITLE	name	Use the specified six character name in the listing page heading.

PROGRAM LISTING

The PIC assembler produces a listing of the assembled program containing the following fields: Line number; address; contents; label; opertor; operand(s) and comment. The address field contains three octal digits (eight bits), the contents field contains four octal digits (twelve bits) and the label, operator, operand(s) and comment fields are columnized to enhance program readability. Each page of listing contains sixty lines and begins with a one line heading. At the end of the program listing all user defined symbols and the number of diagnostics issued are summarized.

BINARY MACHINECODE

The PIC assembler produces binary machine code punched on paper tape formatted for loading by the CP1600 resident loader. This format permits the program to be loaded into suitable CP1600 microcomputer memory locations for execution by a PIC emulator. The paper tapes are formatted into one or more variable length binary records. Each record contains a four frame header and up to 132 data frames followed by a check sum frame. The first frame in each record contains a 001 except for the last record which contains a 377. The second frame contains the PIC assembly base address, the third frame contains 000 and fourth frame contains the number of data frames following in the record. The last data frame is followed by record check sum frame which is used to verify the data when the tape is read. Each PIC instruction is punched in a three frame sequence which contains 001, the least significant eight bits and the most significant four bits. Address adjustments resulting from imbedded ORG or RES assembly directives result in a three frame sequence containing a 000, the address adjustment and 000.

DIAGNOSTICS

The PIC Assembler issues the following diagnostic messages when the indicated error conditions are detected:

SYNTAX	Syntax error
LABEL	Label illegal or missing
OP UNREC	Operator unrecognized
UNDF SYM	Undefined symbol referenced
DBL DEF	Double or multi-defined symbol
MDEF SYM	Double or multi-defined symbol referenced
FILE REG	File Register designator illegal
BIT NUM	Bit Number designator illegal
OPRN VAL	Operand value illegal
LITERAL	Literal illegal
DEST	Destination illegal
PHASE	Phase error, i.e., symbol has different definition in pass 2 than in pass 1
?SYNTAX	Questionable syntax
?LABEL	Questionable use of label
ADR/DEST	Questionable address or destination
?USE	Questionable use of directive
MEM LIM	PIC ROM limit exceeded
TRUNCATN	Statement field too long, truncated

PIC Simulator

FEATURES

- Simulation of all PIC instructions.
- Access to all PIC operational registers.
- Execute, Trace and Step Modes.
- Console—interrupt and up to eight program breakpoints.
- Real time clock simulation.
- Input/output simulation.
- Execution time accumulation.
- Symbolic instruction mode.
- Numeric quantities expressed in octal or decimal.

DESCRIPTION

The PIC simulator (PICSIM) is a program which simulates the PIC1650. Programs assembled by the PIC symbolic assembler or programs entered manually may be quickly and easily debugged and verified using PICSIM.

The PIC simulator is available in two versions allowing execution on a wide variety of computers. One version coded in FORTRAN IV is intended for use on popular minicomputer and larger time sharing systems. The other version executes on a GIMINI microcomputer.

PICSIM executes on a GIMINI microcomputer with at least 6K words of RAM memory and a teleptype or equivalent console. PICSIM is supplied as a relocatable load module which is loaded and executed using the GIMINI resident monitor. The user communicates interactively with PICSIM using a set of commands which are used to control the simulation environment and program execution.

USING PICSIM ON GIMINI

A terminal and a high speed reader/punch are required to use PICSIM on the GIMINI microcomputer system. The PIC simulator program tape is first loaded via the high speed reader by the loader command "LH". To execute, command "E" is typed in. PICSIM identifies the version in use and prints out "Command summary? (Y/N):" The user responses with "N", if the printout of those commands are not required. Next PICSIM will request the next command to be executed by printing "Command?" To load the object tape, "LH" is entered. PICSIM will again request another command. The user can then enter any of the commands described below.

FORTRAN IV PICSIM

PICSIM can be used on a wide variety of computers with real time operating systems. With this configuration the first PICSIM command would be L. This would load the object tape produced by PICAL into PICSIM. The appropriate file name for the object file is entered at this time. At this point the execution of PICSIM is identical to the GIMINI version.

COMMANDS

The following commands may be entered on the console keyboard whenever a command prompt is displayed. Numeric quantities in commands, indicate by n, a, i, j in the descriptions may be entered in octal or decimal format. Decimal quantities are preceded by a period, i.e., ".15" is decimal 15 where "15" is octal 15. Quantities displayed by PICSIM are always in octal. If a command is unrecognized or contains an error, a "?" is displayed followed by another command prompt. All commands must be entered as indicated followed by a carriage return.

? — Display Command Summary

Bn, A — Set program breakpoint n (0-7) at memory address a (0-7777).

Bn — Remove program breakpoint n (0-7).

B — Remove all program breakpoints.

Cn — Continue program execution from the current breakpoint. If optional n is specified, n subsequent program breakpoints that may be encountered will be ignored. This feature is useful when a program loop is to be breakpointed after n executions. If the current program was not breakpointed, the message "NO ACTIVE BRK PNT" is issued and the command is rejected.

DB — Display the currently specified program breakpoints. If the program was breakpointed, that breakpoint is preceded by "@". If a console interrupt (CNTRL/C) caused a breakpoint "@ C=address" is displayed. If there are no breakpoints set, "NONE!!" is displayed.

DIi,j — Display the instructions from memory locations i to j inclusive in symbolic format. See note 1.

DMi,j — Display the contents of memory from location i to j inclusive in dump format. See note 1.

DR — Display the contents of the W register, the RAR (Return Address Register Stack) and the 32 file registers. See note 1.

DT — Display the accumulated program execution time in microseconds.

Ea — Execute starting at memory address a. If a is not specified, execution starts at the current PC (File Reg. 2) address. When program execution starts, the execution time counter is zeroed. See note 3.

Fn — Inspect/change the contents of File Register n (0-.32). See note 2.

Ia — Inspect/change the instruction at memory address a in symbolic format. See note 2.

Lda — Load memory from device d (H=high speed, L=low speed) starting at address a.

Ma — Inspect/change the contents of memory address a. See note 2.

Oi,j — Output the PICSIM object file from address a to b. See Note 4.

Pdi,j — Punch the contents of memory on device d (H=high speed, L=low speed) from address i to j inclusive.

Rn — Set the interrupt repetition rate to n PIC machine cycles and activate the real time clock counter.
R — Deactivate interrupts.

R? — Display the current interrupt repetition rate.

Sa — Step the program starting at memory address a. If a is not specified, stepping starts at the current PC (File Reg 2) address.

Ta — Trace program executions starting at memory address. If a is not specified, tracing starts at the current PC (File Reg 2) address. As each instruction is executed, the contents of the PC (program counter) is indicated by the display "@aaaa", where aaaa is the current address. See note 3.

W — Inspect/change the contents of the W register.

X — Exit to the GIMINI resident monitor.

ZM — Zero memory.

ZR — Zero registers, (W, RAR and File Registers).

ZS — Zero RAR Stack.

ZT — Zero the accumulated execution time.

NOTES:

1. Striking console key "C" while depressing the "CTRL" key causes the console output to be terminated on GIMINI Systems. On time sharing systems the "Break" key is used.

2. Entering "/" opens the next location or register, "-" opens the previous location or register.

3. Striking console Reg. "C" while depressing the "CTRL" key on GIMINI Systems causes program execution to be suspended and interaction with the user resumed. The display "!C@aaaa" indicates which instruction, i.e., aaaa is its address, was about to be executed. CTRL/C acts just like a breakpoint. On time sharing systems the "Break" key is used.

4. Used on FORTRAN version to output edited object tape.

INPUT/OUTPUT

PICSIM provides for simulation of both input and output operations through PIC file registers 5, 6, 7, 8 (IOA, IOB, IOC, IOD). Whenever an instruction sample file registers 5, 6, 7 or 8, the following display is output on the console: "@aaaa, T=n USEC, ENTER IOREG DATA:" and program execution is suspended. In the display, "@aaaa" indicates the memory address of the instruction, "T=n USEC" indicates the accumulated execution time and "f" is A,B,C or D. Program execution resumes after the user enters appropriate data. Whenever an instruction places data in file registers 5,6,7 or 8, the following display is output on the console: "@aaaa, T=n USEC, IOREGf=dddd" and program execution continues. In the display, "@aaaa" indicates the memory address of the instruction, "T= USEC" indicates the accumulated execution time, "f" is A, B, C or D and "dddd" is the current contents of the register.

SYMBOLIC INSTRUCTIONS

The following symbolic instructions may be entered into memory from the console:

NOP	COMF f,d	BTFSS f,d
MOVWF f	INCF	RETLW i
CLRW	DECFSZ	CALL i
CLRF f	RRF f,d	GOTO x
SUBWF f,d	RLF f,d	GOTO0 i
DECF f,d	SWAPF f,d	GOTO1 i
IORWF f,d	INCFSZ f,d	MOVLW i
ANDWF f,d	BCF f,d	IORLW i
XORWF f,d	BSF f,d	ANDLW i
ADDWF f,d	BTFSC f,d	XORLW i
MOVF f,d		

where f = file register 0-37 (0-.31)
d = destination: 0 or W; 1 or F
i = literal 0-377 (0-.256)
x = literal 0-777 (0-.511)

ERROR CONDITIONS

PICSIM detects several error conditions while simulating the execution of PIC programs. The following error messages are issued as a result of the indicated error conditions. After the error message is displayed program execution is suspended and a command prompt is issued.

@aaaa, STK OVERFLOW!!	More than two levels of CALL instructions have been executed.
@aaaa, STK UNDERFLOW!!	More than two levels of RET instructions have been executed.
@aaaa, INVALID READ OF PC!!	The program has attempted to read the contents of PC (File register 2), i.e., the program counter.

PIC Debug

DESCRIPTION

PICBUG is a debug program contained in a PIC1650, which will enable the user to debug his PIC application program contained in 512X12 of RAM on the DB1650 Development System.

PICBUG contains the debug commands listed below (boldfaced items are typed by the user) and the TTY service routines and the ability to terminate a lengthy display listing, and issue another command prompt, by the user depressing Control C.

PICBUG COMMANDS

1. ADDRESS INSPECTION

$Aa(CR) Inspect address a (in octal)

Example:

$A200(CR) Inspect address 200.
200 = 07142: Address 200 contains 7142

Note: After typing the selected memory contents PICBUG prompts a colon. The user can inspect the following memory location by typing a / or the previous location by typing a -. To modify the memory location the user simply types in the desired value. A(CR) terminates the command.

Example:

$A200(CR) Inspect address 200
200 = 7142:/ Address 200 contains 7142
201 = 3403:**2103/** Address 201 contains 3403, this is modified to contain 2103
202 = 1200: — Address 202 contains 1200
201 = 2103:**(CR)** Address 201 contains 2103
$ Next Command

2. ADDRESS DISPLAY

$DAa,b(CR) Display the contents of program memory addresses a to b inclusive

Example:

$DA202,213(CR) Display the contents of addresses 202 to 213 inclusive.

```
202   1200  3131  7416  0000  2451  0615  5216  4407
212   2616  6252
$
```

3. REGISTER INSPECTION

$Rn. Inspect Register number n (in octal). Note: W register is number 40.

After displaying the register contents, PICBUG prompts a colon. By typing a new value after the colon the user can modify the register contents. A(CR) terminates the command. Note that the / and - responses are not recognized by this command. Note that when register zero is displayed the result is the contents of the register pointed to by the File Select Register (F4). The contents of the W register cannot be modified using the R command.

Example:

$R20.235:**(CR)** Register 20 contains 235
$R26.306:**001(CR)** Register 27 contains 306 which is modified to 001
$R26.001:**(CR)** Register 27 contains 001
$ Next command

4. DISPLAY ALL REGISTERS

$DR Displays all registers including W. The W register is displayed on the same line as the command.

Example:

$DR135

```
 0   372  054  265  111  373  366  175  203
10   040  166  251  175  122  005  312  017
20   235  101  333  000  157  216  001  377
30   166  231  274  372  077  157  222  134
$
```

Note: The register 4 (the File Select Register) points to Register 33 (the 5 LSBs of register 4). Therefore registers 0 and 33 contain the same data in this example.

5. PROGRAM LOAD FROM TELETYPE READER

$L(CR) Load the PIC program memory from the teletype reader beginning at the origin specified on the tape.

6. PROGRAM OUTPUT TO TELETYPE PUNCH

$Pa,b(CR) Punch the PIC program memory on the teletype punch beginning at address a and ending at address b.

Note: Punch unit must be enabled before execution.

Example:

$P0,777(CR) Punch entire PIC program memory.

7. PROGRAM EXECUTION, BREAKPOINTS, AND SINGLE STEP

$Ea(CR) Execute the PIC program beginning at address a. If a is not specified then execution begins at address 777.

Note: There is no breakpoint command in PICBUG, however the PIC development card is designed to recognize the octal code 0001 as a halt command. When reaching a halt command PICBUG will output the W register and a new prompt.

Example: To execute the program from address 100 to address 135. After 135 is executed we want to examine register 15 then continue execution from that point.

$A136(CR)	Inspect address 136
136 = 6205:**1(CR)**	Change addr. 136 to halt
$E100.237:	Execute beginning at addr. 100. When halt at 136 is reached the W register contains 237
A136(CR)$R15.173:**(CR)**	Register 15 contains 173
136 = 0001:**6205(CR)**	Inspect address 136. Restore addr. 136 to original contents
$E136.	Resume execution beginning at addr. 136.

The PICBUG Execute command also contains a single step feature. The single step feature is enabled by considering the address field (a) in the Execute command as a 16 bit quantity and setting the MSB of this number to a one. This allows PICBUG to accept the T (single step command). Using the T command the program can be single stepped with the contents of the W register displayed at each step.

Example:	**Execute in single step mode beginning at addr. 206. W register after executing 206 contains 123.**
$A206(CR)	Inspect addr. 206
206 = 4325:**1(CR)**	Change addr. 206 to halt
$E200.173:	Execute beginning at addr. 200. When halt at 206 is reached the W register contains 173.
$A206(CR)	Inspect addr. 206
206 = 0001:**4325(CR)**	Restore addr. 206 to original contents
$E100206.0123:	Execute in single step mode beginning at addr. 206. W register after executing 206 contains 123.
$T0317:	W register after addr. 207 = 317
$T0164:	W register after addr. 210 = 164
$T0013:	W register after addr. 211 = 013
$	Next command

MICRO ELECTRONICS

SBA SERIES MICROCOMPUTER

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
LSI CIRCUITS			
1 BIT SINGLE CHIP MICRO-COMPUTER	The SBA can directly evaluate a set of Boolean equations. Thirty programmable inputs and outputs as well as memory make the SBA a true 1-bit microcomputer.	**SBA**	**3-30**
SINGLE CHIP DEVELOPMENT MICRO-COMPUTER	SBA microcomputer without ROM.	**SBA-1**	**3-41**
HARDWARE/SOFTWARE			
SBA FIELD DEMO SYSTEM	Contains an SBA-1, a program counter, and sockets to 5 1K PROMs.	**SBA-FD**	**3-42**
SBA COMPILER	Converts a list of Boolean equations to optimized SBA code.	**SBACOMP**	**3-43**
SBA SIMULATOR	Simulates all SBA actions for program debug and verification.	**SBASIM**	**3-48**

Single Bit Microcomputer / Sequential Boolean Analyzer

FEATURES

- Easy programming using Boolean equations.
- 1023 words of program
- 30 programmable inputs, outputs, or multiplexed input/outputs.
- 120 element Read/Write memory
- 16 element stack
- AND, OR, XOR, COMPARE, INVERT basic logic functions
- Simple and versatile clock generation
- TTL/CMOS compatible inputs and outputs
- Powerful output drive enabling direct interface to displays
- Simulator and software program compiling facilities available

DESCRIPTION

The SBA is a microprogrammable Sequential Boolean Analyzer which forms the basic controlling element for many systems requiring timing and control functions. The SBA is fabricated in GI's low voltage Ion Implant N-channel process resulting in high speed operation and low power dissipation.

APPLICATIONS

The SBA is suitable for a very wide spectrum of applications such as:

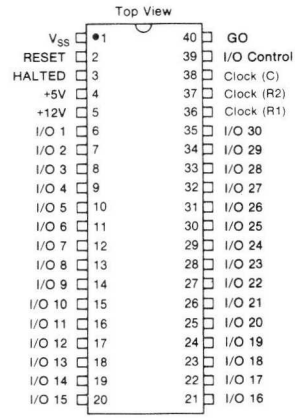
TELECOM: Simple PAX controllers, Relay circuit control, Answering machine controllers, Line seeker/monitor.

INDUSTRIAL: Complex sequential timers, Small machine controllers, Special purpose digital clocks, Alarm monitor.

CONSUMER: Gaming machines, White goods timers, Combination locks, Pinball machine/one arm bandit.

PIN CONFIGURATION

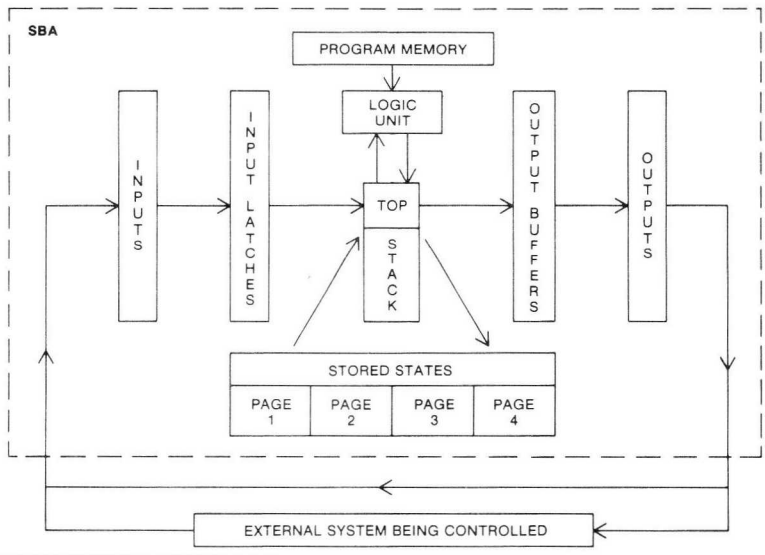
40 LEAD DUAL IN LINE



MICROPROCESSORS: As a slave processor for BCD/binary conversion, Binary/BCD conversion, Alarm condition monitor/interrupt generator, Peripheral controller.

In general the SBA is best suited to applications where a control response is required in milliseconds rather than microseconds.

BLOCK DIAGRAM AND DATA PATHS



PIN FUNCTIONS

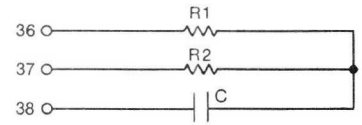
INPUTS/OUTPUTS — There ae 30 input/outputs on the circuit which can be mask programmed as inputs, outputs, or inputs/outputs.

I/O Control — When this output is at logic '0', those Inputs/Outputs that are programmed to be multiplexed will output information. When it is at logic '1', it may read input data.

CLOCK PINS — Pin 36 can be driven from an external clock source. Otherwise, components R1, R2 and C are connected as in the following diagram for on-chip clock generation. R2 and C provide the basic timing as required and R1 should be about 2 to 5 times R2.

Typical ranges are C=68-1000pF and R2=5-50K.

Typical suggested values are C=100pF, R2=5K, R1=15K.



RESET Input — When taken to a logic '1', this input will reset the program to the start position. Can be left unconnected if not required.

GO Input — When taken to a logic '0', this input will halt the program at the end of the program cycle and will activate the HALTED output. When taken to logic '1' or left unconnected, the program will cycle continuously.

HALTED Output — A logic '1' on this output indicates that the program has stopped cycling.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -0.3V to +15V
Storage Temperature Range ..... −65°C to +150°C
Operating Ambient Temperature Range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{CC} = +12V ± 10%
V_{GG} = +5V ± 15%

Characteristic	Min.	Typ.	Max.	Units	Conditions
Clock	10	—	800	kHz	Note 1
Inputs					
Logic '0' level	−0.3	—	+0.4	V	
Logic '1' level	+2.4	—	+12	V	
Current	—	—	10	µA	V_{IN} = +12V
Timing	—	—	—	—	Note 2
Outputs					
Logic '0'	—	100	—	Ω	0.7V at 7mA
Sink Current	—	7	20	mA	Max total power 150mW
Logic '1'	1.2	—	—	MΩ	open drain
Leakage current	—	—	10	µA	V_{OUT} = +12V
Timing	—	—	—	—	Note 2

NOTES:

1. Clock frequency controlled by external R/C network.
2. The timing of inputs and outputs depends on the clock frequency and the program length.
3. The SBA has a Power-down mode wherein the +12V may be removed with the +5V kept applied to hold the internal storage of the device. Power consumption in this mode is typically 25mW.

Powering-down sequence:

1. Take GO to logic '0' and wait until a program cycle is completed (HALTED becomes true). This avoids powering-down in the middle of an evaluation cycle.
2. Apply logic 'I' to RESET to hold the device stable while powering down.
3. Remove +12V.

All inputs except +5V may now be removed. The SBA will hold its memory indefinitely.

Powering-up sequence:

1. Apply RESET to hold device stable.
2. Apply +12V carefully (avoid surges and spikes).
3. Remove RESET and the SBA will continue from where it left off.

Note that any data left on the stack is not saved-only the stored states are saved.

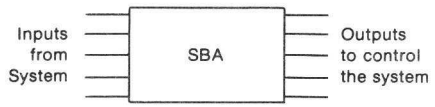
A. INTRODUCTION

The Sequential Boolean Analyzer (SBA) is a very simple single bit processor which can directly evaluate a set of Boolean equations.

The use of Boolean Equations as a 'programming language' has a number of unique advantages:

1. it is concise
2. it is standardized worldwide
3. engineers already use it and *understand it*
4. universities teach it now and have done so for many years.
5. it serves the dual purpose of both program and documentation
6. it has stood the test of time.

The equations define the logic that controls the system to which the SBA inputs and outputs are connected.



In addition to Boolean logic, most systems require that some events have to be 'remembered', this being the reason for the use of flip flops in TTL type logic implementations. In the SBA a number of internal storage elements are provided for such purposes.

A memory is used to hold an encoded version of the Boolean equations that define the desired function of the SBA and there is a one to one correspondence between the data in this memory and the Boolean Equations as written by an engineer.

B. PRINCIPLE OF OPERATION

A block diagram of the SBA showing the program memory, inputs, logic unit, stack, stored states and outputs is shown in Fig. 1.

The SBA functions as follows:

1. The new inputs are read in from the system being controlled and are latched into the input latches.
2. The SBA now reads the Boolean equations out of the memory and, using the logic unit and the stack, it processes the input data and stored states one Boolean term at a time to produce results which are either 'remembered' as stored states or placed in the output buffer.
3. The Boolean equations are taken from the memory term by term and when all the equations have been evaluated the results are transferred from the output buffers to the outputs and thus to the system being controlled. The program address counter is then reset and the cycle begins again.

C. BASIC PROGRAMMING

The internal operation of the SBA need not concern the user. The device can simply be thought of as a variable array of logic. It can be treated as abstract logic or as the logic family most familiar to the engineer, although speed and response time must be considered separately as it is somewhat unique in the SBA.

The logic representing the function to be performed by the SBA is described by a set of Boolean Equations. These can be of any length and are composed of the four logical functions, AND, OR, EXCLUSIVE OR and COMPARE, together with invert or negate and as many levels of brackets as are required. Rules and restrictions are minimal.

Stored States — Basic Storage

The Stored States can be used to store the state of some input or logical combinations from one program cycle to the next. For example, if it were required to produce an output whenever an input changed state, the value of the input must be stored and compared with the new input in the next cycle. The equations might be:

output = input * store; (where * represents exclusive OR)
store = input;

Thus, when the input is different from the stored value, i.e. the state of the input last time, the output is produced.

It should be noted here that because of the sequential nature of the SBA the equations are performed one at a time. So the 'store' equation must come after the 'output' equation otherwise the

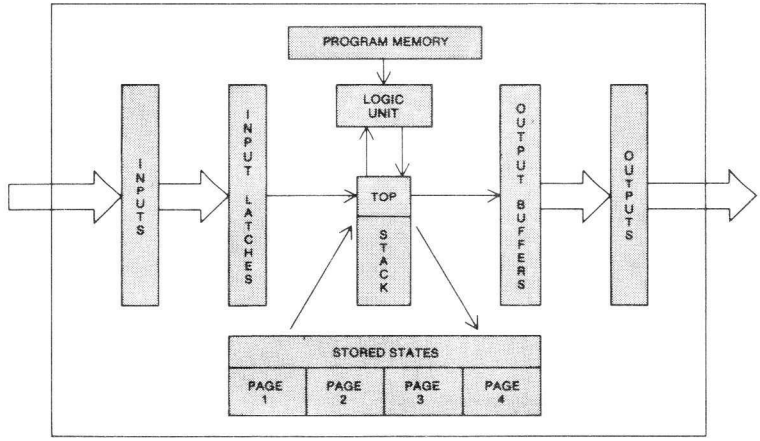


Fig. 1 BLOCK DIAGRAM

store would contain the same value as the input of the current program cycle.

The Stored States can also be considered in groups for storing numbers, machine states, etc., and also for counters and sequence generators. Again the equations can either be generated purely logically from a truth table of the required sequence or by considering an appropriate hardwre solution.

Stored State — Temporary Storage

Stored States do not necessarily have to be used as stores from one cycle to the next. It is often convenient to use these as temporary stores within a program cycle. A typical example is when a calculated value is to be used in several equations. Rather than calculate the value each time, it can be calculated once and stored and then read directly from the store as required. Such 'temporary stores' may be updated as many times as required in a program cycle and it is often convenient to reserve a couple of stored states on each page for this purpose. An example might be the Stored State 'temp' being used as a reset for a store and then later as an enable for an output:

```
temp = reset logic;
store A = (store A logic).-temp;
store B = (store B logic).-temp;
etc., then later in the program
temp = enable logic;
output A = (output A logic).temp;
output B = (output B logic).temp;
etc.
```

If the SBA compiler is used, the name for the temporary store must be the same (as 'temp' above) to define the same bit and it can be seen that there might be confusion in knowing the function of the store in a particular part of the program. The problem can be solved by knowing that SBACOMP only takes the first 4 characters of the name. So as long as these remain constant, the same bit of storage will be used and the name can be extended to indicate the current use of that particular store. In the above example the names could have been 'tempreset' and 'tempenable'.

Order of Equations

The most important rule in SBA programming has already been mentioned and that is the order of the equations. While the timing as seen external to the device is clearly defined, it must always be remembered that the equations within a program cycle are performed in sequence and care must be taken to ensure that stores are updated at the right time.

The first example illustrates the overall construction of a program and is demonstrated by considering the store defining the current state of the machine. The state will be output to the system being controlled and the inputs read back from the system. These, together with the present state, will define the next state to be output to the system. When the state number is used in the SBA equations, the position of that equation in relation to the equations updating the state will obviously define which state is being referred to. The state number before updating will refer to the state output to the system last time and will therefore be associated with the current inputs since these are a direct result of that state. The state number after updating will refer to the next state and will be used in determining the outputs.

Another important time to watch the updating of stores is when using such things as counters. A 3 bit binary counter stepped by 'step' might be written:

```
A = A*step;
B = B*(step.A);
C = C*(step.A.B);
```

where the least significant bit changes whenever 'step' is true and the subsequent bits only when all previous bits are true AND 'step' is true. It can be seen that the equations cannot be written as shown because the values on the right hand side refer to the present value of the counter and those on the left hand side the next value. After the first equation, A has been updated and so in the next equation the wrong value wili be read. (Note that a hardware solution would update all bits in parallel.) In this case the stack can be utilized to advantage by storing the new values as they are calculated and only when all bits are completed are the stored states updated from the stack. The example would actually be written:

```
stak = A*step;
stak = B*(step.A);
stak = C*(step.A.B);
C = save;
B = save;
A = save;
```

Equations 3 and 4 can be combined but, if written like this for clarity, they will, in fact, be combined by the compiler.

The Pages of Stored States

The order of equations and the variables within the equations can also be important (as far as economy of instructions are concerned) when the different pages of Stored States are used. Equations using variables from more than one page can, in extreme circumstances, use more page change instructions than actual processing!

For this reason, those bits commonly used together (e.g. counters) should be grouped on a single page. It is better to leave a page partly unused in order to do this. Thus four 15 bit counters would certainly be better put one counter per page with the odd associated bits (like resets) kept on their respective pages, rather than squeezing onto two pages and having to put resets etc., on a different page.

If possible, processing should be performed in the order of pages. Thus page 1 processing would be done first, then page 2 and so on to avoid unnecessary page changes. It is easiest to write the program first and then allocate the stores to pages to get the flow right. Data transferring from one page to another can often be stacked first as demonstrated in the following.

Bits on page 1 labelled 1A, 1B, 1C to be moved to page 2, bits labelled 2A, 2B, 2C, and if written:

```
2A = 1A;
2B = 1B;
2C = 1C;
```

will use 11 instructions while:

```
stak = 1A;
stak = 1B;
stak = 1C;
2C = save;
2B = save;
2A = save;
```

uses only 9. If the pages were 1 and 4, the number of instructions would be 17 and 11; if moving page 3 to page 2 we would have 14 against 10. Obsessive page instruction saving is, however, not usually required and is only important when using the ROM to its maximum capacity. It is generally best to write the equations initially using the simple basic rules and to resort to more clever reduction techniques if the ROM is filled.

D. PROGRAMMING EXAMPLES

Combinational Logic

Little needs to be said here since any boolean equations is valid and can include AND, OR, EXOR, COMPARE and INVERT operators and as many variables and brackets as are required.

For greatest economy of instructions the equation should be minimized as far as possible, using EXOR and COMP if appropriate, and in general sums of minterms are most efficient.

Latches

The straightforward storing, temporarily or otherwise, of input data or logical combinations has been discussed and needs no further comment.

However, it is often required that a piece of data be latched into a store, and in hardware solutions devices such as S-R, J-K and D type latches are available for this function. The stored states in the SBA together with a bit of logic can be made to act as latches, the type being limited only by the imagination. A few examples are as follows:

(a) Simple S-R latch that is set by the variable 'set' and reset by 'reset': Q = set + Q.-reset
(b) In (a) the 'set' will override if both inputs appear together. If 'reset' is to override: Q = (set + Q).-reset
(c) Clocked latches have greater variety, a simple D type being: Q = data.clock + -clock.Q
(d) A clocked set - reset:
Q = (set.clock) + Q.-(reset.clock)
(e) Clocked set, asynchronous reset, set override:
Q = (set.clock) + Q.-reset
(f) Clocked set, asynchronous overriding reset:
Q = ((set.clock) + Q).-reset
(g) Full J-K latches:
Q = J.clock.-Q + Q.-(K.clock)

It is usually best to design the latch to fit the particular requirement since, in general, the more features required the more instructions are needed. If a latch is required to change on a particular edge of a clock, another store is required and we have, for example:

```
clock = inclock.-storeclock;
storeclock = inclock;
```

to detect the 0-1 transition. Either or both edges can be detected in this way. It can be noted here that once an input clock has been monitored for a transition then anything in the whole of that program cycle can be clocked by the same edge.

Counters and Sequence Generators

There are several ways in which counters can be programmed, but a good general purpose method is described here.

The counter will have an input to tell it when to count and let this be called COUNT.

Consider each bit of the counter in turn, from the least to most significant bits, and determine the conditions that require that bit to change. This condition, ANDed with COUNT, can be made to change tne bit using the exclusive OR instruction. So for the Rth bit, if the change condition is CR we have:

```
R = R*(COUNT.CR);
```

Care must, of course, be taken to ensure that bits are not used after they have been updated. They can be stored conveniently on the stack. In a binary counter each bit changes when all bits of lower significance are true, and we have, for a 4 bit counter as an example:

```
stak = A*COUNT;
stak = B*(COUNT.A);
stak = C*(COUNT.A.B);
stack = D*(COUNT.A.B.C);
D = save;
C = save;
B = save;
A = save;
```

If the counter is to step each program cycle (for a switch scanner or a counter using the cycle for its timing, for example), COUNT can be removed and the first equation changed to stak = -A;

The binary case is very regular and an alternative approach, which is more economical for large (over 4 bits) counters, uses temporary stores to build up the change conditions progressively:

```
T1 = COUNT.A
A = A*COUNT
T2 = T1.B
B = B*T1
T1 = T2.C
C = C*T2
T2 = T1.D
D = D*T1
etc.
```

Note that this time stacking has been avoided since the change condition is built up progressively. It can also be seen that only two temporary stores are required.

The technique is further illustrated by considering the following 'random' sequence:

State	DCBA
1	0000
2	0111
3	1110
4	0001
5	1011
6	0011
7	0100
8	1001
9	0000;

Examining each bit we see that:

A changes after states 1, 2, 3, 6, 7, 8
B changes after states 1, 3, 4, 6
C changes after states 1, 3, 6, 7
D changes after states 2, 3, 4, 5, 7, 8

Assuming the non-valid states cannot occur, and using standard reduction techniques, the change conditions reduce to:

```
CA = -A + B.-D + -B.D
CB = -C.-D + C.D
CC = -A + B.-C.-D
CD = C + D + A.-B
```

Now including STEP, and reducing still further for the SBA using exclusive OR(*) and compare (#), we have finally:

```
stak = A * STEP.(-A + (B*D));
stak = B * STEP.(C#D);
stak = C * STEP.(-A + B.-C.-D);
stak = D* STEP.(C + D + A.-B);
D = save;
C = save;
B = save;
A = save;
```

And, for completeness, the carry output is given by A.-B.-C.D, reducing to:

```
COUT = -B.D;
```

which should go at the beginning, before the states are updated.

E. SYSTEM DESCRIPTION

The Sequential Boolean Analyzer consists of the following major components (refer to Fig. 1):

1. A Program Memory which holds the set of Boolean equations defining the system operations. In the single chip version of the SBA this is contained in an on-chip mask programmable ROM. There is another version (SBA-1) in which the program memory is off the chip and it can then be ROM, RAM or PROM as required. The Boolean equations which define the logical relationships between the SBA inputs, stored states, and outputs are stored in the memory as 8 bit words in an encoded form. An exact definition of the code is given in the next section.
2. A set of up to 30 input buffers which are latched at the start of the evaluation of Boolean equations. This is done so the input values are consistent during the whole period of time it takes to evaluate all the Boolean equations once.
3. A number of pages of 30 stored-state flip flops which can be grouped to emulate counters and shift registers, or used singly as 'flags' to remember the state of the machine, or in logic equation reduction. The SBA addressing structure only allows for 30 addresses, but the number of stored states is increased to 120 by having typically 4 pages of 30 each. Two instructions control a 'page counter'. One steps the counter and so changes the page, and the other sets it back to the first or 'home page'.
4. A logic unit which can perform all the possible logic functions of two variables, namely AND, OR, EXCLUSIVE OR and COMPARE, and also negate (invert). The truth tables of the functions are shown in Fig. 2. Any logic system can be described by a set of Boolean equations written with these operators.

   The logic unit always has two inputs and produces one output and there are two types of action.

   (a) One input comes from an input latch or stored state; the second input comes from the top of the stack, and the result is placed on the top of the stack.
   (b) One input comes from the top of the stack; the second input comes from the next location of the stack; and the result is left on the top of the stack.
5. The stack is always involved in logical evaluations, as the top of the stack is always one of the operands to the logic unit. The stack is just a pile of Boolean values and can be imagined as a vertical shift register in which data is always put into or taken from the top. When data is added to the stack, it is said to be 'pushed' onto the stack. The new data becomes the top of the stack and all the previous data is pushed down the stack by one place. If the opposite is performed, the data in the stack is moved up by one place and the stack is said to be 'popped'. The top of the stack will be lost and the data previously just below the top will become the new top of the stack.

   The data stack in the SBA is normally used as workspace or accumulator and the top of the stack is used in most of the instructions together, sometimes, with the next location down. However, the stack can also be used to store temporary Boolean variables and helps greatly in the evaluation of Boolean equations containing brackets. For example a function such as:

   A. (B.C. + (D.E + F.G).(H.I + J.K))

   would be evaluated in the following way:

Operation	Result
(a) evaluate D.E.	D.E
(b) push into the stack	
(c) evaluate F.G	
(d) OR	D.E+F.G
(e) push into the stack	
(f) evaluate H.I + J.K as in (a)-(d)	
(g) AND	
(h) push into stack	(D.E+F.G).(H.I+J.K)
(i) evaluate B.C	
(j) OR	B.C+(D.E+F.G).(H.I+J.K)
(k) AND the stack with A	Final result.

   Naturally this is not the only way the stack can be used, the variation being limited only by the imagination.
6. A set of up to 30 output buffers which have their new values stored in them as the Boolean equations are evaluated. When all the equations are complete, at the end of a program cycle, the data on the output buffers is relatched into the output drivers connected to the system being controlled. In this way the external outputs of the SBA are updated once per cycle and remain unchanged until the end of the next complete evaluation of the Boolean equations.

F. CONTROL LOGIC

As well as the major functional blocks described above, the SBA contains some simple control logic which operates transparently to the user. At the end of a complete program cycle, the following actions are performed:

(a) the contents of the output buffers are relatched into the outputs
(b) the top of the stack is set to a logic 1
(c) the page counter is set to the home page
(d) new inputs are latched
(e) the program address counter is set to point at the first term of the first Boolean equation.

Once the SBA has started a program cycle, the program address counter is simply incremented every SBA clock cycle, the instruction read out and acted upon.

AND

A	B	RESULT
0	0	0
0	1	0
1	0	0
1	1	1

Output true only if both inputs true.

OR

A	B	RESULT
0	0	0
0	1	1
1	0	1
1	1	1

Output true if either input true.

EXCLUSIVE OR

A	B	RESULT
0	0	0
0	1	1
1	0	1
1	1	0

Output true when inputs differ

COMPARE

A	B	RESULT
0	0	1
0	1	0
1	0	0
1	1	1

Output true when inputs compare.

Fig. 2 LOGIC FUNCTIONS

G. INPUT/OUTPUTS

The addressing capability of the SBA allows for 30 inputs and 30 outputs. There are 30 pins available as Input/Outputs and so if more than 30 total inputs and outputs are used they must be multiplexed.

There is a mask programmable option on each of the 30 pins to allow them to be inputs, outputs or multiplexed input/outputs. Regardless of the option, the internal addressing of the pins remains the same and so, for example, if an application requres only one input and the board layout requires it to be the last pin the program must use address 30.

Input

When programmed as an INPUT,nothing will be able to be output from the pin even if the program loads something in the respective output buffer.

Output

When programmed as an OUTPUT, the input data path is still connected and the value on the pin will be latched with all the other inputs at the appropriate time. This fact can be utilized as follows:

(a) It is sometimes required that the value of an output is used in the processing during the following cycle and would normally have to be copied into a Stored State. Feeding an output back as an input in this way avoids this problem and can also be used as a limited supply of extra stored states, if spare pins are available, that can also be read outside the chip.

(b) As well as reading the value of the output directly, the output can be modified by making use of the open drain construction of the output driver. The value of the output can be modified by an externally connected active pull-down device and the result read into the input. Something like a manual override would be a simple use of this facility while more complex logic functions can also be easily performed.

Multiplexed Input/Output

For complete separation of inputs and outputs the MULTIPLEXED facility must be used although external logic must be used for demultiplexing.

Output Drive Capability

The Output drivers have an impedance of 100 Ohms and are nominally rated at a sink current of 7mA. Thus each output can drive 2 TTL loads plus a 10 KOhm pull-up resistor to +5V.

The nominal current rating is determined by the total allowable power dissipation in the output circuits, which is a maximum of 150mW. The 7mA rating has been determined assuming all 30 outputs are being used. If less than the maximum are in use, the current rating for each can be increased up to the maximum rating of 20mA, keeping within the 150mW power restriction. Fig. 3 gives a guide to the current capacity for different numbers of outputs in use.

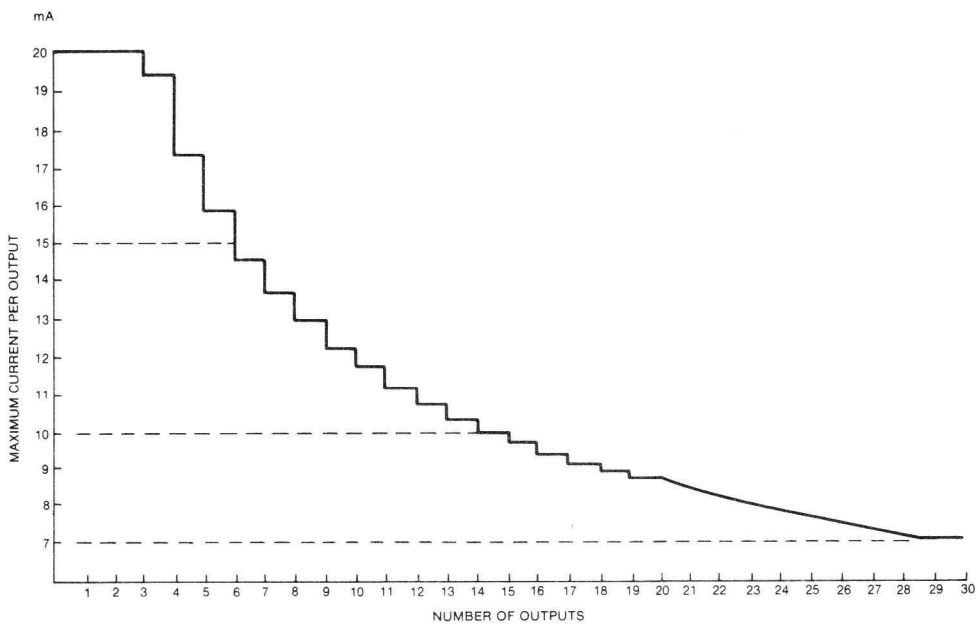


Fig. 3

H. DEVICE TIMING

The clock can be generated internally with the help of an external R/C network connected to the three 'clock' pins, or an external clock can be applied to the clock input.

The SBA will perform the instructions in the ROM, one per clock cycle, until the end of program is reached. At this point a special sequence is performed that is shown in Fig. 4.

The possible variations are due to separate or multiplexed inputs/outputs and the use of HALTED and GO.

Input Timing

Inputs are strobed into the device once per program cycle, as shown in Fig. 4, whether they are exclusive inputs or multiplexed.

Output Timing

If a pin is dedicated to the output function, then the logic level remains constant throughout the program and is updated at the end of each cycle as shown in Fig. 4.

In a multiplexed I/O the output data is present for two clock cycles at the end of each program cycle, the I/O control providing a strobe so the data can be stored in an external device (on the negative edge).

Modes of Operation

1. If the SBA is required to cycle continuously the GO input will be true. In this case there will be one clock cycle between I/O control disappearing and the SPA strobing the inputs. This is the more common mode of operation.

2. If GO is not present after the I/O control goes high, the HALTED output will appear and the SBA will stop. When GO becomes true, HALTED will be removed and the SBA will continue by latching a new set of inputs. Although this mode can be useful it is usually better to put the control into the program itself and run continuously.

Cycle Times

Since all instructions have been arranged to take the same time, the total time taken for a complete program cycle is the time for 1 clock cycle multiplied by the total number of instructions in the program (including RESTART) plus 6 (for the end of cycle sequence). If the cycle is stopped by removing GO, the time can be up to 1 clock cycle less. Thus the maximum possible cycle time is:

Clock period x (1023 + 6) = 1.28625ms at 800kHz
= 10.29ms at 100kHz

In general we have:

$$\frac{\text{no. of instructions} + 6}{\text{clock frequency in kHz}} = \text{program cycle time in ms.}$$

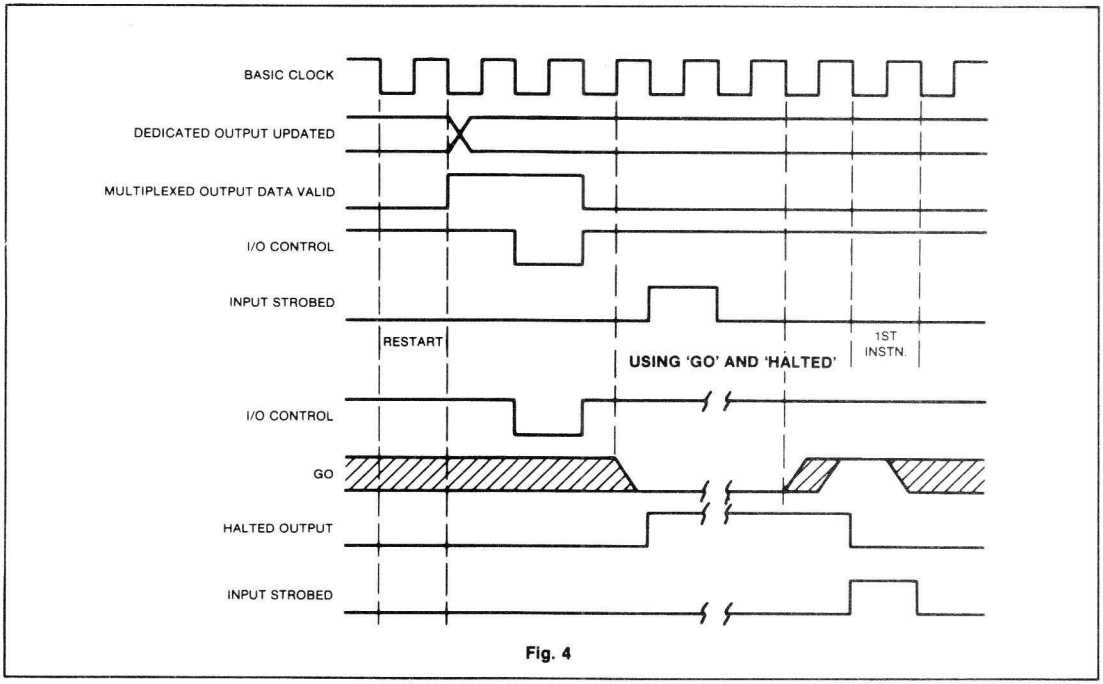


Fig. 4

I. BOOLEAN EQUATION CODES

In order to make the best use of the space available for memory, the codes representing the Boolean operations should be as efficient as possible.

An 8 bit word is used for each instruction code. 5 bits provide an address for the inputs, outputs or stored states, two of the 32 available addresses being reserved for addressless instructions.

The remaining 3 bits of the code enables a total of 24 instructions to be made available.

The 8 bit binary word is conveniently represented by 3 octal (radix 8) digits ranging from 0 to 377 (00 000 000 to 11 111 111 binary). The least significant 3 binary digits are treated as the instruction, and the 5 most significant bits as the address. Addresses 1 to 36 (octal) represent the 30 addresses required throughout the SBA (1-30 in decimal). Addresses 0 and 37 (all 0's and all 1's binary) are reserved for instructions as shown in Fig. 5.

Memory Code in OCTAL		MNEMONIC	Functional Description of Code
01 to 36	0	ANDIN	This input specified by the address is ANDed with the top of the stack.
01 to 36	1	NANDIN	The logical inverse of the input specified by the address is ANDed with the top of the stack.
01 to 36	2	ANDSS	The stored state specified by the address* is ANDed with the top of the stack.
01 to 36	3	NANDSS	The logical inverse of the stored state specified by the address* is ANDed with the top of the stack.
01 to 36	4	ASPI	The stored state specified by the address* is ANDed with the top of the stack, then a 1 is pushed onto stack.
01 to 36	6	NASPI	The inverse of the stored state specified by the address* is ANDed with the top of the stack then a 1 is pushed onto stack.
01 to 36	5	STORE	The value on top of the stack is stored in the stored state specified by the address* and a logical 1 left on the stack.
01 to 36	7	OUTPUT	The value on top of the stack is stored in the output buffer specified by the address and a 1 left on the stack.

Memory Code in OCTAL	MNEMONIC	Functional Description of Code
000	RESTART	Restart evaluation of equations
001	INVERT	Invert top of stack
002	PAGE	Change Page
003	HOME	Back to Home Page
004	PUSH 0	Push logic 0 onto stack
005	PUSH 1	Push logic 1 onto stack
006	PUSH C	Push and copy top of stack
007	POP	Pop the stack
370	AND	Perform the function on the top two locations of the stack. Store result on top of stack.
371	OR	
372	COMP	
373	EXOR	
374	PAND	Perform the function on the top two locations of the stack. Push result into stack leaving logic 1 on top
375	POR	
376	PCOMP	
377	PEXOR	

*The address of a stored state defines 1 of 30 on the currently enabled page.

Fig.5 BOOLEAN EQUATION CODES

Description of Codes.

The codes used for defining the Boolean equations fall into four categories:

(a) single operand instructions which affect the stack
(b) logical operations taking inputs from the stack and storing the result on the stack
(c) data transfer instructions for inputs, stored states, and outputs
(d) program control instructions.

Category (a) — stack manipulation (See Fig. 6):

1. Invert top of stack. The Boolean value is taken from the top of the stack and replaced by its logical inverse; a 1 becomes a 0, and a 0 becomes a 1. The stack is neither pushed or popped.
2. Push 0 onto stack. All data values on the stack are pushed down one place and a logic 0 entered on top of the stack.
3. Push 1 onto stack. All items in the stack are pushed down one place and a logic 1 put on the top.
4. Push and Copy top of stack. Data is moved down the stack and the previous top of stack (now the next position down) is copied to the top.
5. Pop the stack. All data values are moved up the stack one place. The old top of stack is lost.

Category (b) — logical operations (See Fig. 7):
There are two types here, a logical function (AND, OR, EXOR, COMP) and the function followed by PUSH:

1. AND, OR EXOR, COMP. The top two elements of the stack are propped into the logic unit, the logical function is performed on them, and the result pushed back onto the stack.
2. AND-PUSH, etc. The top two values on the stack are popped into the logic unit, the appropriate function is performed on them, the result is pushed onto the stack, and this is followed by a logical 1. This form of logical operation is used when the result is to be saved in the stack for subsequent processing. The 1 is put onto the stack to make it ready for further evaluations.

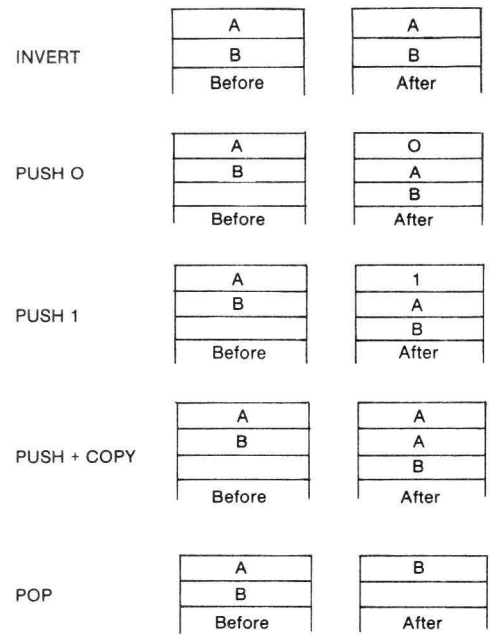
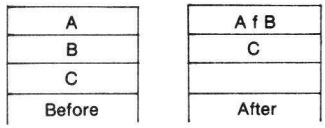


Fig.6 STACK MANIPULATION

TOP OF STACK = A function B, where function = AND, OR, EXCLUSIVE OR, COMPARE:



In the case of AND PUSH, OR PUSH, EXCLUSIVE OR-PUSH, COMPARE-PUSH:

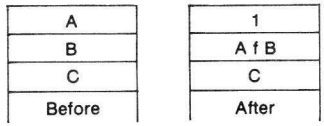


Fig.7 LOGICAL OPERATIONS

STORE A;

Before	After
B	1
C	C

The value of B on the top of the stack is stored in stored state of address A and replaced by a logical 1.

OUTPUT A;

Before	After
B	1
C	C

The value of B on the top of the stack is stored in output buffer of address A and replaced by a logical 1.

Fig.8 OUTPUT OPERATIONS

ANDIN A;
ANDSS A;

Before	After
B	A • B
C	C

NANDIN A;
NANDSS A;

Before	After
B	$\overline{A}$ • B
C	C

ANDSS - A;
PUSH 1

Before	After
B	1
C	A • B
	C

NANDSS - A;
PUSH 1

Before	After
B	1
C	$\overline{A}$ • B
	C

Fig.9 INPUT OPERATIONS

Category (c) — input/output operations (See Figs. 8 and 9): These instructions have two parts, the command and the address. The command defines the data path (input-stack, stored state-stack, stack-stored state or stack-output) and the logical operation to be performed, if any. The address defines which of the 30 pieces of data is to be manipulated.

STORE and OUTPUT take the logic value from the top of the stack and transfer it to the approprite stored state or output buffer, the top of the stack being replaced by a logical 1 ready for the next evaluation.

ANDIN takes the value of the addressed input and ANDs it with the top of the stack.

NANDIN takes the logical inverse of the addressed inputs and ANDs it with the top of the stack.

ANDSS takes the value of the addressed stored state and ANDs it with the top of the stack.

NANDSS takes the logical inverse of the addressed stored state and ANDs it with the top of the stack.

In the above four operations, the stack is neither pushed nor popped.

ASP1 takes the value of the addressed stored state, ANDs it with the top of the stack, and pushes 1 onto the stack.

NASP1 takes the logical inverse of the addressed stored state, ANDs it with the top of the stack, and pushes 1 onto the stack.

Category (d) — control:

PAGE. There are typically 4 pages of stored states in the SBA, and the instructions reading and writing to and from the stored states only provide an address within the currently enabled page. The PAGE instruction steps the page counter and enables the next page.

HOME. If it is required to enable a page of stored states that has been passed, the HOME instruction causes the page counter to go back to enable the home page.

As an example, if the page counter is currently enabling page 3 and it is required to update a stored state on page 4, the PAGE instruction would be used. If now a stored state on page 2 is required, a HOME instruction will switch back to page 1 and a PAGE instruction will step to page 2.

RESTART. This code is always the last code in the program memory (note that its value is conveniently all zeros) and when seen by the control logic the following is performed:

1. the contents of the output buffers are relatched to the outputs.
2. a new set of inputs are latched
3. the top of the stack is set to logical 1
4. the page counter is reset to the home page
5. the program address counter is reset to restart the evaluation of Boolean equations.

SBA Development Microcomputer

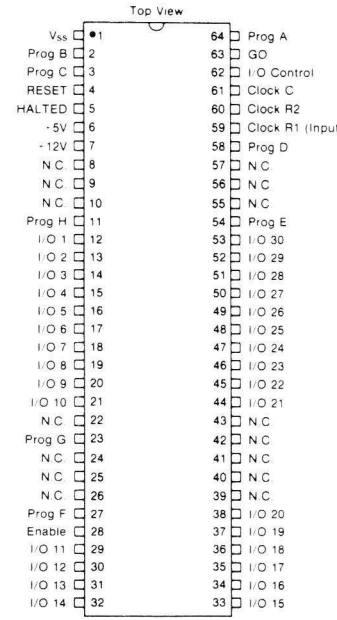
FEATURES

- SBA microcomputer with ROM removed.
- SBA's ROM data lines brought out to pins.
- Useful for engineering prototyping and field trial demonstrations.

DESCRIPTION

The SBA-1 MOS/LSI circuit array is exactly the same as the SBA except for the fact that the program ROM has been removed and all 30 I/O lines are assigned as multiplexed inputs/outputs. The ROM data lines are brought out to pins resulting in the use of a 64 pin package.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



SBA Field Demo System

DESCRIPTION

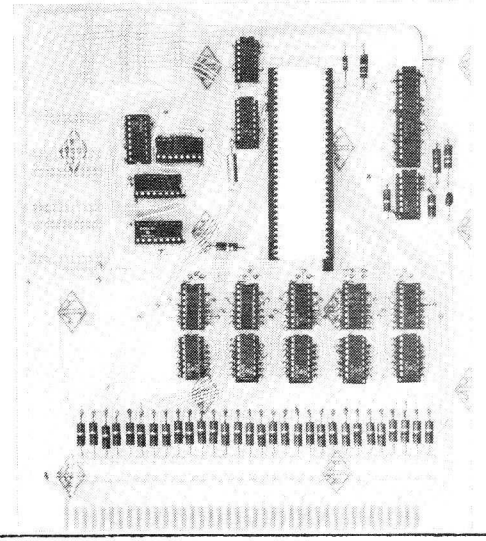
The SBA Field Demo System is used to demonstrate an SBA's capability in the field before committing to a masked ROM. The card contains an SBA-1, a program counter, demultiplexing circuitry, and 5 sockets for 1702A type PROMs.

The program counter is used to address the PROMs sequentially to provide, via the SBA-1's Prog A-Prog H inputs, the instruction sequence to be followed.

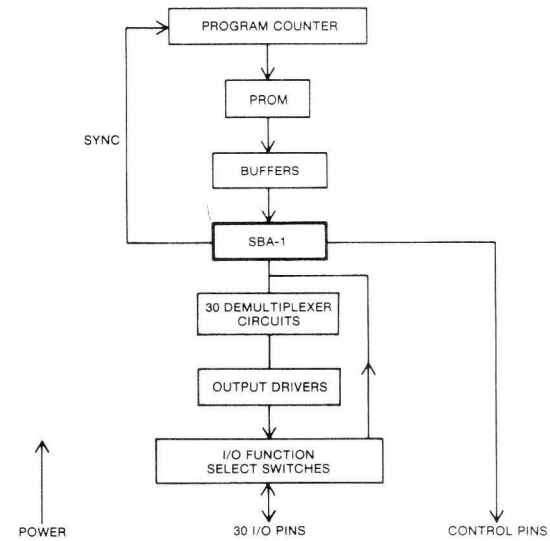
The SBA-1 used has all 30 I/O's multiplexed and demultiplexing circuitry is provided on the SBA-FD board.

The SBA-FD board is 7½"×9" terminated in a 40 pin edge connector (to emulate the SBA's 40 pins) and requires approximately 200mA/−9V for the PROMs, 600mA/+5V for SBA1 and board logic, and 50mA/−12V for the SBA-1 only.

SBA FIELD DEMO CARD



BLOCK DIAGRAM



SBA Compiler

A. DESCRIPTION

SBACOMP is a program which takes as its input a list of Boolean equations and produces the equivalent equations in terms of SBA codes. The output file produced can be used directly with the SBA simulation program SBASIM.

SBACOMP is available in either a Host System version or in CP1600 assembly language for execution on a GIMINI microcomputer system. The following describes the GIMINI version (requires 16K of RAM).

A user develops a set of Boolean equations which define his system and from these equations develops an input file of a special format which is acceptable to SBACOMP. As the Boolean equations can be specified with user defined names for input, output and stored state addresses, the input file can be used as the documentation for the user's system.

Apart from the output of SBA codes a user can request any of the following two options:—

1. the printing, on the user's terminal, of the name tables for inputs, outputs and stored states.
2. the printing, on the user's terminal, of the original equations and the produced (non-optimized) SBA codes.

The final output file is produced once an attempt has been made to optimize the codes without changing the user's logic function. This can save ROM memory.

B. PREPARATION OF INPUT FILE

An input file is made up of seven distinct sections which must all be present. Each line of the file should start in column one (i.e. no preceding blanks are allowed) and should be no longer than 68 characters.

1. Title

The first line should be a title, if it is not the first line the message

"TITLE?"

is printed on the user's terminal but the compiler continues to execute. The six characters T, I, T, L, E and a blank must be present, followed by a user given title which is printed on the user's terminal and output to the output file as a descriptive heading.

The next four sections can be specified in any order but must all be present.

2. Inputs

In this section each user defined input name is associated with an input address. The six characters I, N, P, U, T and S should appear on a line by themselves. When the compiler finds this character string it is then ready to start filling the input name table. Each name should be given on a separate line and can be any combination of the letters A to Z and the digits 0 to 9. A name can have any number of characters but only the first four characters will be significant.

If the name tables are requested by a user, the names printed on the terminal will only be four characters long. A blank line at the end of the section tells the compiler that all the input names have been defined. For example

```
INPUTS
FRED =20
ENGLEBERT =10
LIZ =30
(Blank Line)
```

will associate the name FRED with input address 20, ENGE with input address 10 and LIZ with input address 30. Note that the addresses can be given in any order.

The addresses must be in the range 1 to 30 and the = must be present. The blank terminating line is important. The same name cannot be associated with more than one address and vice versa. If no inputs are used, which is highly unlikely, the INPUTS heading should be present followed immediately by a blank line. Anything after a ; character will be ignored, therefore comments may be put on a line as long as there is a separating ; character. Any line with the character ; in the first column will be completely ignored.

3. Outputs

In this section each user defined name is associated with an output address. The seven characters O, U, T, P, U, T and S should appear on a line by themselves. All the above remarks about INPUTS apply here.

4. Sstates

In this section each user defined stored state name is associated with a stored state address. The stored state names should be defined in pages of up to 30 addresses, maximum 4 pages. At least one page number must be defined and the pages can be defined in any order. The seven characters S, S, T, A, T, E and S should appear on a line by themselves followed on the next line by the six characters 'P', 'A', 'G', 'E', blank and I where $1 \leqslant I \leqslant 4$. For example

```
SSTATES
PAGE 1
TOM = 10
PAGE 2
DICK = 10
(Blank Line)
```

associates the name TOM with stored state 10 on page 1 and the name DICK with stored state 10 on page 2. All the above remarks about INPUTS apply here. If one page is used it must be page 1, if two pages are used they must be page 1, and page 2 etc. Most of the stored states on page 1 should be used before page 2 is used.

Note that because a stored state can appear on either side of an equation no output can have the same name as a stored state and no input can have the same name as a stored state. However, an input and an output can have the same name, because an output can only appear on the left hand side of an equation and an input can only appear on the right hand side of an equation. This greatly facilitates coding of SBA systems having outputs directly connected to inputs. All stored state names must be unique, i.e. a stored state on page 1 cannot have the same name as a stored state on page 2.

5. Symbols

An equation is a string of variable names separated by symbols which indicate the operations to be carried out on the variables.

There is a set of ten acceptable symbols, four of which a user can define himself. The four symbols are those representing the four standard Boolean operators AND, OR, EXCLUSIVE—OR and COMPARE. The eight characters S,Y,M,B,O,L,S and blank must be present followed by the four symbols each separated by a character (comma or blank). For example

SYMBOLS • + !*

indicates that the operator AND is represented by •, the operator OR is represented by +, the operator EXCLUSIVE—OR is represented by ! and the operator COMPARE is represented by *. The symbols must appear in this order. If this line is interpreted wrongly by the compiler the produced SBA codes will be absolute rubbish. To avoid this situation, the compiler prints its interpretation of this line on the user's terminal. For example

AND = .
OR = +
EXOR = !
COMP = *

If there has been any mis-interpretation it can be seen immediately and the program aborted.

The other six symbols are right hand parenthesis), left hand parenthesis (, equals =, not −, a comment indicating symbol ; and an equation continuation symbol /.

If there are any errors in the input file up to this point the program will abort here.

6. Equations

In this section the system equations, which should be expressed as SUMS OF MINTERMS and then simplified as far as possible, are entered. When a variable is negated the NOT symbol should come on the left hand side of the variable name. For example NOT A should be written —A. If an equation needs more than one line the symbol / should terminate each line to show that the equation is continued on the next line. Any information after the symbol ; will be treated as comment and ignored.

Any line with a ; in the first column will be treated as a comment and ignored. Blanks within an equation are ignored, there should always be one = symbol in an equation and the number of left hand parentheses should match the number of right hand parentheses.

In evaluating an equation the symbols are given priorities, those with the highest priority being processed first.

Highest Priority : any expression enclosed in parentheses
: NOT symbol
: AND symbol
Lowest Priority : OR, EXCLUSIVE—OR and COMPARE symbols

In the case of symbols of equal precedence the symbols are processed from left to right.

Each equation should start on a new line.

Two special purpose names, STAK and SAVE are built into the compiler. They should be used when the new values of a group of equations are not required until the whole group has been evaluated. Using STAK the new values can be pushed on the stack until required then be popped off the stack using SAVE.

For example if A = B + C and B = −A + C the necessary equations would be

STAK = B + C
STAK = −A + C
"
"
B = SAVE
A = SAVE

−STAK and −SAVE are not allowed and no user variable name should start with the characters STAK or SAVE. STAK should only appear on the left hand side of an equation and SAVE should only appear on the right hand side of an equation.

Notes on Equations

1. A single entity should never be enclosed in parenthesis, eg A = −(B) is completely unnecessary, A = −B is correct. A = −B will produce more efficient code than −A = B.
2. If a pin is permanently 1 the necessary equation could be coded A = X + $\overline{X}$ or the pin could be hardwired to a 1. If a pin is permanently 0 the necessary equation could be coded A = X • $\overline{X}$ or the pin could be hardwired to a 0.
3. If two or more outputs have the same defining equation, a temporary stored state could be used to hold the value of the equation and then this stored state value could be outputted to the various outputs. For example if A = E • H, B = E • H and C = E • H where A, B and C are outputs then the equations could be coded

   X = E • H
   A = X
   B = X
   C = X where X is a stored state.

   If however, A was a stored state the equations could be coded

   A = E • H
   B = A
   C = A
4. If two or more equations contain a common term, a temporary stored state could be used to hold the value of the common term and then this stored value could replace the common term in each equation. For example if A = D + E • H, B = F • E • H and C = G + E • H then the equations could be coded

   X = E • H
   A = D + X
   B = F • X
   C = G + X where X is a stored state.
5. If a minterm contains a parenthesized sub-function, this minterm should be written with the sub-function as its first term as this produces more efficient code. For example A = B • C • (D f E) should be written

   A = (D f E) • B • C

Limitation

There should be no more than 15 STAK equations in any one group, i.e. before a group of SAVE equations.

7. End

The characters E, N and D should appear on a line by themselves immediately after the last equation.

This section indicates the physical end of the input file. No user defined variable name should start with the characters E, N and D.

See Appendix A for an example input file.

C. OUTPUT FROM THE COMPILER

The output file of SBA codes produced by the compiler can be used directly with the SBA simulation program SBASIM.

The user defined title is the first line of the output file, this enables a user to keep track of his output files. If requested, the name tables for inputs, outputs and stored states will be printed on a user's terminal. All 30 of the input, output and stored state (4 pages) names are printed.

If an element was not used its place in the tables will be blank. It is often useful to obtain a print out of the name tables without actually processing the equations. This can be achieved by setting an option, see operating instructions.

The SBA codes are produced by processing one equation at a time. If requested the original equation and the equivalent SBA

codes are printed on a user's terminal as the compiler translates the equations. When all the equations have been translated the compiler checks to see that all defined inputs, outputs and stored states have been used in the equations. If some of the variables have not been used some of the following warning messages will be printed on a user's terminal.

"INPUT_____NOT IN ANY EQUATION"
"OUTPUT_____NOT IN ANY EQUATION"
"NO RHS USE OF SSTATE____"
"NO LHS USE OF SSTATE____"

The messages indicate possible errors and a user should take the necessary action. They do not affect the creation of the SBA codes. The compiler continues to run from here and next prints the message.

"X INSTS IN PROG"

on a user's terminal, where X is a positive integer.

The compiler then looks at the SBA codes to see if they can be optimized. If they cannot be optimized the message

"PROG CANNOT BE OPTIMIZED"

will be printed. If the codes can be optimized the message

"X INSTS IN OPTIMIZED PROG"

will be printed. If any error messages have been printed on a user's terminal then the SBA codes will not be complete and there is no point in producing the output file.

The instructions in the output file should be referred to in the range 0 to 1023.

D. OPERATING INSTRUCTIONS

Once written an input file should be built via the text editor and punched onto paper tape.

To run SBACOMP, the relocatable load module should be read into memory and executed from its entry address. The message:

"GI SBACOMP VOIA"

will be printed followed by the question:

"SRC? (H/L)"

A user should reply "H" if the input file is to be entered via a high speed reader or "L" if it is to be entered via a teletype (low speed) reader. Next the question:

"TABLES? (Y/N/O)"

will be printed. A user should reply "Y" if he wants the input, output and stored state name tables printed on his terminal, "N" if he does not require the tables or "O" if he requires only the tables. Next the question:

"EQUATIONS? (Y/N)"

will be printed. A user should reply "Y" if he wants the original equations and the produced SBA codes printed on his terminal or "N" if he does not require the information. A user should always reply "Y" to this question until there are no errors in his input file. This way a user can see the line of input to which an error message refers.

From this point the compiler will start to process the input file, printing out the requested information and any error messages. If there are any errors in the input file between the "TITLE" and "EQUATIONS" headings, SBACOMP will return control to the GIMINI monitor when the latter heading has been reached. When SBACOMP reaches the "END" heading, it will return control to the GIMINI monitor if there were any errors in the equations. If there were no errors in the input file the compiler will ask the question:

"OUTPUT? (H/L/N)"

A user should reply "H" if he wants the output file to be punched on a high speed device, "L" if he wants it punched on a low speed device or "N" if he does not want the output file produced.

If the "EQUATIONS" or "END" heading is missing from the input file, the reader will "hang" when the physical end of the paper tape is reached. A user should press the STOP/START button on the front panel of the GIMINI, set the switch register to 171000, load this into register 7 and then press STOP/START again. This will return control to the GIMINI monitor and SBACOMP can be executed again once the input file has been changed.

The compiler will accept an input file which is split into several tapes as long as there is a Form Feed character at the end of each tape. This form feed character is automatically generated when using the GIMINI Text Editor to create an input file. When the end of one tape is reached the next tape should be loaded and the CTRL/C keys should be pressed. This will initiate the reading of the next tape.

E. ERROR MESSAGES

Unless otherwise stated the errors are fatal.

1) ERROR — "TITLE?" (non-fatal)
   Reason — either the TITLE line is not the first line of the input file or the six characters T, I, T, L, E and blank are in the wrong order.
   Action — insert a new line or correct first line of the input file.

2) ERROR — "INPUTS?"
   "OUTPUTS?"
   "SSTATES?"
   "PAGES?"
   "SYMBOLS?"
   Reason — the indicated heading or headings have been omitted.
   Action — correct input file by inserting the necessary heading or headings.

3) ERROR — "INPUT & SSTATE HAVE SAME NAME_____"
   — "OUTPUT & SSTATE HAVE SAME NAME_____"
   Reason — self explanatory.
   Action — change one of the names, making sure that the equations are correspondingly changed.

4) ERROR — " = NOT FOUND"
   Reason — an = was not found in a name defining line.
   Action — correct erroneous line, which is printed out after the error message.

5) ERROR — "ILL ADDR"
   Reason — an address is out with the range $1 \leqslant$ Address $\leqslant 30$.
   Action — correct erroneous line, which is printed out after the error message.

6) ERROR — "DUP ADDR"
   Reason — an attempt to associate the same address with more than one name.
   Action — correct address in erroneous line, which is printed out after the error message.

7) ERROR — "DUP NAME"
   Reason — an attempt to associate the same name with more than one address.
   Action — correct name in erroneous line, which is printed out after the error message.

8) ERROR — "ILL CHAR"
   Reason — a character which is neither a letter of the alphabet, a digit nor one of the legal symbols has been found.
   Action — correct erroneous line, which is printed out after the error message.

9) ERROR — "VAR_____NOT IN TABLES"
   Reason — a user defined name has appeared in an equation but has not been defined in the input, output or stored state tables.

Action — either add the variable name to the tables or correct the name in the indicated equation.

10) ERROR — "INPUT ON WRONG SIDE OF ="
— "OUTPUT ON WRONG SIDE OF ="
Reason — internal transfer of information to inputs or from outputs is not possible.
Action — correct indicated equation or input/output name.

11) ERROR — "MIS-MATCHED PARENTHESES"
Reason — self explanatory
Action — correct indicated equation.

12) ERROR — "MISSING ="
Reason — self explanatory
Action — correct indicated equation.

13) ERROR — "ILL SYNTAX"
Reason — (a) −STAK or −SAVE
(b) STAK on right hand side of an equation
(c) SAVE on left hand side of an equation
(d) more than one = symbol
(e) no variable name before the = symbol
(f) another symbol, other than a leading − symbol, before the = symbol (−A • B = C + D)
(g) an illegal combination of symbol—symbol, symbol—variable, variable—symbol or variable—variable.
Action — correct indicated equation.

Note:

All variable—variable combinations are illegal.
Illegal variable—symbol combination are A− and A(.
The illegal symbol—variable combination is)A.
There are 19 legal symbol—symbol combinations.
Let • = AND, + = OR, ! = EXOR and * = COMP.
The legal combinations are then

1.).
2.)+
3.)!
4.)*
5.);
6.))
7. •−
8. +−
9. !−
10. *−
11. =−
12. (−
13. ((
14. •(
15. +(
16. !(
17. *(
18. =(
19. −(

Due to limited storage space certain arrays within the compiler have been restricted to a certain size. Any of the following three error messages may appear, indicating that a certain array is not large enough.

14. ERROR — "SOURCE FULL"
15. — "S OR V STACK FULL"
16. — "ROM FULL"
Reason — above
Action — for 14 and 15 breaking down the indicated equation into more than one equation will help or consult your programming staff who can enlarge the necessary arrays.

The following two error messages are system errors and indicate an error within the compiler. Please notify the appropriate personnel if they should occur.

17. ERROR — "CORRUPT ADDRESS"
18. ERROR — "S OR V STACK UNDERFLOW"

F. EXAMPLE OF A BINARY DECADE COUNTER

The equation for a binary decade counter can be minimized to:—

$$W_{n+1} = W_n \bullet A + X_n \bullet B$$
$$X_{n+1} = X_n \bullet (A + \overline{Y_n}) + \overline{X_n} \bullet B$$
$$Y_{n+1} = Y_n \bullet A + \overline{W_n} \bullet \overline{Y_n} \bullet Z_n \bullet C_1$$
$$Z_{n+1} = Z_n \,!\, C_1$$
$$C_2 = W_n \bullet Z_n \bullet C_1$$

Where $A = \overline{C_1} + \overline{Z_n}$, $B = Y_n \bullet Z_n \bullet C_1$, C_1 is the carry in and C_2 is the carry out.

Let C be an input, A,B,W,X,Y and Z be stored states and C_2 be an output. The input file would look like the following:

```
TITLE DECADE COUNTER

INPUTS
C1 = 1 ; CARRY IN

OUTPUTS
C2 = 1 ; CARRY OUT

SSTATES
PAGE 1
W = 1
X = 2
Y = 3
Z = 4
PAGE 2
;
; PAGE 2 IS BEING USED FOR DEMONSTRATION
; NORMALLY PAGE 1 WOULD STILL HAVE BEEN USED
;
A = 1
B = 2

SYMBOLS • + ! *
EQUATIONS
;
; A AND B ARE TERMS COMMON TO SEVERAL EQUATIONS
;
A = −C1 + −Z
B = Y • Z • C1
STAK = A • W + X • B; PUSH ON STACK
STAK = X • (A + −Y) + B • −X; PUSH ON STACK
STAK = Y • A + −W • −Y • Z • C1; PUSH ON STACK
STAK = Z ! C1; PUSH ON STACK
C2 = W • Z • C1
Z = SAVE; POP OFF STACK
Y = SAVE; POP OFF STACK
X = SAVE; POP OFF STACK
W = SAVE; POP OFF STACK
END
```

In this example the new values of W,X,Y and Z are pushed onto the stack until all the equations have been evaluated. Note that there is no need to push the last equation of the group onto the stack. Note also that a blank comment line before and after the actual comment line makes the comment stand out clearly. The output from the compiler would look like the following:—

```
S160DM V01B
$
 LH0
INIT ADDR 000000
FINL ADDR 023754
ENTR ADDR 000000
$E0

GI SBACOMP V01A
SRC? (H/L):H
TABLES? (Y/N/O):Y
EQUATIONS? (Y/N):Y
        DECADE COUNTER
PAGE 1
PAGE 2
AND  = •
OR   = +
EXOR = !
COMP = *
```

	INPUTS	OUTPUTS	STORED STATES				OCTAL
			PAGE 1	PAGE 2	PAGE 3	PAGE 4	
1	C1	C2	W	A			1
2			X	B			2
3			Y				3
4			Z				4
5							5
6							6
7							7
8							10
9							11
10							12
11							13
12							14
13							15
14							16
15							17
16							20
17							21
18							22
19							23
20							24
21							25
22							26
23							27
24							30
25							31
26							32
27							33
28							34
29							35
30							36

```
A AND B ARE TERMS COMMON TO SEVERAL EQUATIONS

A = -C1 + -Z
045,011,371,002,016,
B = Y.Z.C1
003,042,032,010,002,026,
STAK = A.W + X.B; PUSH ON STACK
003,012,002,012,005,022,003,022,371,005,
STAK = X. (A + -Y) + B.-X; PUSH ON STACK
035,002,012,371,003,022,005,023,002,022,
371,005,
STAK = Y.A + -W.-Y.Z.C1; PUSH ON STACK
012,003,032,005,033,013,042,010,371,005,
STAK = Z ! C1; PUSH ON STACK
044,010,373,005,
C2 = W.Z.C1
042,012,010,017,
Z = SAVE; POP OFF STACK
077,046,
Y = SAVE; POP OFF STACK
007,036,
X = SAVE; POP OFF STACK
007,026,
W = SAVE; POP OFF STACK
007,016,
000,
END

60 INSTS IN PROG
53 INSTS IN OPTIMISED PROG
OUTPUT? (H/L/N) :H

S160DM V01B
$
```

The following is a listing of the output file produced.

```
C       DECADE COUNTER
045,011,371,002,016,003,042,032,010,002,
026,003,012,002,014,022,003,022,375,035,
002,012,371,003,024,023,002,022,375,012,
003,034,033,013,042,010,375,044,010,377,
042,012,010,017,007,046,007,036,007,026,
007,016,000,
END
```

SBA Simulator

A. DESCRIPTION

SBASIM is a program which simulates the action of the "SEQUENTIAL BOOLEAN ANALYZER" where there are 30 inputs, 30 outputs, 30 output buffers and 4 pages, each of which has 30 stored states.

SBASIM is available in either a Host System version or in CP1600 assembly language for execution on a GIMINI microcomputer system. The following describes the GIMINI version.

A user develops a set of Boolean equations which defines the system and then codes these equations into a series of instructions which makes up the user program. SBASIM reads the user program from a paper tape and stores the instructions sequentially in the ROM. The ROM has 200 locations to allow for inefficient coding at the development stage of a system. The ROM locations are addressed from 0 to 1999.

A user first sets the initial conditions of the outputs, stored states and inputs of his system. SBASIM is then ready to accept a series of commands (see Simulator Commands), by which a user can control the simulation of the program.

During a simulation SBASIM cycles sequentially through the ROM decoding an instruction simulating its action and then continuing onto the next instruction. The X command should be used to terminate a simulation.

B. PROGRAM PREPARATION

Hand Coding Equations

First define the system to be simulated by developing a set of Boolean equations to describe it. The resulting equations should then be translated into SBA codes (see Appendix A for codes).

The program will be a string of 3 digit octal instructions separated by commas, maximum 18 instructions per line. The last instruction of a line should always be followed by a comma. Comment lines, which must begin with the character C, may be inserted anywhere in the program.

RESTART (code 000) should always be the last instruction of a program. If the instruction is not present SBASIM will superficially insert the instruction into the user program. If a user gives the "PUNCH" command the RESTART instruction will appear on the output tape, if the final address was requested.

END should be the last line of a program. If END is not present SBASIM will continue to look for data and will have to be interrupted by the return to monitor sequence.

A program once written should be punched onto paper tape with as many comments as possible to aid testing.

SBA Compiler

The SBA Compiler is a program which takes as its input a list of Boolean equations and produces the equivalent equations in terms of SBA Codes. Either of the two files produced by the SBA Compiler can be used directly with SBASIM, eliminating the need for hand coding the Boolean equations. The equations can be specified with user defined names for input, stored state and output addresses and therefore can be used as the documentation for the system.

C. SETTING THE INITIAL CONDITIONS

When SBASIM is first run a user is requested to set the initial conditions of the outputs, stored states and inputs. The first request will be:

"HOW MANY OUTPUTS?"

to which a user should reply with a number lying between 1 and 30. If no outputs are used, which is highly unlikely, one dummy output should be used.

Once the number of outputs has been accepted the message

"INITIAL OUTPUTS"

will be printed, in response to which the initial value of each output either a 1 or 0 should be typed. If a dummy is used it should be set to 0.

When the initial outputs have been accepted SBASIM then asks

"HOW MANY PAGES?"

to which a user should reply with a number lying between 1 and 4, page 1 must always be used. The next question will be

"HOW MANY SSTATES ON PAGE 1"

a user should reply with a number lying between 1 and 30. If no stored states are used a dummy should be defined. Once the number of stored states has been accepted the message

"INITIAL SSTATES ON PAGE 1"

will be printed. The response is the same as for outputs. The process is repeated until all the used pages of stored states have been defined. In order to keep the number of instructions in a program to a minimum all or most of the stored states on one page should be used before defining another page.

The next question asked will be

"HOW MANY INPUTS?"

a user should reply with a number lying between 1 and 30. If no inputs are used a dummy should be defined. If an initial value is set wrongly or a wrong number of outputs etc., is entered a user must complete the initialization of all the variables, then using the INIT command start again.

The number of outputs etc., must be equal to the highest address used, e.g. if output 1,3 and 10 are used then the number of outputs used should be entered as 10 and the unused addresses set to 0.

D. SIMULATOR COMMANDS

Once the initialization is complete SBASIM is ready to accept a command. The message "COMMAND?" is printed to which a user should reply with one of the following commands. If a command is unrecognized or contains an error a "?" is printed followed by another command prompt. No line typed by a user can be longer than 72 characters.

1. Command — ?
   Description — Display command summary.
2. Command — PI
   Description — PRINT INPUTS, the line printed will be "INPUTS = AA - - A" where A is a binary digit and the number of A's will be the number of inputs defined at the initialization stage.

3. Command — PO
   Description — PRINT OUTPUTS, the line printed will be "OUTPUTS = AA - - A" where A is a binary digit and the number of A's will be the number of outputs defined at the initialization stage.
4. Command — PB
   Description — PRINT BUFFERS, the line printed will be "BUFFERS = AA - - A" where A is a binary digit and the number of A's will be the number of outputs defined at the initialization stage.
5. Command — P1, P2, P3 or P4
   Description — PRINT A PAGE OF STORED STATES, the line printed will be "PAGE X = AA - - A" where $1 \leq X \leq 4$, A is a binary digit and the number of A's will be the number of stored states for page X defined at the initialization stage.
6. Command — PS
   Description — PRINT STACK, the line printed will be "STACK = AA - - A" where A is a binary digit and the number of A's is the current level of the stack, the top of stack being the digit furthest to the right.
7. Command — PD
   Description — PRINT DEPTH, the line printed will be "DEPTH = I" ($1 \leq I \leq 16$) where I is the maximum depth to which the stack has been pushed during the execution of a program.
8. Command — PA(GE) i.e. only PA is required.
   Description — PRINT CURRENT PAGE NUMBER, the line printed will be "CURRENT PAGE = I" ($I \leq I \leq 4$). This command helps a user to keep track of which stored state is being used at any one point of a simulation.
9. Command Lda
   Description — LOAD the paper tape containing the SBA codes into the ROM from device d (d = H for high speed, d = L for low speed) starting at address "a" ($0 \leq a \leq 1999$). When a tape has been read in the messages "INIT ADDR - - -" "FINAL ADDR - - -" will be printed.
10. Command — Pda, b
    Description — PUNCH the contents of the ROM on device d (d = H for high speed, d = L for low speed) from address a to b inclusive ($0 \leq a, b \leq 1999$).
11. Command — Bn, a
    Description — Set program breakpoint n ($0 \leq n \leq 7$) at ROM address a ($0 \leq a \leq 1999$). A maximum of 8 breakpoints is allowed. A simulation can be stopped at address "a" so that the other simulator commands can be used to investigate the status of the SBA to help with debugging of user programs.
12. Command — Bn
    Description — Reset program breakpoint n ($0 \leq n \leq 7$).
13. Command — B
    Description — Reset all program breakpoints.
14. Command — C(ONT)
    Description — CONTINUE program execution from the current breakpoint. When a breakpoint address is reached that address is not executed until the next "C" command is given. The message "Bn at a" will be printed when a breakpoint address is reached.
15. Command — DB
    Description — DISPLAY currently set BREAKPOINTS. The message "Bn: a" is printed for each set breakpoint. If no breakpoints are set the message "NONE!!" will be printed.
16. Command — Ea
    Description — EDIT/EXAMINE address "a". The message "a = b:" will be printed where a is the address and b is the contents, a 3 digit octal number. A user can change the contents of this address by typing a new 3 digit octal number after the ":". By typing carriage return after the ":" or the new contents the command prompt will be given by typing "/" address a + 1 and its contents will be printed or by typing "-" address a - 1 and its contents will be printed.
17. Command — IN(IT)
    Description — RESET INITIAL CONDITIONS. This command can be used to stop the current simulation and go back to reset the initial conditions. The program counter is reset to point to the first ROM location, the top of the stack is reset to 1 so that a new simulation can begin. Breakpoints, Automatic Print Options Output/Input connections (see later) are not cleared.
18. Command — Gn, aa - - a ("a" is a binary digit).
    Description — Simulate n cycles with the inputs set to aa - - a. The number of inputs should be the number of inputs defined at the initialization stage.
19. Command — X
    Description — EXIT to the GIMINI resident monitor

The following commands will be useful to a user when he becomes more proficient at using SBASIM.

20. Command — SP
    Description — SET AUTOMATIC PRINT OPTIONS. A user can choose to have certain variables printed out automatically at the end of each cycle. Any of the variables INPUTS, OUTPUTS, BUFFER PAGES OF STORED STATES and the STACK may be requested. The command will be of the form SP I, 1, 1, S etc.,
    The possible characters that can be used are I,0,B,1,2,3,4 and S.
21. Command — RP
    Description — RESET AUTOMATIC PRINT OPTIONS. This command will stop the automatic printing of variables which had previously been set. The command will be of the form RP I, O etc.,
22. Command — SC A, B ($1 \leq A, B \leq 30$)
    Description — This command sets an OUTPUT to an INPUT. A is an output address and B is an input address. Only one input and one output can be connected together. If an input or output is connected twice the first connection will be overwritten.
23. Command — RC A, B
    Description — This command resets the connection between OUTPUT A and INPUT B. The message "NO SUCH CONNECTION" will be printed if the given connection is not set or when no connection of OUTPUT A has been made.
24. Command — PC
    Description — PRINT I/O CONNECTIONS. A table of the output addresses connected to input addresses will be printed.
    OUTPUT IS CONNECTED TO INPUT
    A B

The message
"THERE ARE NO I/O CONNECTIONS"
will be printed when no connections are set.

25. Command — IS N, II - - I (I is a binary digit and $1 \leqslant N \leqslant 16$)
Description — INITIALIZE THE STACK.
N is the number of levels of the stack that will be used and each level is set to a value I. The last digit typed will become the new value of the top of the stack. This command will have to be used when a user wants to use values which have been left on the stack during a previous cycle. This command ensures that during the first cycle there is something to pop off the stack.

At the end of each cycle a number is printed indicating which cycle has just been simulated.

E. OPERATING INSTRUCTIONS

To run SBASIM, the relocatable load module should be read into memory and executed from its entry address. The message
"GI SBASIM VOIA"
will be printed followed by the question
"COMMAND SUMMARY? (Y/N)"
to which a user should reply accordingly. Next the initialization sequence will be executed. When this stage is complete the command prompt will be printed and the simulation proper can begin. A simulation can be interrupted while executing cycles by striking console key "C" and the "CTRL" key at the same time. When a user strikes CTRL/C the present cycle is completed and then the command prompt printed.
If when using the "LOAD" or "PUNCH" command the peripheral in question was not ready SBASIM returns control to the GIMINI monitor. A user should enable the peripheral in question and then execute SBASIM from its entry address +2. The system will be in the state in which it was before the aborted "LOAD" or "PUNCH" command was given.
If the END is missing from the input tape, the reader will hang up after the "LOAD" command has been executed. A user should press the STOP/START button on the front panel of the GIMINI, set the switch register to 171000, load this into register 7 and then press STOP/START again. This will return control to the GIMINI monitor and SBASIM can be executed from its entry address +2 The system will have the program in the ROM and the simulation can continue.

F. ERROR MESSAGES

1. Error — "STACK OVERFLOW at N" ($0 \leqslant N \leqslant 1999$).
Reason — an attempt to push the stack beyond its maximum level, the stack has a maximum of 16 levels.
Action — restructure the program to hold temporary or new values in spare stored states instead of the stack.

2. Error — "STACK UNDERFLOW at N" ($0 \leqslant N \leqslant 1999$).
Reason — an attempt to pop a value off the stack when the stack is already empty.
Action — investigate the program around location N. Should the INITIALIZE STACK command have been used?

3. Error — "ROM FULL"
Reason — there are more than 2000 instructions in the program.
Action — this should never happen, as in real life the program will have to fit into a 1K ROM. Restructure the program in an attempt to decrease the number of instructions used.

4. Error — "ILLEGAL CHAR"
Reason — there is a non-octal digit in an instruction on an input tape.
Action — edit the input tape in the area where the reader stopped.

5. Error — "COMMA MISSING"
Reason — a comma must follow every instruction on an input tape.
Action — edit the input tape in the area where the reader stopped.

6. Error — "ADDRESS OUT OF RANGE at N" ($0 \leqslant N \leqslant 1999$).
Reason — the address part of an instruction is not in the range $0 \leqslant I \leqslant 37$ (octal).
Action — use EDIT command on location indicated, INIT and start again.

7 Error — "NO SUCH CONNECTION"
Reason — The RC command has been given for an output which had not been previously connected to any input or the given output/input connection had not been previously set.
Action — None needed.

8. Error — "THERE ARE NO I/O CONNECTIONS"
Reason — the PC command has been given when there are no connections to print.
Action — none needed.

9. Error — "NONE!!"
Reson — the DB has been given when there are no breakpoints to display.
Action — none needed.

G. EXAMPLES ON THE USE OF SBASIM

The equations for a binary decade counter can be minimized to

$$W_{n+1} = W_n \cdot A + X_n \cdot B$$
$$X_{n+1} = X_n \cdot (A + \overline{Y}_n) + \overline{X}_n \cdot B$$
$$Y_{n+1} = Y_n \cdot A + \overline{W}_n \cdot \overline{Y}_n \cdot Z_n \cdot C_1$$
$$Z_{n+1} = Z_n ! C_1$$
$$C_2 = W_n \cdot Z_n \cdot C_1$$

Where $A = \overline{C_1} + Z_n$, $B = Y_n . Z_n . C_1$, C_1 is the carry in and C_2 is the carry out.

For the 1st example let C by input 1, A, B, W, X Y and Z be stored states 8, 9, 1, 2, 3 and 4 of page 1 and C_2^1 be output 1.

Example 1

The SBA codes for the above equations would then look like the following:

Mnemonic	Code	Comments
NASPI Z	045	NAND Z with top of stack, push 1
NANDIN C_1	011	NAND C_1 with top of stack
OR	371	form $\overline{Z}+C_1$ on top of stack
STORE A	106	store top of stack in A
ANDSS Y	032	AND Y with top of stack
ANDSS Z	042	form Y.Z on top of stack
ANDIN C_1	010	form $Y.Z.C_1$ on top of stack
STORE B	116	store top of stack in B
ANDSS W	012	AND W with top of stack
ASPI A	104	form W.A, push 1
ANDSS X	022	AND X with top of stack
ANDSS B	112	form X.B on top of stack
POR	375	form W.A+X.B, push 1 saving new value of W on stack
ASPI A	104	AND A with top of stack, push 1
NANDSS Y	033	NAND Y with top of stack
OR	371	form $A+\overline{Y}$ on top of stack
ASPI X	024	form $X.(A+\overline{Y})$, push 1
NANDSS X	023	NAND X with top of stack
ANDSS B	112	form $\overline{X}.B$ on top of stack
POR	375	form $X.(A+\overline{Y})+\overline{X}.B$, push 1 saving new value of X on stack
ANDSS Y	032	AND Y with top of stack
ASPI A	104	form Y.A, push 1
NANDSS W	013	NAND W with top of stack
NANDSS Y	033	form $\overline{W}.\overline{Y}$ on top of stack

Mnemonic	Code	Comments
ANDSS Z	042	form $\overline{W}.\overline{Y}.Z$ on top of stack
ANDIN C_1	010	form $\overline{W}.\overline{Y}.Z.C_1$ on top of stack
POR	375	form $Y.A+\overline{W}.\overline{Y}.Z.C_1$, push 1 saving new value of Y on stack
ASPI Z	044	AND Z with top of stack, push 1
ANDIN C_1	010	AND C with top of stack
PXOR	377	form Z!C, push 1 saving new value of Z on stack
ANDIN C_1	010	AND C_1 with top of stack
ANDSS Z	042	form $Z.C_1$ on top of stack
ANDSS W	012	form $W.Z.C_1$ on top of stack
OUTPUT C_2	017	output top of stack to C_2
POP	007	pop the stack
STORE Z	046	store top of stack in Z
POP	007	pop the stack
STORE Y	036	store top of stack in Y
POP	007	pop the stack
STORE X	026	store top of stack in X
POP	007	pop the stack
STORE W	016	store top of stack in Y
RESTART	000	restart cycle

Note that the POP instructions are necessary because the OUTPUT and STORE instructions leave a 1 on the top of the stack.

For the second example let W_n, X_n, Y_n, Z_n and C_1 be inputs 1, 2, 3, 4 and 5, A and B be stored states 1 and 2 and $W_{n+1}, X_{n+1}, Y_{n+1}, Z_{n+1}$ and C_2 be outputs 1, 2, 3, 4 and 5. To make the counter work outputs 1, 2, 3 and 4 can be connected to inputs 1, 2, 3 and 4. This will overwrite those inputs given by the user at the start of each cycle.

Example 2

The SBA codes for the above equations would then look like the following:

Mnemonic	Code	Comments
NANDIN Z_n	041	NAND Z_n with top of stack
PUSH 1	005	push 1 onto stack
NANDIN C_1	051	NAND C_1 with top of stack
OR	371	form $\overline{Z}_n+\overline{C}_1$
STORE A	016	store top of stack in A
ANDIN Y_n	030	AND Y_n with top of stack
ANDIN Z_n	040	form $Y_n.Z_n$
ANDIN C_1	050	form $Y_n.Z_n.C_1$
STORE B	026	store top of stack in B
ANDIN W_n	010	AND W_n with top of stack
ASPI A	014	form $W_n.A$, push 1
ANDIN X_n	020	AND X_n with top of stack
ANDSS B	022	form $X_n.B$
OR	371	form $W_n.A+X_n.B$
OUTPUT W_{n+1}	017	output to top of stack to W_{n+1}
NANDIN X_n	021	NAND X_n with top of stack
ASPI B	024	form $\overline{X}_n.B$, push 1
ASPI A	014	AND A with top of stack, push 1
NANDIN Y_n	031	NAND Y_n with top of stack
OR	371	form $A+\overline{Y}_n$
ANDIN X_n	020	form $X_n.(A+\overline{Y}_n)$
OR	371	form $X_n.(A+\overline{Y}_n)+\overline{X}_n.B$
OUTPUT X_{n+1}	027	output top of stack to X_{n+1}
ANDIN Y_n	030	AND Y_n with top of stack
ASPI A	014	form $Y_n.A$, push 1
NANDIN W_n	011	NAND W_n with top of stack
NANDIN Y_n	031	form $\overline{W}_n.\overline{Y}_n$
ANDIN Z_n	040	form $\overline{W}_n.\overline{Y}_n.Z_n$
ANDIN C_1	050	form $W_n.Y_n.Z_n.C_1$
OR	371	form $Y_n.A+\overline{W}_n.\overline{Y}_n.Z_n.C_1$
OUPUT Y_{n+1}	037	output top of stack to Y_{n+1}
ANDIN Z_n	040	AND Z_n with top of stack
PUSH 1	005	push 1
ANDIN C_1	050	AND C_1 with top of stack
EXOR	373	form $Z_n!C_1$
OUTPUT Z_{n+1}	047	output top of stack to Z_{n+1}
ANDIN W_n	010	AND W_n with top of stack
ANDIN Z_n	040	form $W_n.Z_n$
ANDIN C_1	050	Form $W_n.Z_n.C_1$
OUTPUT C_2	057	output top of stack to C_2
RESTART	000	restart cycle

Both examples need about the same number of instructions but the second uses less stored states which are normally used up sooner than the inputs.

The following is a computer simulation of the above two examples:

```
C
C       DECADE COUNTER EXAMPLE 1
C
C       CALCULATE COMMON TERMS A AND B
C
045,011,371,106,032,042,010,116,
C
C       CALCULATE NEW VALUE OF W AND SAVE ON STACK
C
012,104,022,112,375,
C
C       CALCULATE NEW VALUE OF X AND SAVE ON STACK
C
104,033,371,024,023,112,375,
C
C       CALCULATE NEW VALUE OF Y AND SAVE ON STACK
C
032,104,013,033,042,010,375,
C
C       CALCULATE NEW VALUE OF Z AND SAVE ON STACK
C
044,010,377,
C
C       CALCULATE C2, THE CARRY OUT
C
010,042,012,017,
C
C       POP SAVED VALUES OFF STACK
C
007,046,007,036,007,026,007,016,
C
C       RESTART
C
000,
END
THE ABOVE IS AN EXAMPLE INPUT FILE.
```

Run of example 1:-

```
S16ODM VO1B
$LHO
INIT   ADDR 000000
FINL   ADDR 016330
ENTR ADDR 000000
$E0
GI SBASIM VO1A
COMMAND SUMMARY? (Y/N) :N
HOW MANY OUTPUTS?
: 1
INITIAL OUTPUTS
: 0
HOW MANY PAGES?
: 1
HOW MANY SSTATES ON PAGE 1
: 9
INITIAL SSTATES ON PAGE 1
:011100000                          Initially in state 7
HOW MANY INPUTS?
: 1
COMMAND?
: LH0                               Read in input file
INIT ADDR 0
FINAL ADDR 42
COMMAND?
:B0, 13
COMMAND?
:B1,20
COMMAND?
:B2,27
COMMAND?
:B3,30
COMMAND?
:B4,34
COMMAND?
:B5,36
COMMAND?
:B6,38
COMMAND?
:B7,40
COMMAND?
:DB                                 Set and display breakpoints
B0:13
B1:20
B2:27
B3:30
B4:34
B5:36
B6:38
B7:40
COMMAND?
:G1,1                               Simulate 1 cycle with input 1
B000@13
COMMAND?
:PS
STACK = 11                          W saved on stack
COMMAND?
:C
B0001@20
COMMAND?
:PS
STACK =101                          X saved on stack
COMMAND?
:C
B002@27
COMMAND?
:PS
STACK = 10001                       Y saved on stack
COMMAND?
:C
B003@30
COMMAND?
:PS
STACK = 10001                       Z saved on stack
COMMAND?
:C
B004@34
COMMAND?
:PB
BUFFERS = 0                         Carry out is zero
COMMAND?
:C
B005@36
COMMAND?
:P1
PAGE = 01100 0001                   Store Z
COMMAND?
```

COMMENTS

```
:C
B006@ 38
COMMAND?
:P1
PAGE 1 = 01000 0001                    Store Y
COMMAND?
:C
B0007@40
COMMAND?
:P1
PAGE = 00000 0001                      Store X
COMMAND?
:B7,42
COMMAND?
:C
B007@42
COMMAND?
:P1
PAGE 1 = 10000 0001                    Store W-now in state 8
COMMAND?
:PD
DEPTH = 5                              5 elements of the stack used
COMMAND?
:IN                                    Initialize
HOW MANY OUTPUTS?
:1
INITIAL OUTPUTS
:0
HOW MANY PAGES?
:1
HOW MANY SSTATES ON PAGE 1
:9
INITIAL SSTATES ON PAGE 1
:100100000                             Initially in state 9
HOW MANY INPUTS?
:1
COMMAND?
:B                                     Remove all breakpoints
COMMAND?
:DB
NONE!!
COMMAND?
:B0,30
COMMAND?
:G1,1
B000@30
COMMAND?
:PS
STACK = 00001                          W, X, Y and Z saved on stack
COMMAND?
:C
1                                      End of 1st cycle
COMMAND?
:PO
OUTPUTS = 1                            Carry out is 1
COMMAND?
:P1
PAGE 1 = 00000 0000                    Now in state 0
COMMAND?
:B                                     Remove all breakpoints
COMMAND?
:G1,1
2                                      End of 2nd cycle
COMMAND?
:PO
OUTPUTS = 0                            Carry out is 0
COMMAND?
:P1
PAGE 1 = 00010 0010                    Now in state 1
COMMAND?
:G1,1
3                                      End of 3rd cycle
COMMAND?
:PO
OUTPUTS = 0                            Carry out is 0
COMMAND?
:P1
PAGE 1 = 00100 0000                    Now in state 2
COMMAND?
:G1,1
4                                      End of 4th cycle
COMMAND?
:P
OUTPUTS = 0                            Carry out is 0
COMMAND?
:P1
PAGE 1 = 00110 0010                    Now in state 3
COMMAND?
:X                                     Exit
S16ODM V01B
$
```

Input file for example 2:

```
C
C       DECADE COUNTER EXAMPLE 2
C
C       CALCULATE COMMON TERMS A AND B
C
041,005,051,371,016,030,040,050,026,
C
C       CALCULATE NEW VALUE OF W
C
010,014,020,022,371,017,
C
C       CALCULATE NEW VALUE OF X
C
021,024,014,031,371,020,371,027,
C
C       CALCULATE NEW VALUE OF Y
C
030,014,011,031,040,050,371,037,
C
C       CALCULATE NEW VALUE OF Z
C
040,005,050,373,047,
C
C       CALCULATE CARRY OUT C2
C
010,040,050,057,
C
C       RESTART
C
000,
END
```

Run of example 2:-

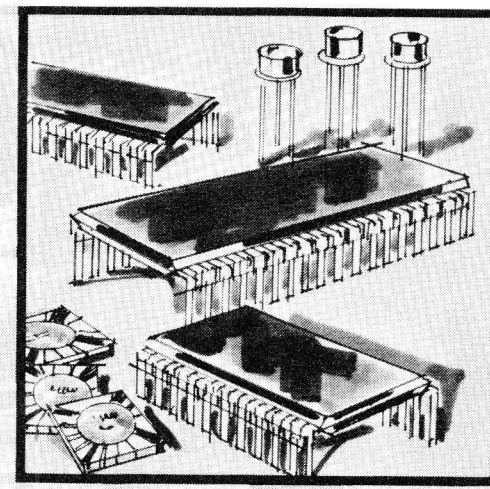
COMMENTS

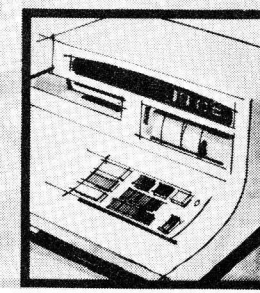
```
S16ODM V01B
$LH0
INIT ADDR 000000
FINL ADDR 016330
ENTR ADDR 000000
$E0

GI SBASIM V01A
COMMAND SUMMARY? (Y/N):N
HOW MANY OUTPUTS?
:5
INITIAL OUTPUTS
:00000
HOW MANY PAGES?
:1
HOW MANY SSTATES ON PAGE 1
:2
INITIAL SSTATES ON PAGE 1
:00
HOW MANY INPUTS?
:5
COMMAND?
:LH0                                  Read in input file
INIT ADDR 0
FINAL ADDR 40
COMMAND?
:SP 0,I                               Set auto print options
COMMAND?
:GI,10001
INPUTS = 10001                        Initially in state 8
OUTPUTS = 10010                       State 9
1
COMMAND?
:GI,10011
INPUTS = 10011                        State 9
OUTPUTS = 00001                       State 0 carry 1
2
COMMAND?
:GI,00111
INPUTS = 00111                        State 3
OUTPUTS = 01000                       State 4
3
COMMAND?
:SETC 1,1                             Illegal command
?
COMMAND?
:SC 1,1                               Set O/I connections
COMMAND?
:SC 2,2
COMMAND?
:SC 3,3
COMMAND?
:SC 4,4
```

```
COMMAND?
:SC 5,5
COMMAND?
:PC                                    Print connections
OUTPUT IS CONNECTED TO INPUT
1                          1
2                          2
3                          3
4                          4
5                          5
COMMAND?
:RC 5,5
COMMAND?
:G12,00001                             Simulate 12 cycles
INPUTS = 01001
OUTPUTS = 01010
4
INPUTS = 01011
OUTPUTS = 01100
5
INPUTS = 01101
OUTPUTS = 01110
6
INPUTS = 01111
OUTPUTS = 10000
7
INPUTS = 10001
OUTPUTS = 10010
8
INTPUTS = 10011
OUTPUTS = 00001
9
INPUTS = 00001
OUTPUTS = 00010
10
INPUTS = 00011
OUTPUTS = 00100
11
INPUTS = 00101
OUTPUTS = 00110
12
INPUTS = 00111
OUTPUTS = 01000
13
INPUTS = 01001
OUTPUTS = 01010
14
INPUTS = 01011
OUTPUTS = 01100
15
COMMAND?
:X
S160DM V01B
$
```

MEMORY 4

RAMs	4- 3
EAROMs	4- 9
ROMs	4- 41
Keyboard Encoders/Character Generators	4- 63
Static Shift Registers	4-105





MICRO ELECTRONICS

RANDOM ACCESS MEMORIES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
1K RAM	1,024 bits organized 256 x 4	RA-3-4256	4-4
		RA-3-4256A	4-4
		RA-3-4256B	4-4

RA-3-4256
RA-3-4256A
RA-3-4256B

1024 Bit Static Random Access Memories

FEATURES

- 256 x 4 Organization
- Single +5 Volt Supply
- True TTL Compatability
- Static Operation—no clocks required
- 500ns Access Time: RA-3-4256
- 650ns Access Time: RA-3-4256A, RA-3-4256B
- Separate Data Input and Output Lines
- Low Power
- Three State Outputs—under control of Chip Select signals
- Power Down State: RA-3-4256, RA-3-4256A
- Zener Protected Inputs

DESCRIPTION

The General Instrument RA-3-4256, RA-3-4256A and RA-3-4256B are 1024 bit, high-speed static random access memories organized as 256 4-bit words. Low voltage N-channel ion implant technology results in true TTL compatibility from a single 5 volt supply, and static operation. These devices are extremely useful in small read-write memory systems for terminals, peripherals, microcomputers, and a wide variety of portable equipment.

The RA-3-4256 and RA-3-4256A can also utilize a back bias substrate and split supply for applications where a low standby power drain is required. These devices may be switched to the power down state under system control with no danger of memory storage errors.

The RA-3-4256B's 22-pin package, which has a 0.4" width, permits tight packing density on printing circuit cards.

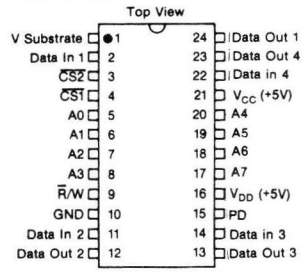
	RA-3-4256	RA-3-4256A	RA-3-4256B
Package	24-pin	24-pin	22-pin
No. of Chip Select Inputs	2	2	1
Power Down Capability	Yes	Yes	No
Max Access Time	500ns	650ns	650ns

PIN CONFIGURATIONS

24 LEAD DUAL IN LINE

RA-3-4256/RA-3-4256A

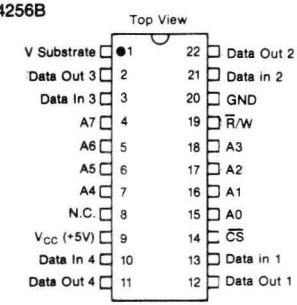
Top View



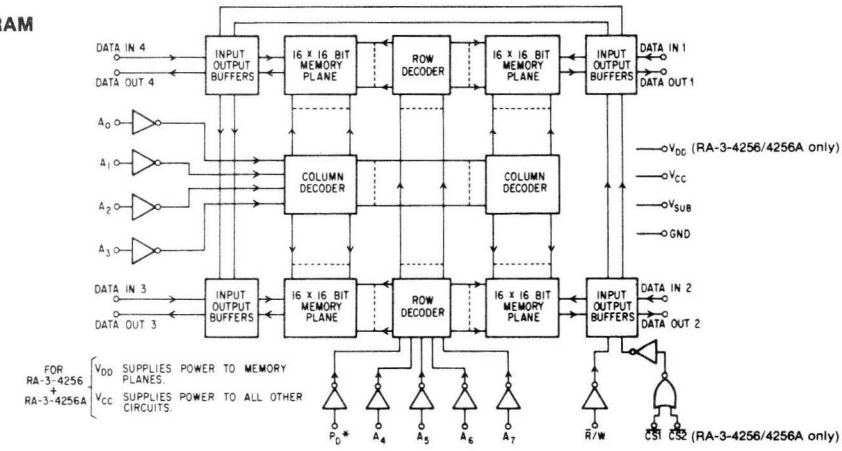
22 LEAD DUAL IN LINE

RA-3-4256B

Top View



BLOCK DIAGRAM



POWER DOWN OPERATION

The RA-3-4256 and RA-3-4256A bring out, to separate pins, the circuit Substrate, the memory plane supply (V_{DD}) and the peripheral circuit's power supply (V_{CC}). These three connections, plus the Power Down input, allow extremely flexible control of the memory during standby and/or reduced voltage and power dissipation operation.

In a static memory the memory cell is a flip flop and, in order to retain information, one side of the flip flop must be on continuously. Thus the static memory power dissipation is higher than for a dynamic memory and techniques for reducing this dissipation when the device is in the standby condition become attractive for the system user.

The power down pin ($\overline{PD}$ pin 15) isolates the memory from the address decoders, so that incorrect data cannot be written into the memory when V_{CC} is not within its specified limits. Even if V_{DD} is maintained by a battery, if V_{CC} falls in a manner such that the $\overline{R}/W$ circuitry considers itself to be in a write mode for a short interval of time, then false data will be written into the memory. To prevent this from happening, $\overline{PD}$ is driven low by a signal (Power Down In) that senses V_{CC} is going below its allowable range; this is usually done by monitoring the power supply's AC input voltage. Fig. 1 shows the timing required before V_{CC} falls, to preserve a memory with a battery backup on V_{DD}.

To prevent miswriting a data word, the fall of the $\overline{PD}$ signal must not intersect the $\overline{R}/W$ pulse. Otherwise, the write operation may not be complete at a given address when $\overline{PD}$ falls. The fall of $\overline{PD}$ during the R/W pulse would prevent that address (and all others) from having access to the memory section of the device. The external gating in Fig. 1b disallows $\overline{PD}$ from falling during a write operation.

Battery backup for V_{DD} can be accomplished as shown in Fig. 2. The germanium power transistor (2N3612) is used here as a power diode. For a card with 10 RA-3-4256's, V_{DD} would draw a maximum current of 500 mA. The 2N3612 would have a maximum collector emmiter voltage drop of .25 v dc at 500 mA base current. During normal operation, if V_{CC} varied from 4.75 to 5.25 volts, V_{DD} would vary from 4.5 to 5.00 volts, which is within the operating specification. In the power down mode, V_{DD} would be supplied by the 5v standby battery. The battery voltge could fall from 5v to 4.5v (which would be from 4.25V to 3.75V for V_{DD} because of the silicon diode) and still keep the memory alive.

Once the memory is powered down so that the total supply current is reduced by a factor of 2 (since V_{CC} = 0 and is not drawing any current), I_{DD} can be reduced in half by placing −5 volts on V_{SS} — pin 1. This back-biases the substrate which reduces the current drawn in each flip-flop in the memory during this memory hold state. The −5 volts on V_{SS} can only be used to retain the information in the memory and must be removed (V_{SS} = 0) before writing into or reading from the memory.

Thus, using the power down mode and placing −5 volts on the substrate, total power dissipated would be reduced 75%, from a maximum of 500mW (5v × 100 mA) to 125 mW (5v × 25 mA).

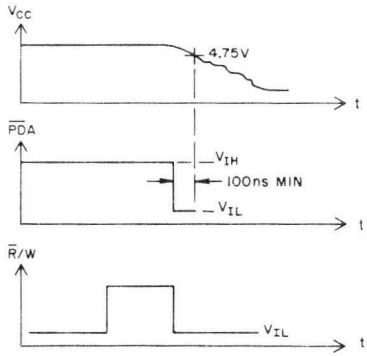


Fig.1a POWER DOWN TIMING

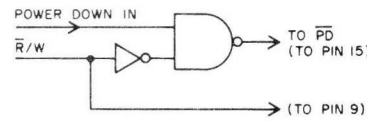


Fig.1b POWER DOWN GATING

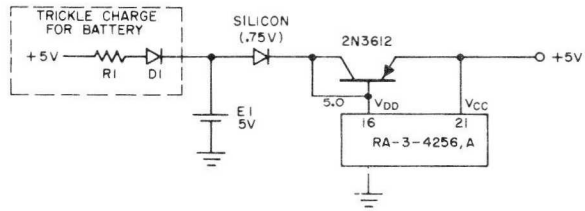


Fig.2 BATTERY STANDBY SCHEMATIC

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC}, V_{DD} and input voltages (with respect to GND) ....-0.3V to +8.0V
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

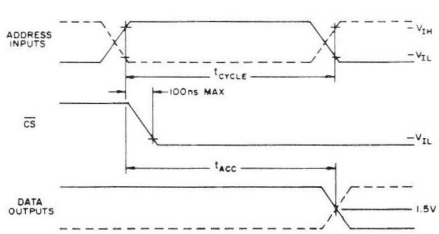
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5% (V_{CC} is the peripheral circuitry supply for the RA-3-4256/4256A and the power supply for RA-3-4256B.)
V_{DD} = +5V ±10% (V_{DD} is the memory call supply for the RA-3-4256/4256A.)
$V_{Substrate}$ = GND
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, C_{LTOTAL} = 100pF

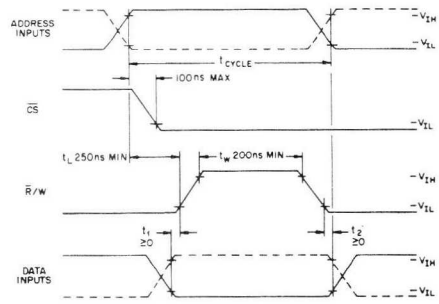
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input load current (all inputs)	I_{IN}	—	—	10	μA	V_{IN}=0V to 5.25V
Output leakage current	I_{LOH}	—	—	10	μA	V_{OUT}=4.0V
Output leakage current	I_{LOL}	—	—	−10	μA	V_{OUT}=0.4V
Input low voltage	V_{IL}	—	—	0.65	V	
Input high voltage	V_{IH}	2.2	—	—	V	
Output low voltage	V_{OL}	—	—	0.40	V	I_{OL}=1.6mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH}=100μA
Input capacitance (all inputs)	C_{IN}	—	5	—	pF	f=1 MHz
Output capacitance (all outputs)	C_{OUT}	—	10	—	pF	f=1 MHz
Total Power Supply Current	I_{DD} & I_{CC}	—	60	100	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{CC}	—	30	50	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{DD}	—	30	50	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{CC}	—	60	100	mA	RA-3-4256B
AC CHARACTERISTICS						
Access Time RA-3-4256	T_{ACC}	—	—	500	ns	
Cycle Time RA-3-4256	T_{CYCLE}	500	—	—	ns	
Access Time RA-3-4256A	T_{ACC}	—	—	650	ns	See Timing Diagrams
Cycle Time RA-3-4256A	T_{CYCLE}	650	—	—	ns	
Access Time RA-3-4256B	T_{ACC}	—	—	650	ns	
Cycle Time RA-3-4256B	T_{CYCLE}	650	—	—	ns	
POWER DOWN DC CHARACTERISTICS (RA-3-4256 & RA-3-4256A ONLY):						
Power Down Sink Current	I_{PD}	—	—	100	μA	V_{PD}=0.4V
Memory hold voltage	V_{DD}	3.75	—	7.0	V	V_{CC}=0
Substrate Power Supply	V_{SS}	−5	—	0	V	−5V in Power Down Mode only
Substrate Power Supply Current	I_{SS}	—	20	100	μA	V_{SS}=−5V, V_{CC}=0

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

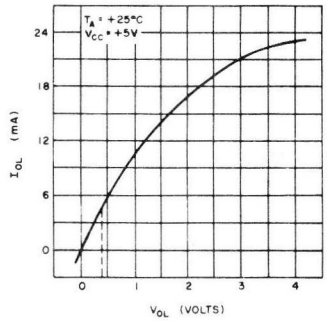


READ ACCESS

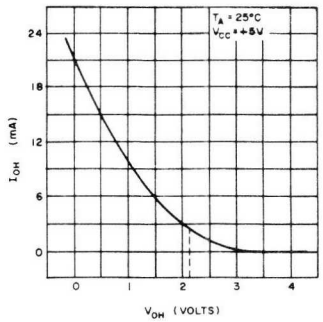


WRITE CYCLE

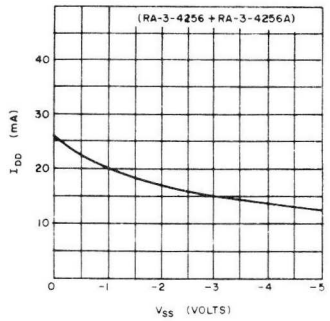
TYPICAL CHARACTERISTIC CURVES



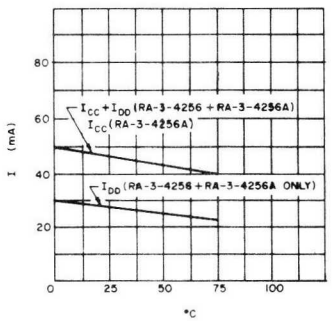
TYPICAL OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



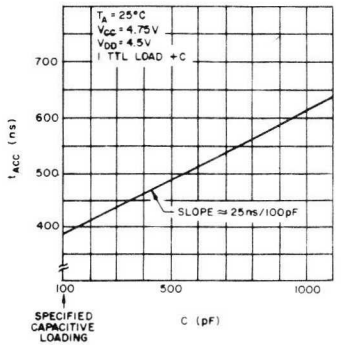
TYPICAL OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



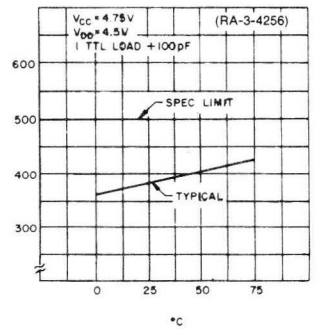
TYPICAL I_{DD} VS. V_{SS} (for memory hold during power down)



TYPICAL POWER SUPPLY CURRENT VS. TEMPERATURE



T_{ACC} (Typical) VS. CAPACITIVE LOADING



T_{ACC} VS. TEMPERATURE

MEMORY

MICRO ELECTRONICS

ELECTRICALLY ALTERABLE READ ONLY MEMORIES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
512 BIT EAROM	512 bits organized 32 x 16	ER2051	4-18
	512 bits organized 64 x 8	ER2055	4-21
1K RAM/EAROM	1,024 bits organized 256 x 4	ER1711	4-13
1400 BIT SERIAL EAROM	1,400 bits organized 100 x 14	ER1400	4-10
4K EAROM	4,096 bits organized 1,024 x 4	ER2401	4-24
		ER3400	4-36
8K EAROM	8,192 bits organized 2,048 x 4	ER2805	4-30

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 Word x 14 bit organization
- Word alterable
- 10 years unpowered data storage
- **Write/Erase time 20ms/word**
- Single -35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Addressing is by two consecutive one-of-ten codes.

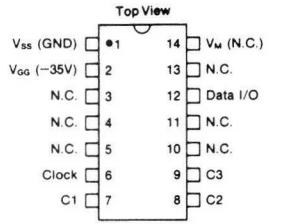
Mode selection is by a 3 bit code applied to C1, C2 and C3.

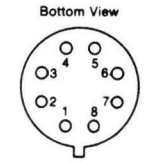
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

Standard package
14 LEAD DUAL IN LINE

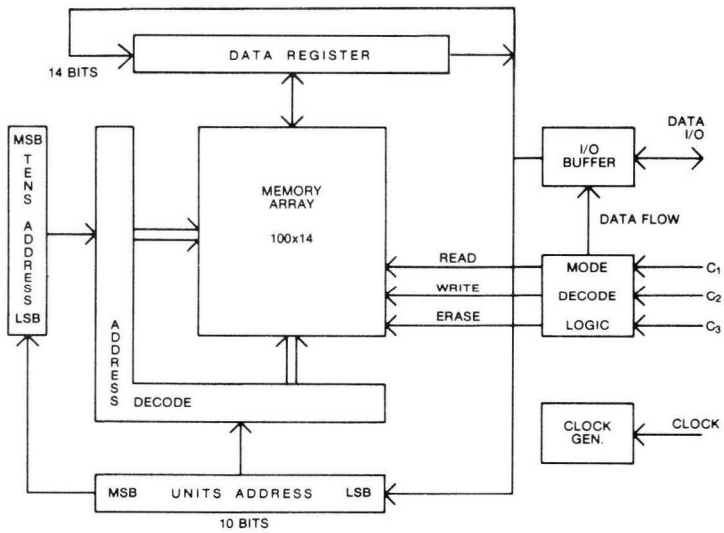
Special Order Package
8 LEAD TO-8 (ER1400T)





1. Data I/O
2. V_M (N.C.)
3. V_{SS} (GND)
4. V_{GG} (−35V)
5. Clock
6. C1
7. C2
8. C3

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to −35 volt supply.
Clock	14kHz timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby—contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read—The address word is read from memory into the data register.
1	0	1	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase—The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write—The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

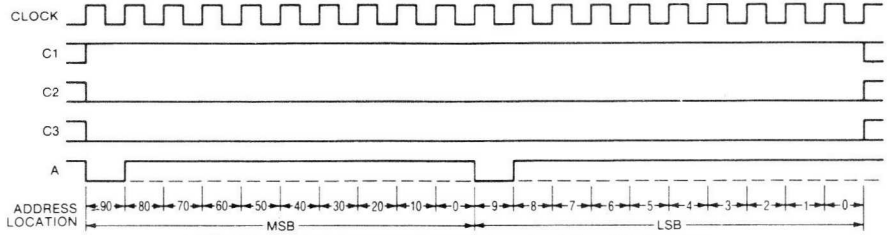
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	VIL	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	VIH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	VOL	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	VOH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply current	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	11.2	14.0	16.8	kHz	
Clock duty cycle	Dϕ	45	50	55	%	
Write time	tw	16.0	20.0	24.0	ms	
Erase time	te	16.0	20.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set up time	t_{CS}	1	—	—	μs	
Control, Data hold time	t_{CH}	0	—	—	ns	
Propagation delay	tpw	—	—	20.0	μs	Load = 1 Meg, 100pF
Unpowered non-volatile data storage	T_S	10	—	—	Years	
Number of erase/write cycles	N_W	—	—	10^5	—	Per word
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

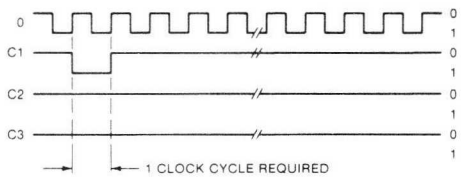
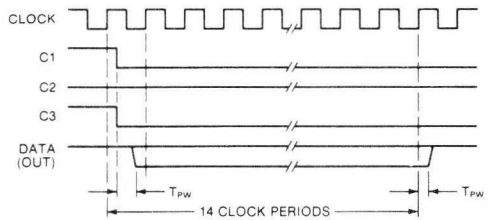


Fig.2 READ



T_{PW} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at $V_{SS}-2$ and -10 volt points.

Fig.3 SHIFT DATA OUT

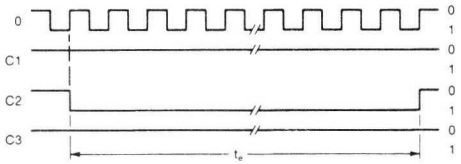


Fig.4 ERASE

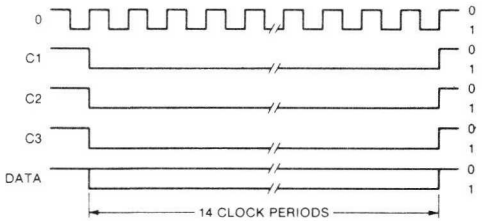


Fig.5 ACCEPT DATA

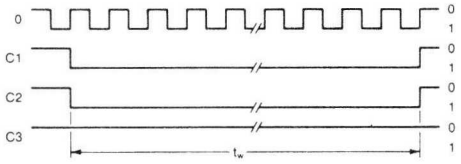


Fig.6 WRITE

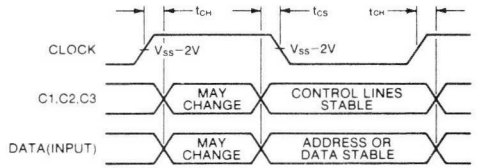


Fig.7 INPUT TIMING

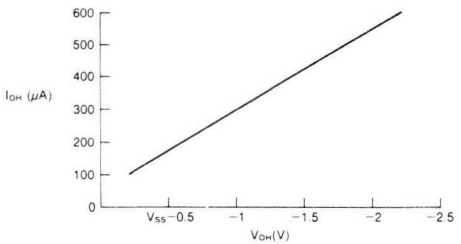


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

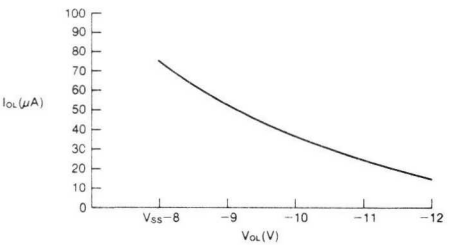


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

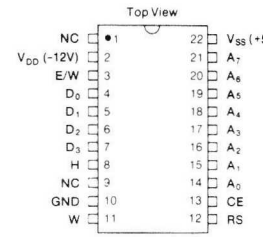
1024 Bit Non-Volatile Random Access Memory

FEATURES

- 256 x 4 organization
- Memory contents stored or restored with single pulse.
- 8 bit binary addressing
- Inputs/Outputs: modified TTL compatible (except E/W)
- On-chip address latching
- Three-state outputs
- Conventional RAM operation
- Non-volatile store on power-down
- Minimum data retention: 72 hours after 1 ms write
- P-channel, Ion-implanted MNOS process
- Dissipated power: 540mW maximum
- Power supplies required: +5, -12
- RAM memory access time: 900 ns

PIN CONFIGURATION

22 LEAD DUAL IN LINE



DESCRIPTION

The ER1711 is a fully decoded 256 x 4 bit static RAM. The EAROM has the added capability of mass storing the last written data by means of a sequential power-down. After a sequenced power-up and a 100 millisecond bulk erase, the device will be ready for normal RAM operation with written data restored.

Non-volatile data is stored by applying a negative writing pulse that selectively tunnels charge into the oxide-nitride interface at the gate insulator of the 2048 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

All stored data is retained for 72 hours minimum after a 1 millisecond write pulse and 30 days minimum after a 10 millisecond write pulse. Data can be stored and recalled by means of a power-down/power-up sequence.

PIN FUNCTIONS

D0 - D3	4 bit data word
A0 - A7	8 bit data address
V_{SS}	+5 Volt supply voltage
V_{DD}	-12 Volt supply voltage
V_{GI}	GND
CE	Chip enable: strobed during RAM cycles, low during EAROM cycles
H	Hold: normally high, low during data recall cycle
W	Write: high during RAM write cycle
RS	Restore: normally low pulsed high during recall cycle
E/W	Erase/Write: controls EAROM memory cells.

OPERATION

In normal operation the ER1711 operates as a random access memory (RAM). Before powering down, the data can be stored in the electrically alterable non-volatile read only memory EAROM cells by a single, negative write pulse. When power is restored, the previously saved data can be recalled by a power-up and data recall cycle which transfers all this saved data to the RAM memory. It is suggested that an Erase cycle be performed soon after the data recall cycle, so that the memory will be prepared in case of another power down cycle. The EAROM cycles operate as follows:

Erase Cycle:

1. The H line should be high and the RS and CE lines low
2. Positively pulse the EW line to +25 volts for 100 to 200 ms.

Stored Data Cycle:

1. The H line should be held high and the RS and CE lines low.
2. Pulse the EW line negative to -22 Volts for 1 to 10 milliseconds to store non-volatile data.
3. The non-volatile EAROM memory cells must have been previously erased for valid data retention.

Power Up and Recall Cycle:

1. Turn on power with CE and RS held to ground and the H and EW lines based to V_{SS}.
2. When power is on lower H and pulse RS to precondition the EAROM cells.
3. Lower RS and ramp down the EW line at-0.1 volts/μsec. This can be done with a series resistor in the ER line of 470K ohm.
4. After the E/W recovery time, bring both the EW and H lines to $+V_{SS}$.
5. If in the course of erasing data, the power shuts down again, the erase cycle can be terminated and a write cycle immediately started without loss of data.

In normal RAM operation only the +5 and -12 volt power supplies are required. The erase store and data read cycles require momentary high voltage pulses to tunnel changes through the MNOS memory transistors. These higher voltages can be created from the +5 and -12 power supplies using the change pumping circuits shown in Figure 1. This circuit will generate the sequence of RS, H and E/W pulses needed for power down and up sequencing. The power down and up cycles are initiated by System Save and Data Recall signals respectively. Figure 1 is a suggested circuit using standard CMOS parts; a similar circuit can be designed with TTL logic instead.

MEMORY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS} (except E/W) ..... +0.3V to -30V
E/W pin relative to V_{SS} ..... +28 to -26V
Operating Ambient Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Soldering Temperature of leads (10 seconds) ..... +300°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

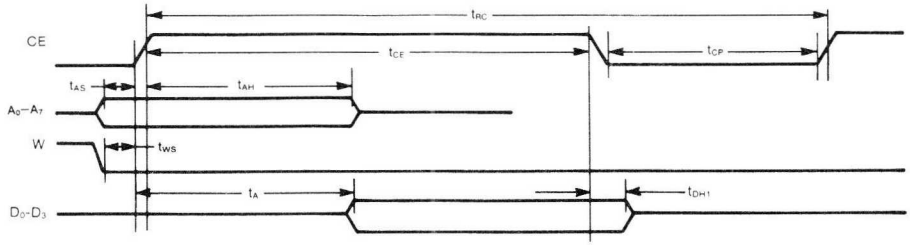
V_{DD} = -12 V±5%
V_{SS} = +5 V±5%
V_{GI} = GND
Operating Temperature T_A = 0° to 70 °C

Characteristics	Symbol	Min.	Typ.**	Max.	Units	Conditions
DC CHARACTERISTICS						
Input Logic 1	V_{IH}	V_{SS}-1.5	—	V_{SS}+0.3	V	
Input Logic 0	V_{IL}	—	—	0.8	V	I_{OH} = 500 µA
Output Logic 1	V_{OH}	2.4	—	—	V	I_{OL} = 1.6 mA
Output Logic 0	V_{OL}	—	—	0.7	V	
Input Leakage (Except pin 1, 2, 3, 9, 10 and 22)	I_L	-10	—	—	µA	V_{IN} = -15
E/W Leakage	I_{EW}	-12	—	12	µA	
V_{DD} Supply Current	I_{DD}	-35	-25	—	mA	
V_{SS} Supply Current	I_{SS}	—	25	40	mA	
Erase Voltage	V_E	+25	—	30	V	I_{EW} = +10 µA
Write Voltage	V_W	-25	—	-20	V	I_{EW} = -10 µA
Recall Voltage	V_R	-15	—	-10	V	I_{EW} = -10 µA
RAM operating	V_D	—	V_{SS}	—	V	
Erase Write Line Capacitance	C_{EW}	200	—	250	pF	f = 1 MHz
Data, Control, Address Lines Capacitance	C_I	—	—	15	pF	f = 1 MHz
AC CHARACTERISTICS: EAROM Cycle						
Erase Pulse Width	t_E	100	—	200	ms	$V_{E/W}$ = +25 V
Non-volatile store time	t_S	1.0	—	10	ms	$V_{E/W}$ = -20V
Recall Precondition time	t_{RP}	5.0	—	10	µs	$V_{E/W}$ = RS = Vss
Recall Ramp time	t_{R1}	90	—	110	µs	
E/W Recovery time	$t_{E/WR}$	0.5	—	2.0	µs	$V_{E/W}$ = -10 V
Recall Ramp time	t_{R2}	90	—	110	µs	
AC CHARACTERISTICS: RAM Read/Write Cycle						
RAM Read/Write Cycle Time	t_{RC}	1500	—	—	ns	
Chip Enable Pulse Width	t_{CE}	850	—	50,000	ns	
Address set up time	t_{AS}	0	—	—	ns	
Address Hold Time	t_{AH}	200	—	—	ns	
Read Access Time	t_A	900	—	—	ns	
Rise, Fall Times	t_R, t_F	—	—	50	ns	
Data Hold Time	t_{DH1}	50	—	—	ns	
Chip Precharge Time	t_{CP}	700	—	—	ns	
Write Pulse Width	t_W	600	—	—	ns	
Write Set Up Time	t_{WS}	0	—	50	ns	
Write Hold Time	t_{WH}	0	—	100	ns	
Data Set Up Time	t_{DS}	0	—	100	ns	
Data Hold Time	t_{DH2}	0	—	100	ns	

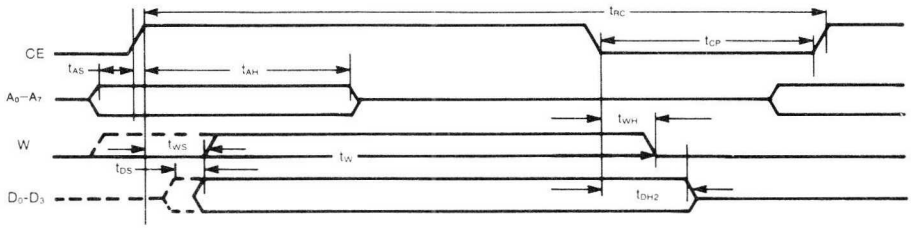
**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

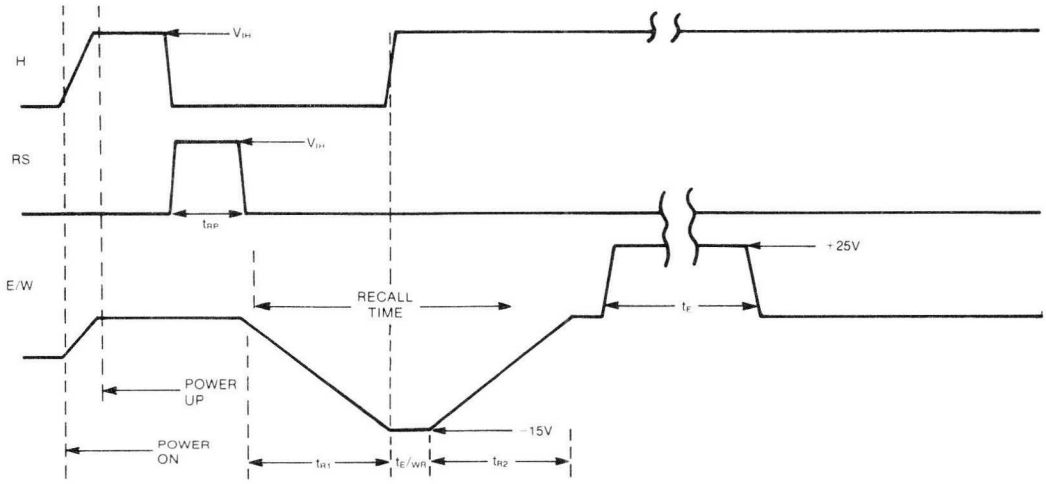
READ MODE, RAM



WRITE MODE, RAM



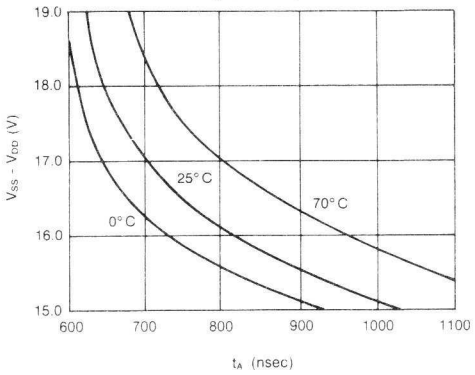
NON VOLATILE MEMORY POWER-UP AND RECALL CYCLE



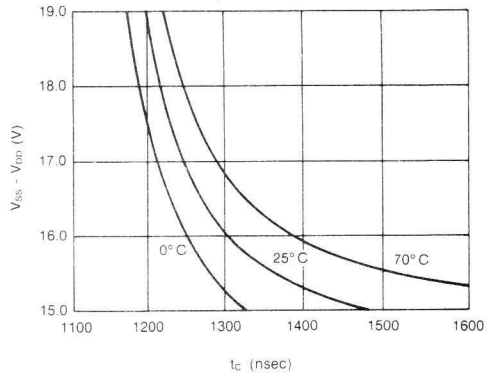
MEMORY

TYPICAL OPERATING CHARACTERISTICS, T_A =0° to 70°C

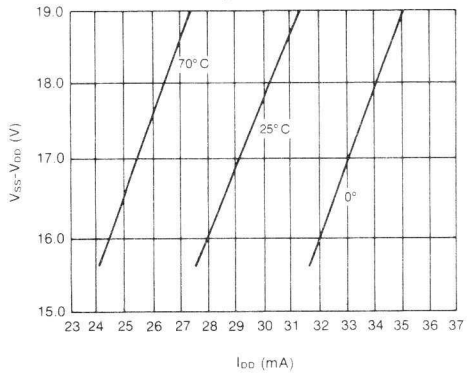
TYPICAL READ ACCESS TIME
VS. POWER SUPPLY VOLTAGE
(V_{SS} - V_{DD})



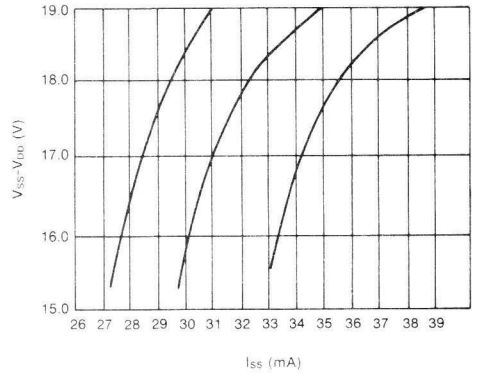
TYPICAL READ CYCLE TIME
VS POWER SUPPLY VOLTAGE
(V_{SS} - V_{DD})



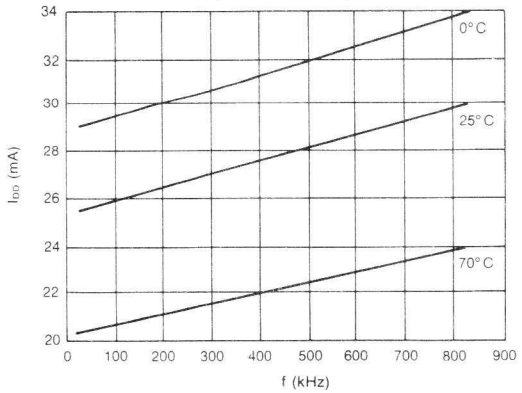
TYPICAL SUPPLY CURRENT (I_{DD})
VS POWER SUPPLY VOLTAGE
(V_{SS} — V_{DD})



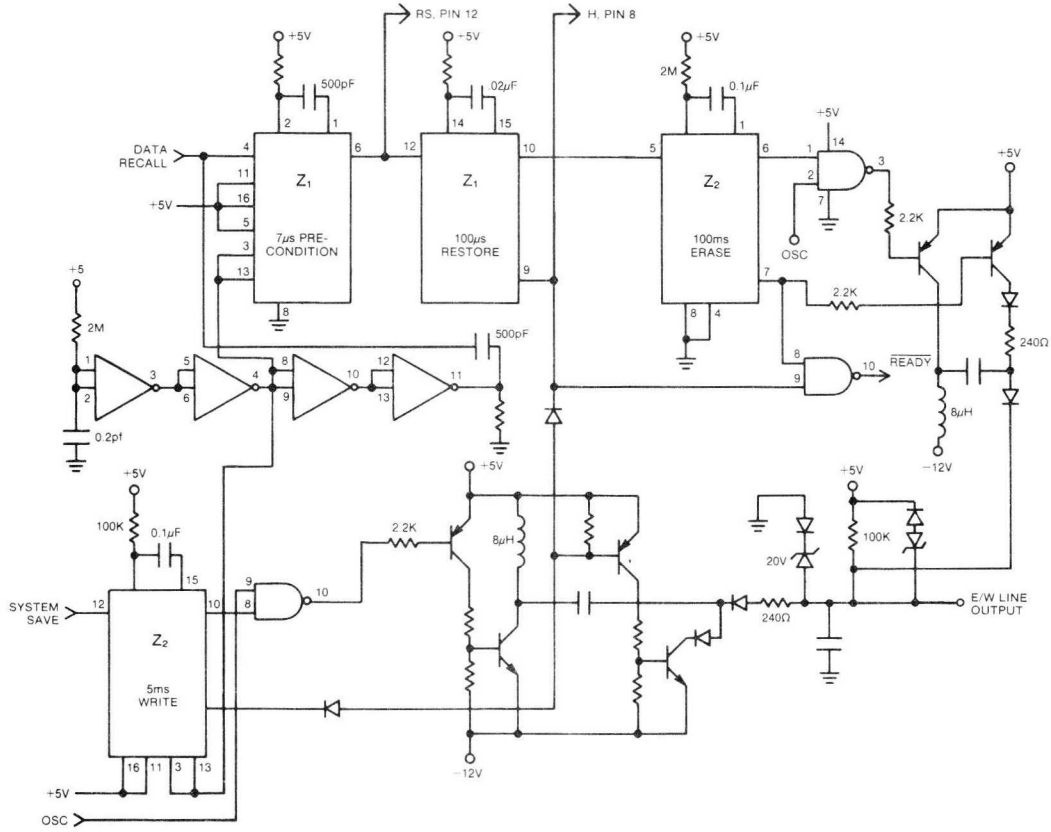
TYPICAL SUPPLY CURRENT (I_{SS})
VS POWER SUPPLY VOLTAGE
(V_{SS} - V_{DD})



TYPICAL SUPPLY CURRENT
VS OPERATING FREQUENCY
(V_{SS} - V_{DD} = 17v)



ERASE/WRITE CIRCUIT



NOTES:
1. Data Recall interrupt at start of power-down cycle
2. NPN Transistors: 2N3904
   PNP Transistors: 2N 3905
3. Diodes: IN914
4. All Resistors: 1/8 W ±10%
5. Unmarked Resistors: 10K
6. Power-up (Restore, Write, into RAM. ERASE EAROM) cycle started by Rise of System Reset.
7. Capacitors: 0.47μF ±10%
8. Dual Monostable CD4098B. Z_1, Z_2
9. Gate CD4011A
10. Inverter CD4093B
11. Oscillator Freq. approx. 50 kHz
12. Two 22 Volt Zener Diodes, IN969

512 Bit Electrically Alterable Read Only Memories

FEATURES

- 32x16 Organization
- 5-Bit Addressing
- TTL Compatible
- Chip Select
- Word Alterable
- 10 Year Unpowered Data Storage at +70°C
- 3 μs Access Time (ER2051)
- 4 μs Access Time (ER2051 HR)
- Write/Erase Time 50 ms/word (ER2051), 100 ms/word (ER2051 HR)
- +5, -28V Supplies
- No Voltage Switching Required

DESCRIPTION

The ER2051 and ER2051 HR are fully decoded 32 X 16 electrically erasable and reprogrammable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Two TTL compatible control pins switch voltages internally for write, read and erase control.

The EAROM may be operated with the V_{SS} power supply between +5 and +10 volts, as long as the V_{SS} - V_{GG} always equals 33 Volts. Thus, V_{SS} can be +5 volts for TTL compatibility or up to +10 volts for CMOS compatibility, if V_{GG} is appropriately adjusted.

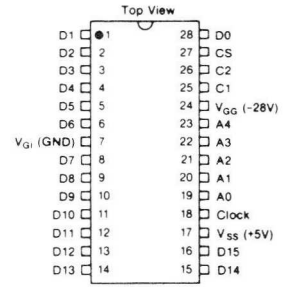
The ER2051 HR is screened to mil std. 883A/method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. It is available in 28 lead ceramic dual in line package.

OPERATION

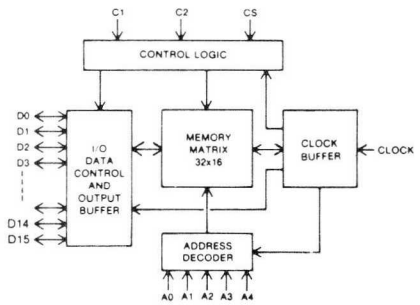
Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which lowers the threshold of both transistors), data is written into one of the transistors lowering its threshold. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs

C1	C2	
0	1	Erase Mode: stored data is erased at addressed location.
1	0	Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation.
0	0	Write Mode: input data written at addressed location. Clock not required.

CLK	Clock Input. Pulse to logic "1" for read operation. Data will remain valid for 20 to 60 seconds; the outputs will then become open circuit until another clock pulse is received.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at -28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to Vss) ..... -35V to +0.3V
Storage temperature ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions are not implied—operating ranges are specified below.

Standard Conditions (for TTL Compatibility)

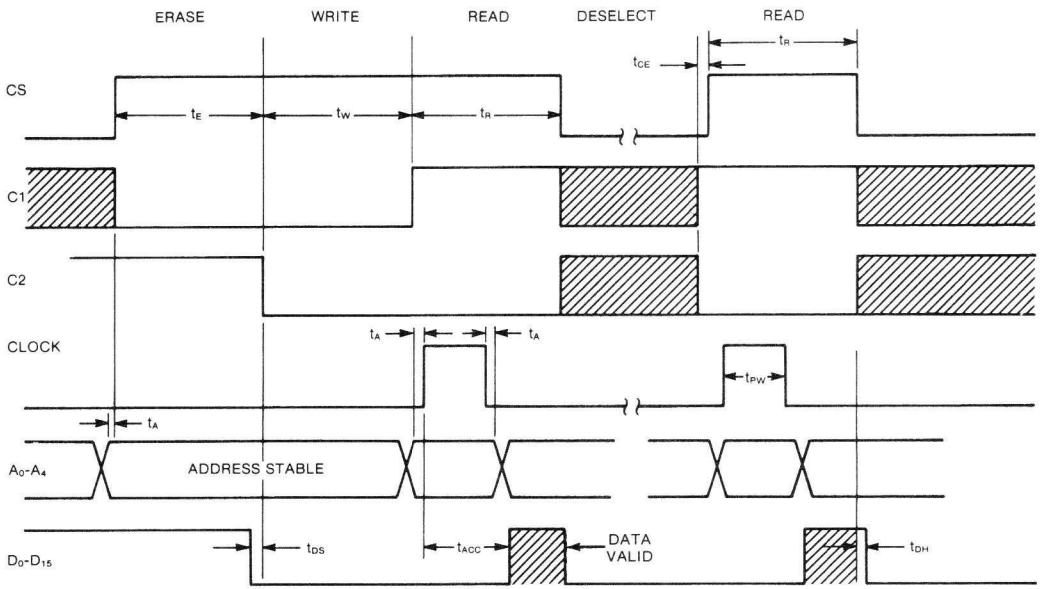
V_{SS} = +5V±5%
V_{GG} = -28V±5%
V_{GI} = GND
Operating Temperature (T_A) = O°C to +70C for ER2051, T_A = -55°C to+125°C for ER2051 HR
Output Load = 100pF, 1 TTL load

Characteristic	Symbol	ER2051 Min	ER2051 Typ.**	ER2051 Max	ER2051 HR Min.	ER2051 HR Typ.**	ER2051 HR Max	Units	Conditions
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} -1.5	-	V_{SS} +0.3	V_{SS} -1.5	-	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} -15	-	0.8	V_{SS} -10	-	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} -1.5	-	-	V_{SS}-1.5	-	-	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	-	-	0.8	-	-	0.8	V	I_{OL} = 1.6 mA for V_{SS} =5V
Input Leakage	I_L	-	2	10	-	2	10	μA	V_{IN} =V_{SS} -15
Output Leakage	I_O	-	2	10	-	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	-	-	14	-	-	18	mA	I_{GG} Returned thru V_{SS}
Write	I_{GG}	-	-	11	-	-	15	mA	
Erase	I_{GG}	-	-	11	-	-	15	mA	
Deselected	I_{GG}	-	-	9	-	-	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	-	-	3.0	-	-	4.0	μs	
Clock Pulse Width	t_{PW}	2.0	-	20.0	2.0	-	20.0	μs	
Erase Cycle Time	t_E	50	-	200.0	100	-	200.0	ms	
Write Cycle Time	t_W	50	-	200.0	100	-	200.0	ms	
Read Cycle Time	t_R	3.5	-	24.0	4.5	-	25	μs	
Address-Clock Time	t_A	50	-	-	50	-	-	ns	
Control-Enable Time	t_{CE}	50	-	-	50	-	-	ns	
Data Set Up Time	t_{DS}	50	-	-	50	-	-	ns	
Data Hold Time	t_{DH}	50	-	-	50	-	-	ns	
Number of Read's/Word between Refresh	N_{RA}	10^{11}	-	-	10^{11}	-	-	-	
Number of Erase/Write Cycles	N_W	10^6	-	-	10^5	-	-	-	
Input Capacitance, all pins	C_{IO}	-	8	15	-	8	15	pF	
Unpowered Data Storage Time	t_S	10	-	-	1	-	-	years	at max. temperature
Power Dissipation, Read Cycle	P_D	-	450	500	-	450	500	mW	at 25°C V_{SS}= +5, V_{GG}= -29
	P_D	not applicable			-	-	500	mW	at 125°C V_{SS}= +5, V_{GG} = -29
	P_D	not applicable			-	-	600	mW	at -55° V_{SS}= +5, V_{GG} = -29
Pulse Rise, fall times	t_{RTF}	10	-	100	10	-	100	ns	

**Typical values are at +25°C and nominal voltages.

MEMORY

TIMING DIAGRAM



512 Bit Electrically Alterable Read Only Memory

FEATURES

- 64 x 8 Organization
- 6-Bit Addressing
- TTL Compatible
- Two Chip Selects
- Word Alterable
- 10 Year Unpowered Data Storage
- 4 μs Access Time
- Write/Erase Time 50ms/word
- +5, -28V Supplies
- No Voltage Switching Required

DESCRIPTION

The ER2055 is a fully decoded 64 x 8 electrically erasable and reprogrammable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Two TTL compatible control pins switch voltages internally for write, read and erase control.

OPERATION

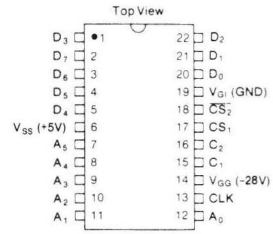
Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which lowers the threshold of both transistors), data is written into one of the transistors lowering its threshold. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

The ER2055 EAROM may be operated with V_{SS} between +5 and +10 volts for either TTL or MOS compatibility. The negative power supply, V_{GG}, should be adjusted so that the difference between V_{SS} and V_{GG} is always 33 volts.

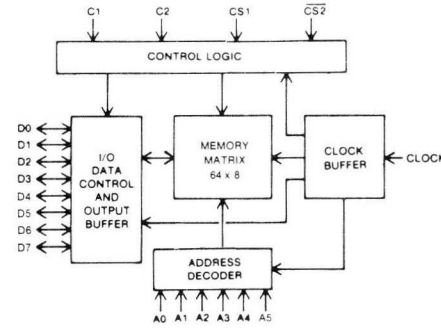
It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

A_0-A_5	6-Bit Word Address
D_0-D_7	Data input and output pins
CS1, $\overline{CS2}$	Chip Selects Chip selected at logic "1" on CS1 and logic "0" on $\overline{CS2}$. When chip is not selected, outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 C2 0 1 Erase Mode: stored data is erased at addressed location. 1 0 Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation. 0 0 Write Mode: input data written at addressed location. Clock not required.
CLK	Clock Input. Pulse to logic "1" for read operation. Data will remain valid for 20 to 60 seconds; the outputs will then become open circuit until another clock pulse is received.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at -28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... -35V to +0.3V
Storage temperature ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

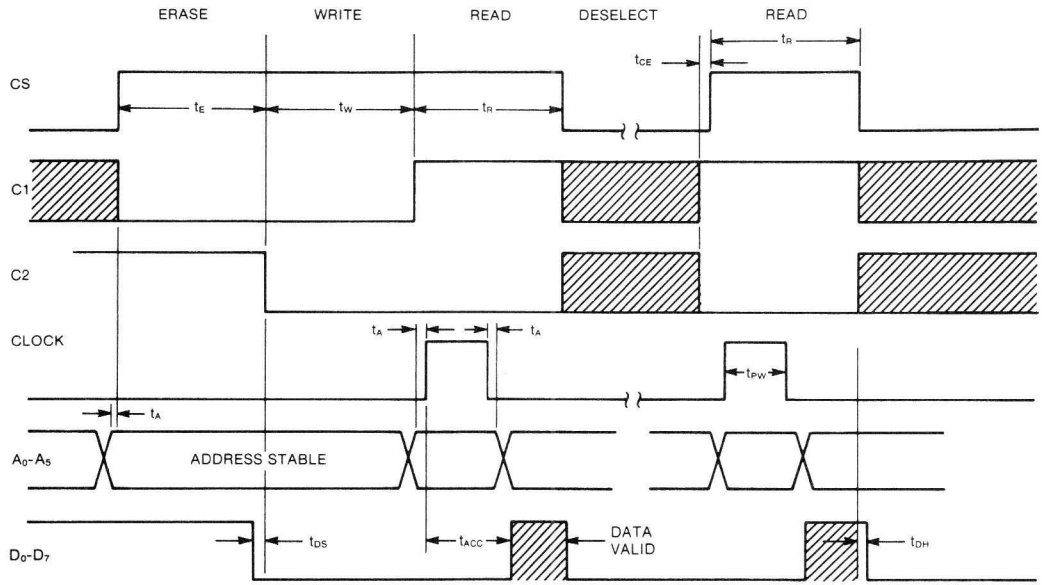
Standard Conditions (for TTL compatibility)

V_{SS} = +5V ±5%
V_{GG} = -28V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C
Output Load = 100pF, 1 TTL load

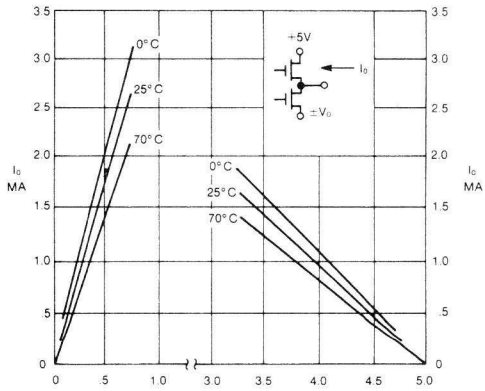
Charcteristics	Symbol	Min.	Typ.**	Max.	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V_{IH}	V_{SS} -1.5	-	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} -15	-	0.8	V	
Output Logic "1"	V_{OH}	V_{SS} -1.5	-	-	V	I_{OH} = 100 μA
Output Logic "0"	V_{OL}	-	-	0.8	V	I_{OL} = 1.6 mA for V_{SS} = 5V
Input Leakage	I_L	-	2	10	μA	V_{IN} = V_{SS} -15
Output Leakage	I_O	-	2	10	μA	Chip deselected
Power Supply Current						
Read	I_{GG}	-	8	10	mA	I_{SS} approx. I_{GG}
Write	I_{GG}	-	6	7	mA	I_{SS} approx. I_{GG}
Erase	I_{GG}	-	4	6	mA	I_{SS} approx. I_{GG}
Deselected	I_{GG}	-	3	4	mA	I_{SS} approx. I_{GG}
AC CHARACTERISTICS						
Access Time	t_{ACC}	-	-	4.0	μs	
Clock Pulse width	t_{PW}	2.0	-	20.0	μs	
Erase Cycle Time	t_E	50	-	200.0	ms	
Write Cycle Time	t_W	50	-	200.0	ms	
Read Cycle Time	t_R	4.0	-	24.0	μs	
Address-Clock Time	t_A	50	-	-	ns	
Control-Enable Time	t_{CE}	50	-	-	ns	
Data Set Up Time	t_{DS}	50	-	-	ns	
Data Hold Time	t_{DH}	50	-	-	ns	
Number of Read's/Word Refresh	N_{RA}	10^{11}	-	-	-	
Number of Erase/Write Cycles	N_W	10^6	-	-	-	
Input Capacitance, all pins	C_{IO}	-	6	10	pF	
Unpowered Data Storage Time	t_S	10	-	-	Years	
Power Dissipation Read Cycle	P_D	-	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = -29
Pulse Rise, fall time	t_{R1} t_F	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

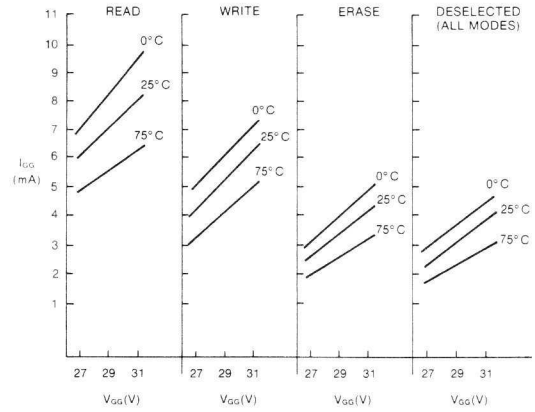
TIMING DIAGRAM



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SUPPLY CURRENT VS POWER SUPPLY VOLTAGE



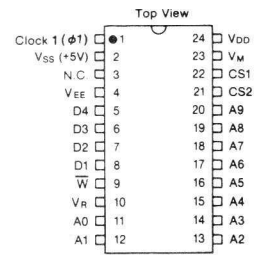
4096 Bit Electrically Alterable Read Only Memory

FEATURES

- 1024 x 4 Organization
- 10-Bit Binary Addressing
- 2 Chip Select Inputs
- Electrically Reprogrammable
- 2 μs Access Time
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible

PIN CONFIGURATION

24 LEAD DUAL IN LINE



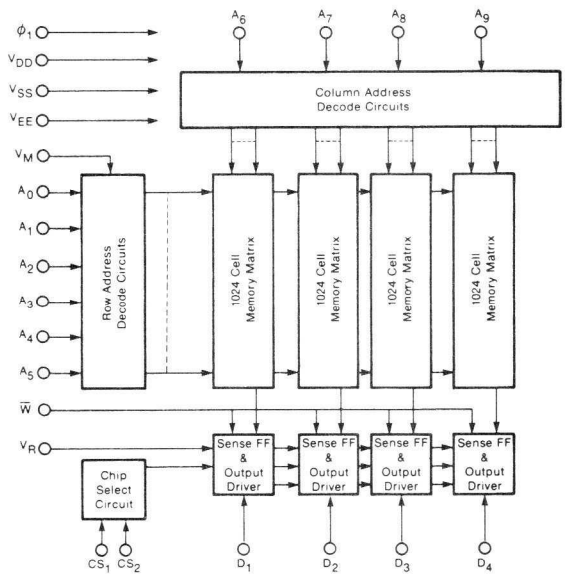
DESCRIPTION

The ER2401A is a fully decoded, 1024 x 4-bit electrically erasable and reprogrammable ROM utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 4096 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Stored data may be accessed a minimum of 2 x 10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a V_{SS}–28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^6 times. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS} . . . . . +0.3V to -30V
Operating ambient temperature . . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Soldering temperature of leads (10 seconds) . . . . . +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to +70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	V_{SS}	V_{SS}	V_{SS}	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to +70°C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1=V_{DD}=V_{SS}$-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	$V_{DD}=V_{SS}$-29, $\overline{W}=V_{SS}$-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase substrate leakage current at V_{SS}-28V	$\overline{W}=V_{SS}$-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V	Outputs open (See Figure 6)	—	8.5	12	mA
I_{DD2}	V_{DD} supply current - write mode at V_{SS}-28V	Outputs open (See Figure 5)	—	18	25	mA
I_{OH}	Data output high current - TTL load	One Series 7400 TTL load with R_S=2K, $V_{CC}=V_{SS}$	-2.0	—	—	mA
I_{OL}	Data output low current - TTL load	(See TTL Notes)	+3.2	—	—	mA
V_{OH}	Data Output high voltage — MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L=100 pF	—	—	V_{SS}-10	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	10	—	—	Years

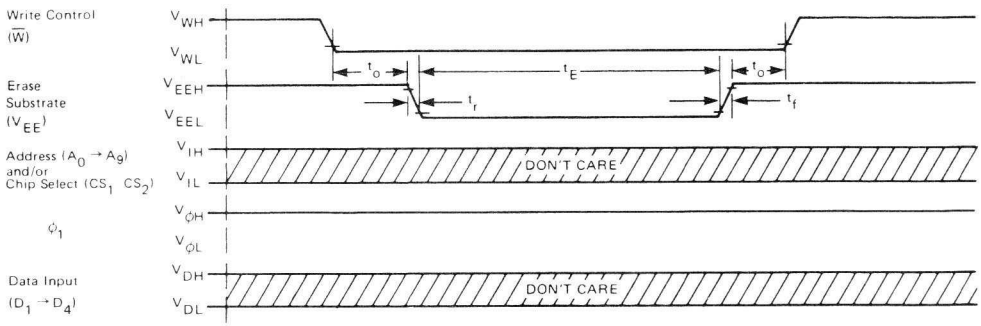
CAPACITANCE AT $V_{IN}=V_{SS}$, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pF
C_W	Write control input capacitance	—	10	20	pF
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pF
C_{EE}	Erase substrate capacitance	—	600	700	pF
C_D	Data input/output capacitance	—	6	10	pF

MEMORY

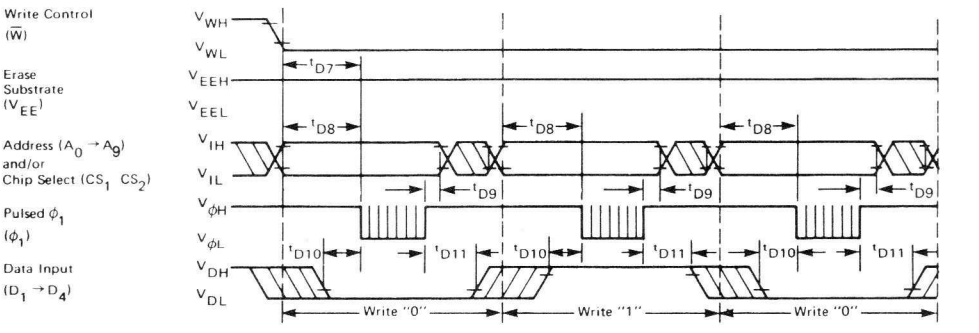
ERASE CYCLE CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_o	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS, T_A = 0°C to +70°C (SEE NOTE 3)

Symbol	Parameter	Min	Typ	Max	Units
$N\phi_W$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^6	—

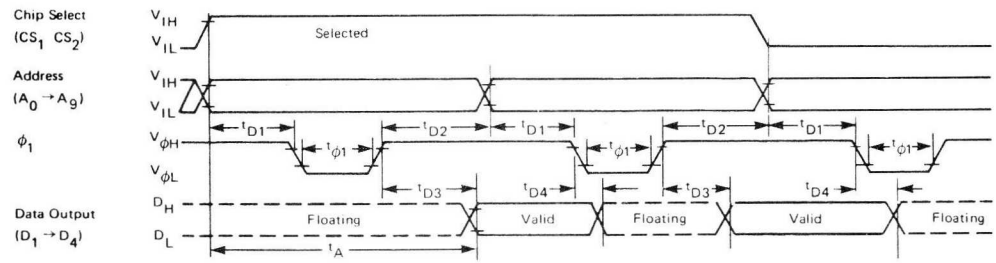


NOTES:

1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec. may result in a floated output condition. Consequently data must be resampled with a 40 μsec. time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25°C and nominal voltages.

READ CYCLE CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units
T_A	Access time (ER2401A)	—	—	2.0	μs
$t\phi_1$	Pulse width (rise and fall times ≤50 ns) (See Note 1)	850	—	2000	ns
t_{D1}	Address and chip select change to ϕ fall delay	400	—	—	ns
t_{D2}	ϕ_1 Rise to address and chip select change delay	0.0	—	—	μs
t_{D3}	ϕ_1 Rise to data output valid delay (See Notes 1 and 2)	—	—	750	ns
t_{D4}	ϕ_1 Fall to floated output delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



MEMORY

TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C, R_S = 2K Ohms, V_{SS} = OV

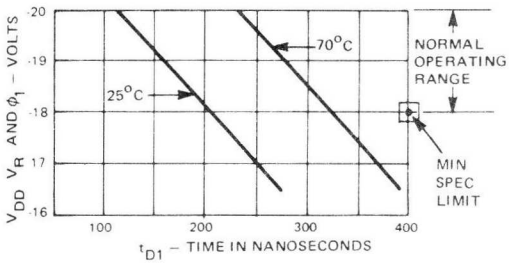


Fig.1 TYPICAL ϕ1 DELAY IN NANOSECONDS VS. POWER SUPPLY VOLTAGE

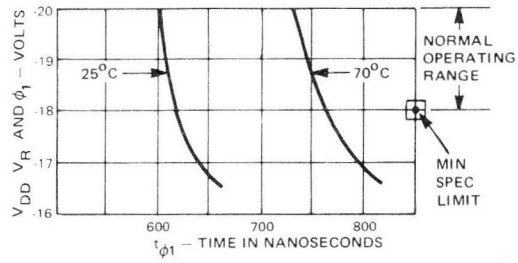


Fig.2 TYPICAL ϕ1 WIDTH IN NANOSECONDS VS. POWER SUPPLY VOLTAGES

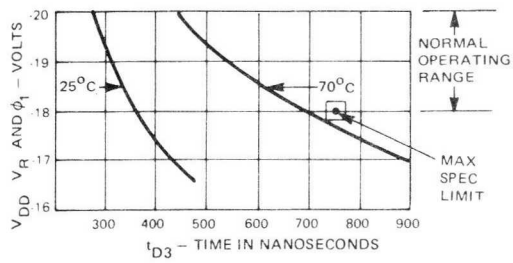


Fig.3 TYPICAL DATA SETUP TIME IN NANOSECONDS VS. POWER SUPPLY VOLTAGES

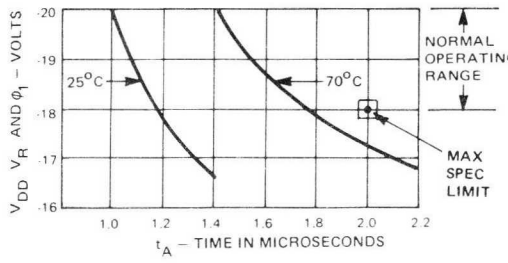


Fig.4 TYPICAL ACCESS TIME IN MICROSECONDS VS. POWER SUPPLY VOLTAGES

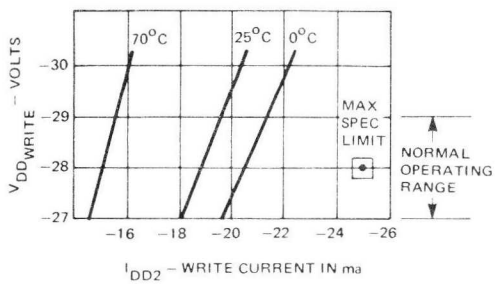


Fig.5 TYPICAL WRITE CURRENT IN MILLIAMPS VS. POWER SUPPLY VOLTAGES
(For deselected, I_{DD2} = ½ Graph I_{DD2})

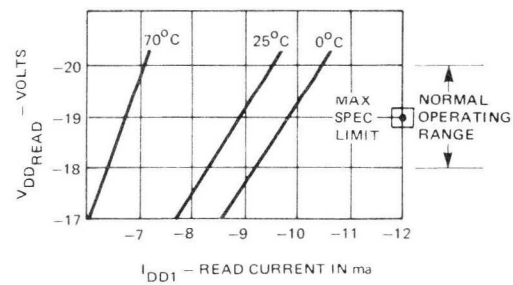


Fig.6 TYPICAL READ CURRENT IN MILLIAMPS VS. POWER SUPPLY VOLTAGE
(Chip selected or deselected)

PIN FUNCTIONS

Chip Select (CS1, CS2)
Both must be in the high state to enable the data output terminals or write data into the device.

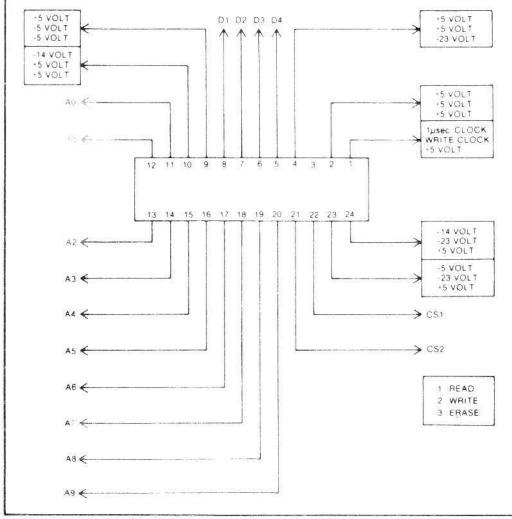
Data Input/Output (D1—D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

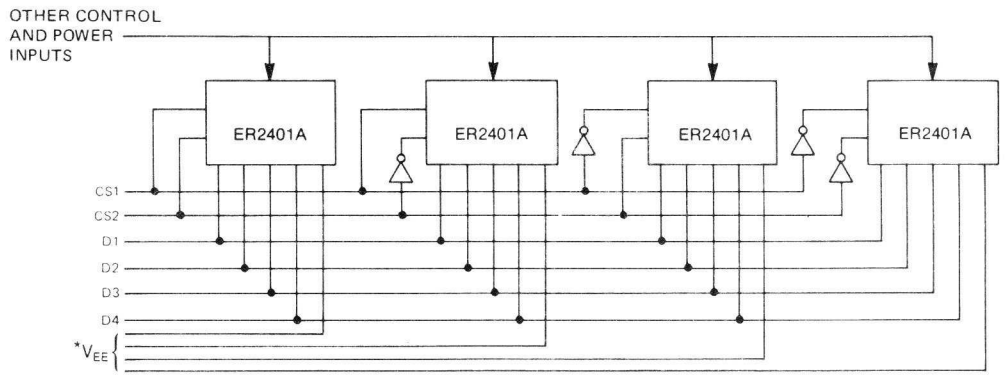
Phase One (ϕ1)
During the write and read operations, pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltage to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible.

NOTE: All control, address and data inputs are TTL-compatible with pull-up resistors.

ER2401A OPERATION

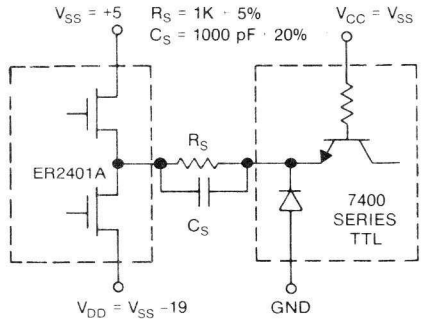


A 4096 × 4 EAROM SUBSYSTEM ORGANIZATION

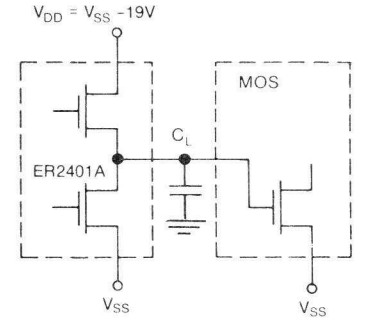


*V_{EE} MUST BE ISOLATED FOR INDIVIDUAL ERASE. MAY BE CONNECTED FOR BULK ERASE.

TTL INTERFACE



MOS INTERFACE



MEMORY

8192 Bit Electrically Alterable Read Only Memory

FEATURES

- 2048 x 4 Organization
- 11-Bit Binary Addressing
- Chip Select Input
- Electrically Reprogrammable
- 1.65 μs Access Time (ER2805)
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible.

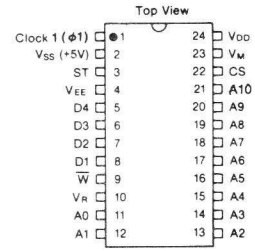
DESCRIPTION

The ER2805 is a fully decoded 2048 x 4-bit electrically erasable and reprogrammable ROM utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

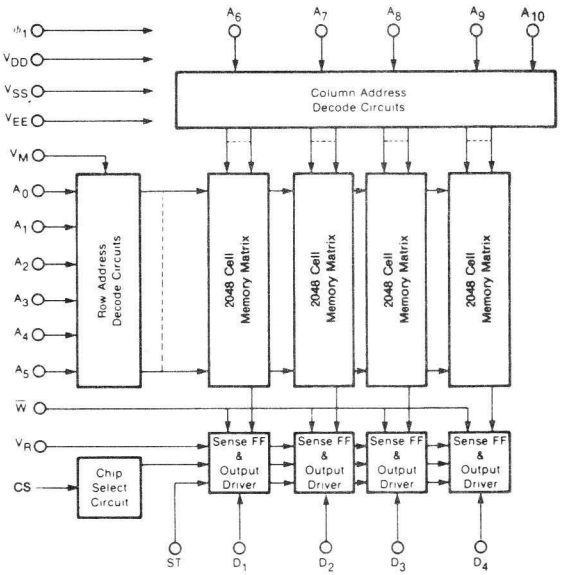
PIN CONFIGURATION

24 LEAD DUAL IN LINE



Stored data may be accessed a minimum of 2×10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a V_{SS}–28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^6 times. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS} . . . . . +0.3V to -30V
Operating ambient temperature . . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Soldering temperature of leads (10 seconds) . . . . . +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to +70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	V_{SS}	V_{SS}	V_{SS}	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{STH}	Strobe input high voltage	—	V_{SS}	—	Not Applicable			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{STL}	Strobe input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to +70°C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi1$=V_{DD}=V_{SS}-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	V_{DD}=V_{SS}-29, ST=$\overline{W}$=V_{SS}-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase leakage current at V_{SS}-28V	$\overline{W}$=ST=V_{SS}-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V ER2805	Outputs open (See Figure 6)	—	11	13	mA
I_{DD2}	V_{DD} supply current - Write mode at V_{SS}-28V ER2805	Outputs open (See Figure 5)	—	24	27	mA
I_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1K, V_{CC}=V_{SS}	V_{SS}-1.5	—	—	V
I_{OL}	Data output low voltage - TTL load	(See TTL Notes)	—	—	V_{SS}-6.6	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L=100 pF	—	—	V_{SS} -7	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	10	—	—	Years

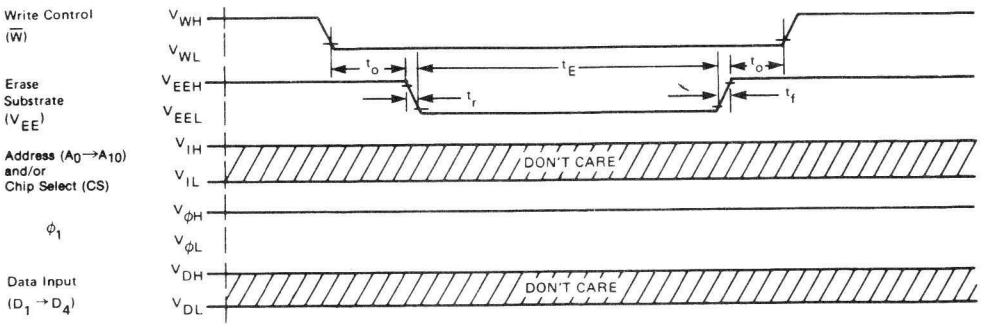
CAPACITANCE AT V_{IN} = V_{SS}, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pF
C_W	Write control input capacitance	—	10	20	pF
C_{ST}	Strobe input capacitance	—	10	15	pF
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pF
C_{EE}	Erase substrate capacitance	—	600	700	pF
C_D	Data input/output capacitance	—	6	10	pF

MEMORY

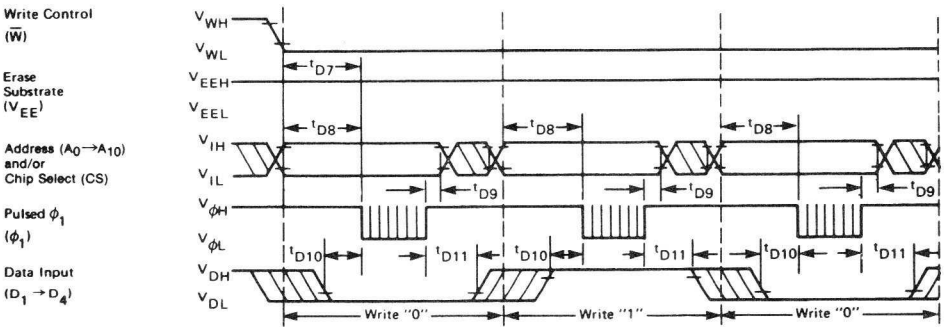
ERASE CYCLE CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_o	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS, T_A=0°C to +70°C (ST=V_{DD}) (SEE NOTE 3)

Symbol	Parameter	Min	Typ	Max	Units
$N\phi_W$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^6	—

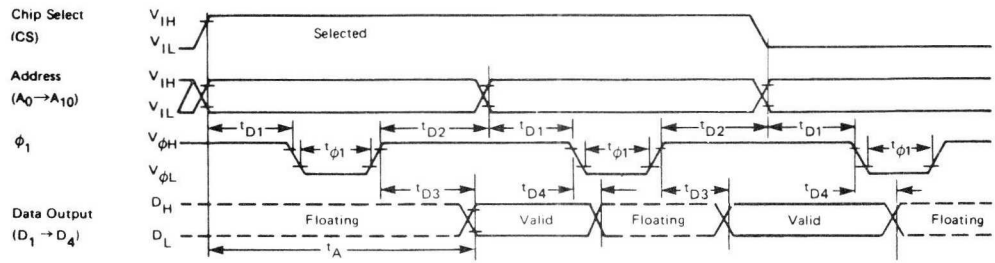


NOTES:

1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec. may result in a floated output condition. Consequently data must be resampled with a 40 μsec. time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25°C and nominal voltages.
5. ST and ϕ pulses are required after the fall of the chip select line to force the data outputs into a high impedance state.

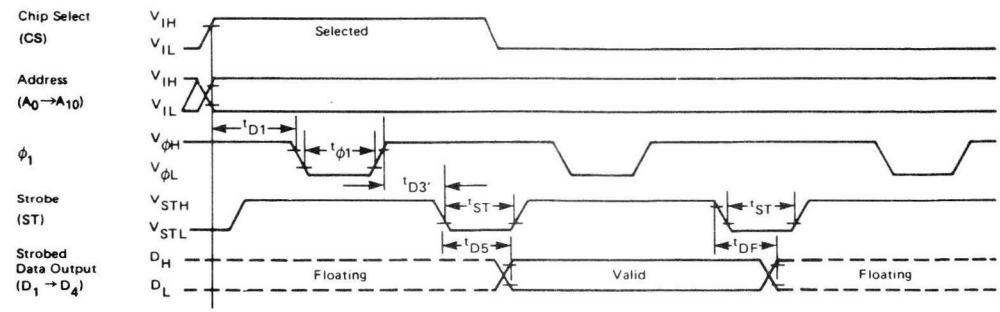
READ CYCLE CHARACTERISTICS FOR NON-STROBED OPERATION, $T_A = 0°C$ to $+70°C$ ($ST = V_{DD}$)

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units
T_A	Access time (strobe=V_{DD})	—	1.2	1.65	μs
$t_{\phi 1}$	Pulse width (rise and fall times ⩽50ns) (See Note 1)	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 fall delay	400	—	—	ns
t_{D2}	ϕ_1 Rise to address and chip select change delay	50	—	300	ns
t_{D3}	ϕ_1 Rise to data output valid delay (See Notes 1 and 2)	—	—	550	ns
t_{D4}	ϕ_1 Fall to floated output delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



READ CYCLE CHARACTERISTICS FOR STROBED OPERATION, $T_A = 0°C$ to $+70°C$

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ⩽50ns) (See Note 1)	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 fall delay	400	—	—	ns
$t_{D3'}$	ϕ_1 Rise to strobe rise delay	0.75	—	—	μs
t_{ST}	Strobe pulse width (rise and fall ⩽50 ns)	500	—	—	ns
t_{D5}	Strobe fall to strobed data output valid delay (See Notes 1 and 2)	—	—	500	ns
t_{DF}	Strobe fall to strobed floated output on deselect delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C, R_S = 2K Ohms, V_{SS} = OV

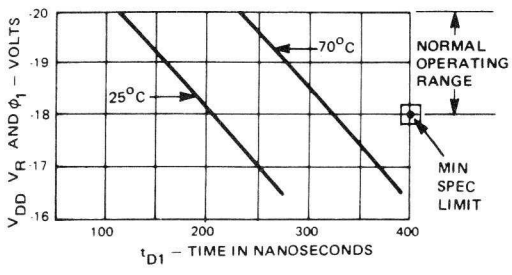


Fig. 1 TYPICAL ϕ1 DELAY IN NANOSECONDS vs. POWER SUPPLY VOLTAGE

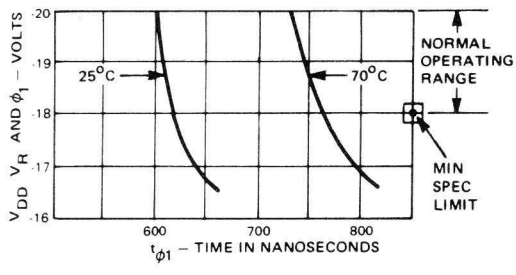


Fig. 2 TYPICAL ϕ1 WIDTH IN NANOSECONDS vs. POWER SUPPLY VOLTAGES

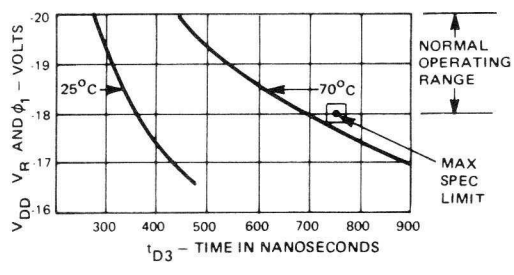


Fig. 3 TYPICAL DATA SETUP TIME IN NANOSECONDS vs. POWER SUPPLY VOLTAGES

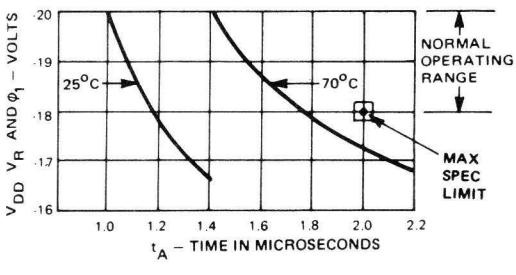


Fig. 4 TYPICAL ACCESS TIME IN MICROSECONDS vs. POWER SUPPLY IN VOLTAGES

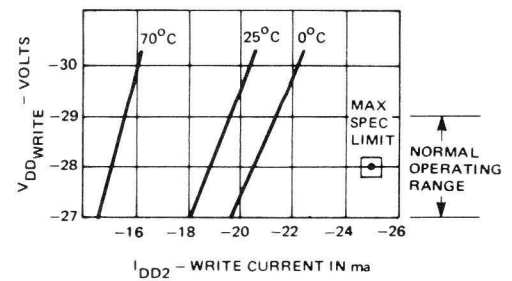


Fig. 5 TYPICAL WRITE CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGES (Deselected I_{DD2} = ½ Graph I_{DD2})

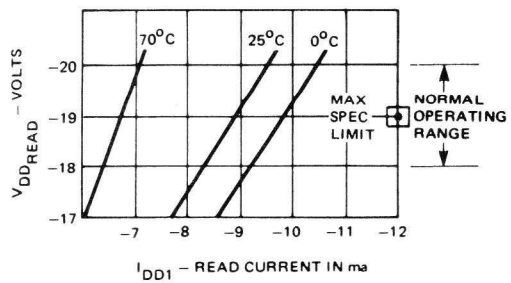


Fig. 6 TYPICAL READ CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGE (Chip selected or deselected)

PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or write data into the device.

Data Input/Output (D1—D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition, after first ST and ϕ pulses.

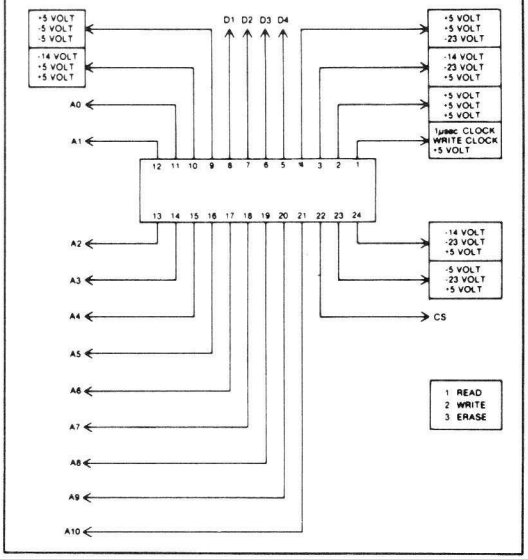
Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

Strobe (ST)
A strobe input is provided for delayed data clockout. In applications where this feature is not desired, the strobe terminal should be maintained at VDD throughout the entire read cyle. The ST input is high-level and not TTL-compatible.

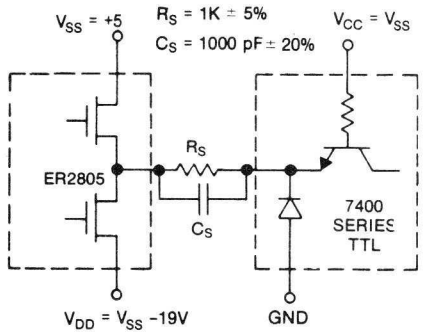
Phase One (ϕ1)
During the write and read operations, pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltage to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible.

NOTE: All control, address and data inputs are TTL-compatible with pull-up resistors.

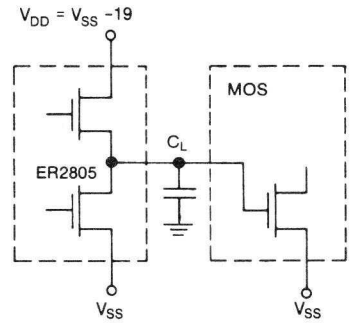
ER2805 OPERATION



TTL INTERFACE



MOS INTERFACE



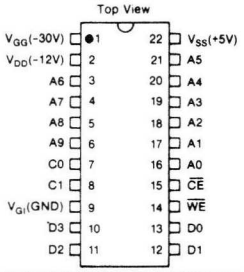
4096 Bit High Speed Electrically Alterable Read Only Memory

FEATURES

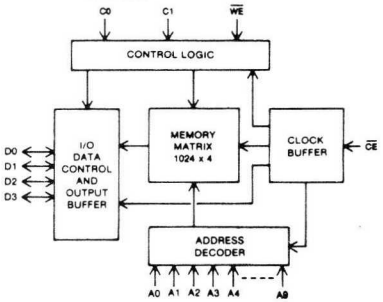
- 1024 × 4 Organization, Fully Decoded
- Single Word or Block Electrically Erasable
- TTL Compatible with Resistor Pull-ups
- Three State Output
- ER3400: 900ns Access Time
- 1.8 μs Cycle Time
- 10 ms Word or Block Erase Time
- 1 ms Write Time
- 22 Pin DIP
- P-Channel Metal Gate MNOS Technology
- 0° C to 70° C Operation
- +5, -12, -30V Power Supplies
- 10^5 Erase-Write Cycles per Word
- 2×10^{11} Read Cycles per Word
- 10 Year Unpowered Nonvolatile Data Storage

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The ER3400 is a word alterable ROM intended for use as a read-mostly memory. It operates with one clock, CHIP ENABLE ($\overline{CE}$), which also serves for chip selection. All other pins of the device can be paralleled with other EAROMs.

Any one of four possible operating modes can be selected by setting the proper binary code on the C0-C1 control lines and pulsing the device with $\overline{CE}$. The four modes are Read, Write, Word Erase and Block Erase. The ER3400 will sense the control lines and change modes only when pulsed by $\overline{CE}$. When in the Read mode, data is read during each $\overline{CE}$ pulse. Writing or erasing of a word continues for as long as the device is in the Write or Erase mode. Each write or erase word cycle must be ended by a dummy read operation. The ER3400 may be permanently damaged if the dummy read cycle is missing or significantly delayed.

A WRITE ENABLE ($\overline{WE}$) input pulse indicates to the ER3400 that the data on the D_0-D_3 data input/output lines is valid input data. This data is then stored internally for use during the write operation.

Although the ER3400 has circuitry to protect it from altering data during power up or down, surrounding logic does not have such protection and may generate errroneous erase or write control signals. It is therefore recommended that V_{GG} be turned on after V_{SS} and turned off while V_{SS} is still within spec. This will absolutely guarantee memory retention.

The ER3400 may be operated in read-only mode at a reduced power level by having $V_{GG} = V_{SS} = +5$ Volts.

PIN FUNCTIONS

A_0-A_9	10-Bit Word Address
D_0-D_3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C_0, C_1	Mode Control Inputs
	C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_{GG}
(with respect to V_{SS}) ..... −20V to +0.3V
Storage temperature (with data retention) ..... −40°C to +70°C
Storage temperature (without data retention) .... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +5V ±5%
V_{DD} = -12V ±5%
V_{GG} = -30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to =70°C

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V_{IH}	V_{SS}-1.5	—	V_{SS}+0.3	Volts	
Input Logic "0"	V_{IL}	-10	—	0.8	Volts	
Output Logic "1"	V_{OH}	V_{SS}-1.5	—	—	Volts	I_{OH} = -2mA
Output Logic "0"	V_{OL}	—	—	0.4	Volts	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	-2.0	μA	V_{IN} = V_{SS} -15 Volts
Data Input Leakage	I_{LD}	—	—	-10.0	μA	V_{IN} = V_{SS} -15 Volts
Power Supply Current						
V_{DD} Supply Current: Chip selected	I_{DD}	—	—	-25.0	mA	V_{DD} = V_{SS} -17 Volts
Chip de-selected	I_{DD}	—	—	−12.0	mA	V_{DD} = V_{SS} -17 Volts
V_{GG} Supply Current: Write mode	I_{GG}	—	—	−4.0	mA	V_{GG} = V_{SS} -35 Volts
V_{SS} Supply Current: Chip selected	I_{SS}	—	—	−31.0	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
Chip de-selected	I_{SS}	—	—	-11.5	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
AC CHARACTERISTICS						
Input capacitance - control inputs	C_I	—	6	8	pF	
Input capacitance - data inputs	C_D	—	8	10	pF	
Read Mode Characteristics						
Address and control to $\overline{CE}$	t_{D1}	0	—	—	ns	
Address and control hold time	t_{D2}	250	—	—	ns	
$\overline{CE}$ to Data I/O Off	t_{D3}	50	—	200	ns	
$\overline{CE}$ high	t_{D4}	900	—	—	ns	
Access time	t_A	—	—	900	ns	RL = 2K to V_{SS}, CL = 100pf
$\overline{CE}$ pulse width	$t_{\overline{CE}}$	900	—	50,000	ns	
Read cycle time	t_{CY}	1800	—	—	ns	
$\overline{CE}$ rise, fall time	t_r, t_f	10	—	100	ns	
Write/Erase Mode Characteristics						
Address and control to $\overline{CE}$	t_{D11}	0	—	—	ns	
Address and control hold time	t_{D12}	250	—	—	ns	
$\overline{CE}$ fall to $\overline{WE}$ fall delay	t_{D13}	0	—	200	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{WE}$ rise to $\overline{CE}$ rise delay	t_{D14}	-50	—	200	ns	
Data stable to $\overline{WE}$	t_{D15}	0	—	—	ns	
$\overline{WE}$ rise to End of Data Stable	t_{D16}	100	—	—	ns	
$\overline{CE}$ pulse width	$t_{\overline{CE}}$	900	—	50,000	ns	
WE pulse width	$t_{\overline{WE}}$	500	—	—	ns	
Write time	t_W	1	—	2	ms	
Erase time	t_E	10	—	20	ms	

**Typical values are at +25°C and nominal voltages.

MEMORY

TIMING DIAGRAMS

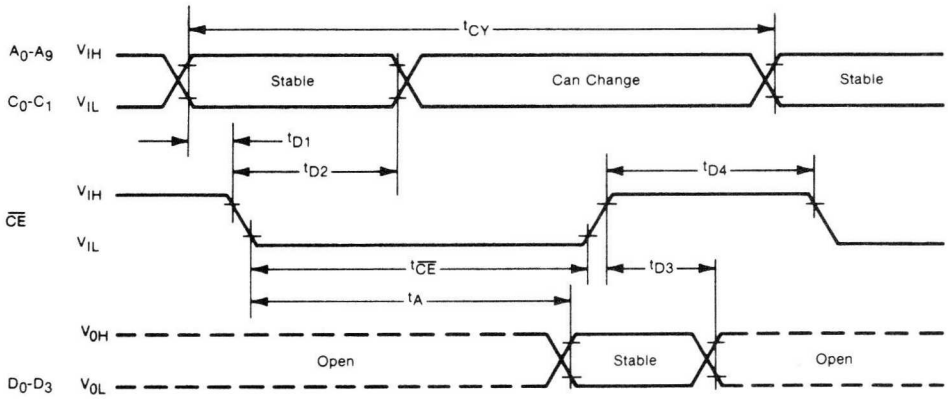


Fig.1: READ MODE TIMING

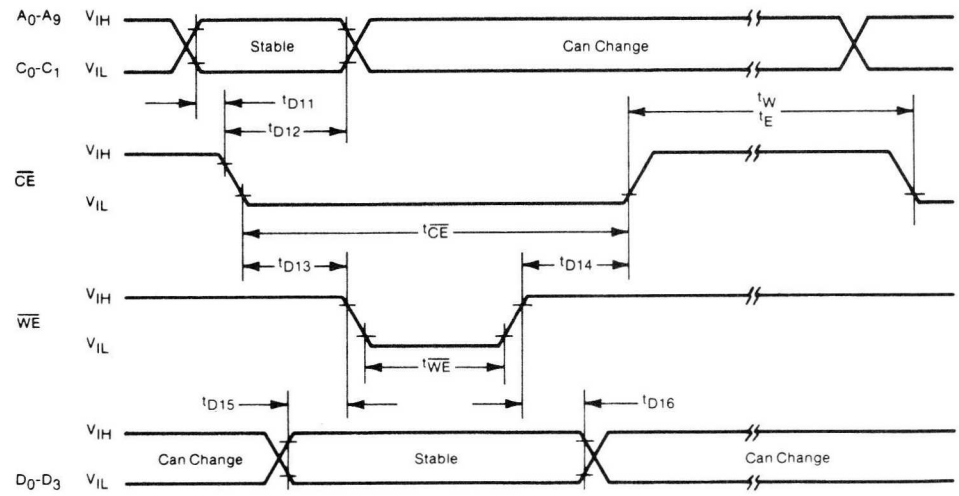


Fig.2: WRITE AND ERASE MODE TIMING

TYPICAL CHARACTERISTIC CURVES

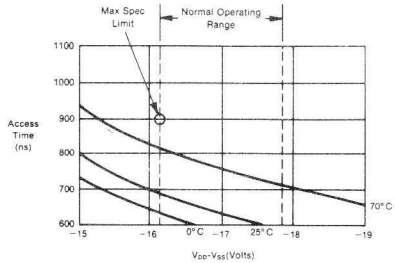


Fig.3: TYPICAL ACCESS TIME vs. POWER SUPPLY VOLTAGE

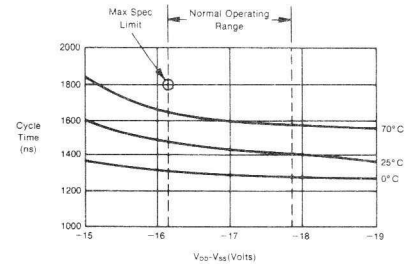


Fig.4: TYPICAL CYCLE TIME vs. POWER SUPPLY VOLTAGE

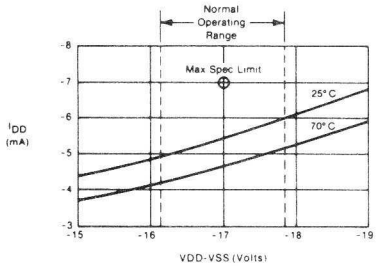


Fig.5: I_{DD} vs. V_{DD}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

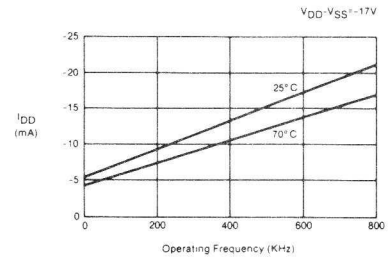


Fig.6: I_{DD} vs. OPERATING FREQUENCY IN READ MODE AND SELECTED

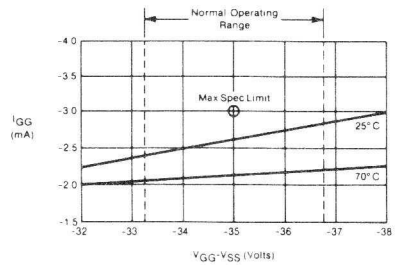


Fig.7: I_{GG} vs. V_{GG}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

READ ONLY MEMORIES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
2K ROM	2,560 bits organized 512 x 5	RO-3-2560	4-42
4K ROM	4,096 bits organized 512 x 8	RO-3-4096	4-44
5K ROM	5,120 bits organized 512 x 10	RO-3-5120	4-46
8K ROM	8,192 bits organized 2,048 x 4	RO-5-8192	4-48
16K ROM	16,384 bits organized 2,048 x 8	RO-3-8316A	4-51
		RO-3-8316B	4-51
		RO-3-9316A	4-51
		RO-3-9316B	4-51
		RO-3-9316C	4-51
	16,384 bits organized 4,096 x 4	RO-3-16384	4-60
32K ROM	32,768 bits organized 4,096 x 8	RO-3-9332A	4-56
		RO-3-9332B	4-56
		RO-3-9332C	4-56
64K ROM	65,536 bits organized 8,192 x 8	RO-3-9364B	4-59

2560 Bit Static Read Only Memory

FEATURES

- 512×5 Organization—ideal for many general purpose applications.
- Single +5 Volt Supply.
- TTL Compatible—all inputs and outputs.
- Static Operation—no clocks required.
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs—under the control of an 'Output Inhibit' input to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs
- Glass Passivation Protection

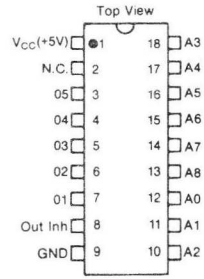
DESCRIPTION

The General Instrument RO-3-2560 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for many general purpose memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2560 can store a full 512 words of 5 bits each.

The RO-3-2560 is one of a family of 512 word Read-Only Memories offered by General Instrument; two others are the RO-3-4096, with a 512×8 memory organization, and the RO-3-5120, with a 512×10 memory organization.

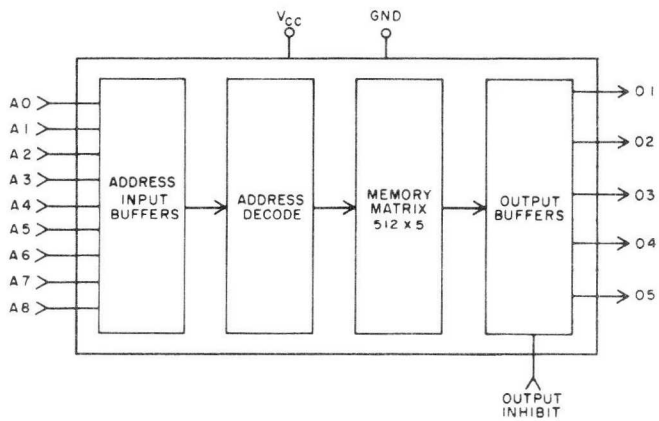
PIN CONFIGURATION

18 LEAD DUAL IN LINE



A separate publication, "RO-3-2560 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2560 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

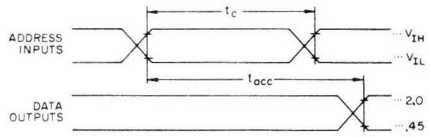
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF

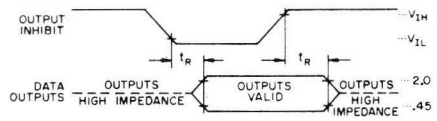
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current	I_{CC}	—	25	33	mA	Outputs Open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT-
OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME
(ADDRESS INPUTS STABLE)

MEMORY

4096 Bit Static Read Only Memory

FEATURES

- 512×8 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns. Maximum Access Time
- 150 mW Typical Power
- Tri-State Outputs—under conrol of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

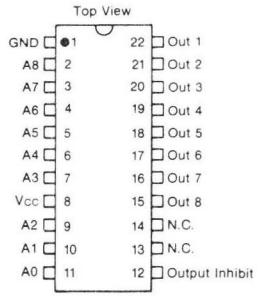
DESCRIPTION

The General Instrument RO-3-4096 is a 4096 bit static Read-Only-Memory. It is organized as 512 eight bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-4096 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

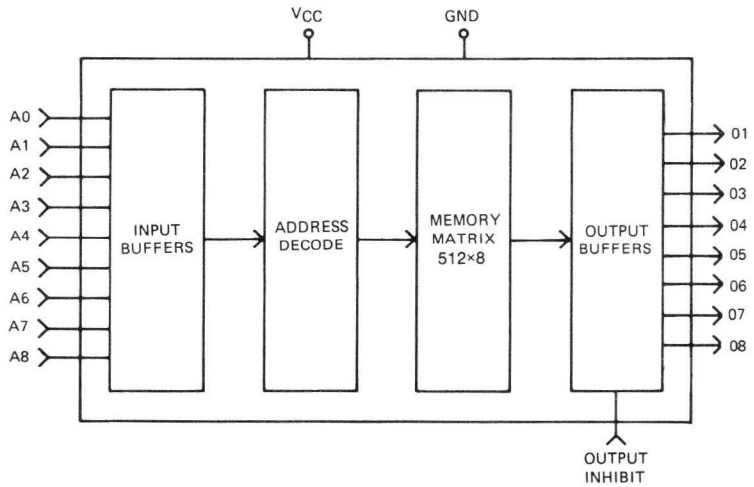
A separate publication, "RO-3-4096 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-4096 memory.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

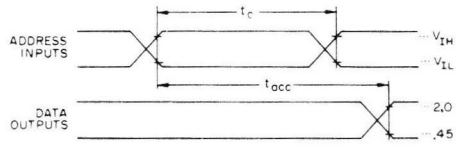
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ± 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, C_L total = 50 pF.

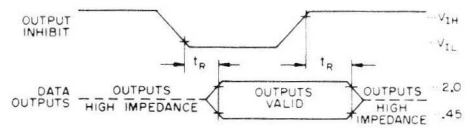
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH}=100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL}=1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current	I_{CC}	—	30	45	mA	
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_L	—	5	8	pF	f = IMHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	200	ns	
Capacitance	C_O	—	8	10	pF	f = IMHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC "0")



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

MEMORY

5120 Bit Static Read Only Memory

FEATURES

- 512×10 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns Maximum Access Time
- 150mW Typical Power
- Three-State Outputs—under control of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

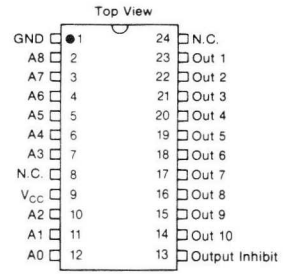
DESCRIPTION

The General Instrument RO-3-5120 is a 5120 bit static Read-Only-Memory. It is organized as 512 ten bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-5120 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

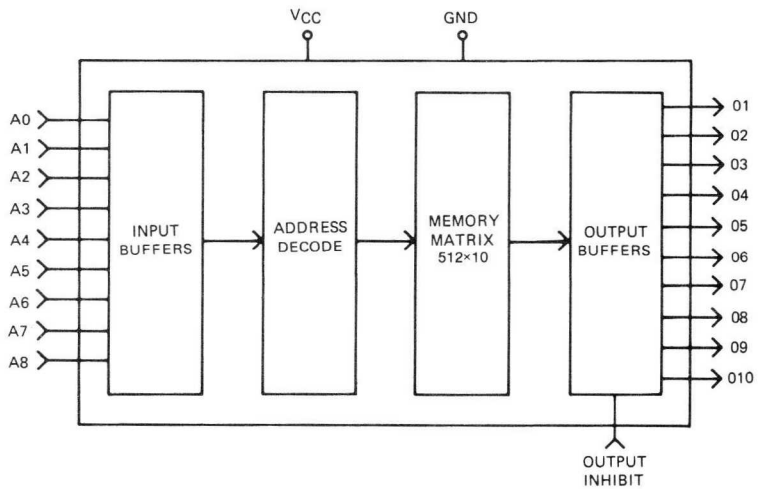
A separate publication, "RO-3-5120 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-5120 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

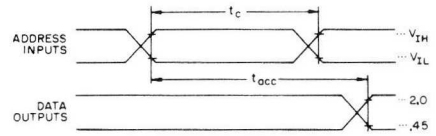
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, $C_{L\ TOTAL}$ = 50pF.

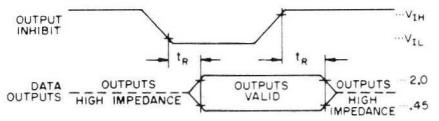
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current	I_{CC}	—	30	45	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

MEMORY

8192 Bit Read Only Memory

FEATURES

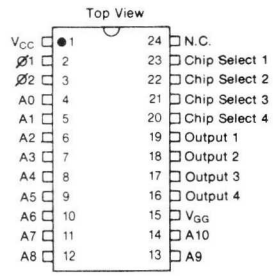
- 2048×4 Organization
- 1.2μs Typical Access Time
- TTL/DTL Compatibility—Inputs and clocks TTL/DTL compatible without external interfacing components.
- Programmable Chip Select—Simplifies design of large memory systems.
- Totally Automated Mask Generation—"RO-5-8192/Custom Coding Information", describing punched card and truth table data specification, is available from GI Sales Offices.
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

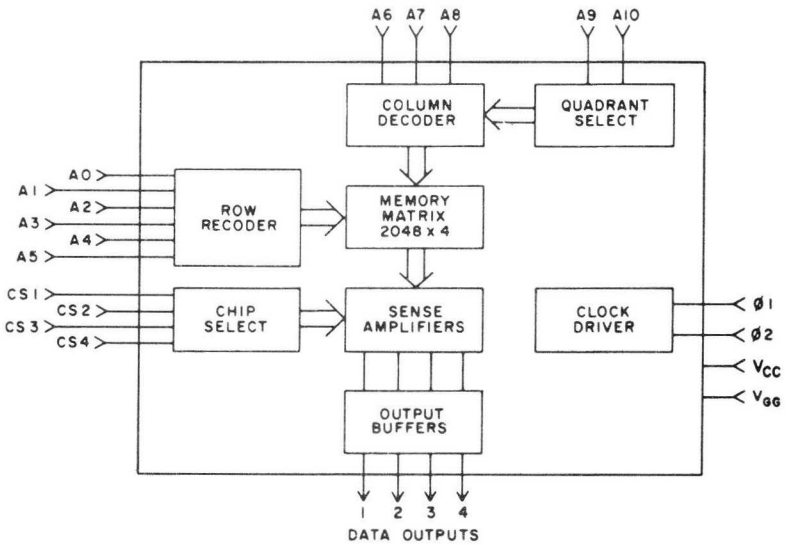
The General Instrument RO-5-8192 is an 8192-bit dynamic Read Only Memory. It is organized as 2048 four bit words and requires 11 bits of addressing. Additional features such as programmable chip select are provided for greater system flexibility. The RO-5-8192 is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. The RO-5-8192 is available pre-programmed as a 4 bit random number generator.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG}, clock and input voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified, below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
V_{GG} = −12 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: R_L = 6.8K to V_{GG}, C_L TOTAL = 100pf.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
Logic "1"	$V\phi_H$	V_{CC}−1.5	—	—	V	
Logic "0"	$V\phi_L$	—	—	+0.8	V	
Leakage	$I_L\phi$	—	—	1.0	μA	$V_{IN} = V_{CC}$−9V, T_A = +25°C
Address, Chip Select Inputs						
Logic "1"	V_{IH}	V_{CC}−1.5	—	—	V	
Logic "0"	V_{IL}	—	—	+0.8	V	
Leakage	I_{LI}	—	—	1.0	μA	$V_{IN} = V_{CC}$−9V, T_A = +25°C
Quadrant Enable Inputs[2]						
Logic "1"	V_{OH}	V_{CC}−1.5	—	—	V	
Logic "0"	V_{OL}	—	—	+0.8	V	
Data Outputs						
Logic "1"	V_{OH}	V_{CC}−1.5	—	—	V	One TTL load
Logic "0"	V_{OL}	—	—	V_{CC}−4.5	V	One TTL load
Power	P_{GG}	—	275	400	mW	
AC CHARACTERISTICS						
Clock Inputs						
Cycle Time	$t_{\phi c}$	2	—	100	μs	
ϕ1 Pulse Width	$t_{\phi 1pw}$	800	—	—	ns	$t_{\phi 1pw}$-$t_{\phi 2id} \geq$400ns
ϕ_1 Pulse Separation	$t_{\phi 1ps}$	1200	—	—	ns	
ϕ_2 Lead Time	$t_{\phi 2ld}$	400	—	—	ns	
ϕ_2 Lag Time	$t_{\phi 2lg}$	400	—	—	ns	
Rise and Fall Times	t_R,t_F	—	—	50	ns	
Capacitance	$C\phi$	—	8	10	pF	1MHz, T_A = +25°C
Inputs						
Set Up Time	t_{DS}	200	—	—	ns	
Hold Time	t_{DH}	200	—	—	ns	
Capacitance	C_I	—	5	7.5	pF	1MHz, T_A = +25°C
Data Outputs						
Propagation Delay	t_{PD}	—	0.6	1	μs	
Access Time	t_{ACC}	—	1.2	1.6	μs	(See Note)
Capacitance	C_O	—	3	5	pF	1MHz, T_A = +25°C

**Typical values are at +25°C and nominal voltages.

NOTE:
Access Time is defined as t_{DS} (min.) + $t_{\phi 2lg}$ (min.) + t_{PD} (max.)

MEMORY

LOGIC DEFINITION

Logic "1" = +5V DC or the more positive voltage
Logic "0" = 0V DC or the more negative voltage

CHIP SELECT

The RO-5-8192 is provided with four programmable bits of chip select. Constructing large memory systems with more than one 8K ROM simply requires wire-working the ROM outputs and assigning different chip select codes to each ROM chip (when a chip is not selected, its outputs are at a logic "0"—the output device is off). In addition, cascading ROMs with the same chip select code provides additional bits per word.

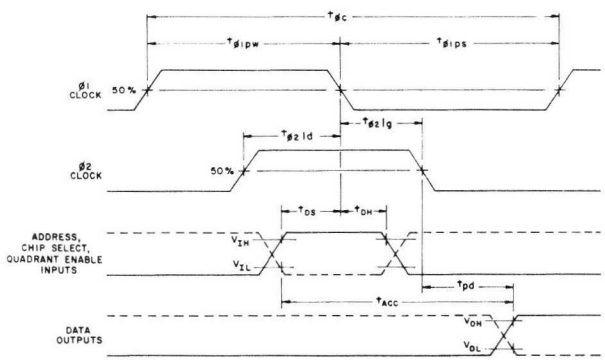
The four chip select bits are permanently programmed into the ROM at the same time as the custom data pattern. 31 different chip select codes are possible—16 unique codes and 15 additional with "don't care" variations (in the following x = 0 or 1):

CS1	CS2	CS3	CS4		
X	X	X	X	—	16 codes
DC	X	X	X	—	8 codes
DC	DC	X	X	—	4 codes
DC	DC	DC	X	—	2 codes
DC	DC	DC	DC	—	1 code

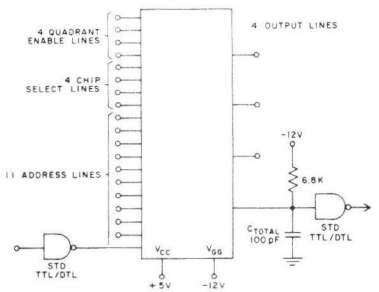
CUSTOM BIT PATTERNS

General Instrument makes use of proven computer techniques to provide fast and accurate generation of custom bit patterns. All necessary material, including the data pattern mask, test data and check lists (for customer verification), are computer-generated and cross-checked. For the full details on data specification, request the booklet "RO-5-8192/Custom Coding Information" from any GI Sales Office.

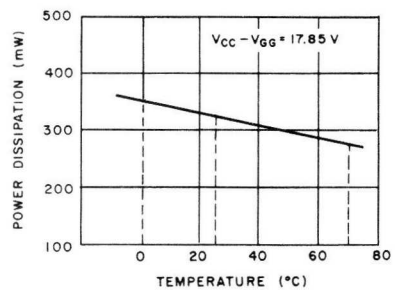
TIMING DIAGRAM



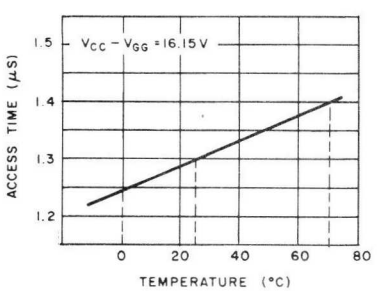
INTERFACE CIRCUIT—TTL/DTL



TYPICAL CHARACTERISTIC CURVES



POWER DISSIPATION vs. TEMPERATURE



ACCESS TIME vs. TEMPERATURE

16384 Bit Static Read Only Memories

FEATURES

- 2048×8 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs.
- Static Operation—no clocks required.
- 850ns Maximum Access Time: RO-3-8316A/9316A
- 450ns Maximum Access Time: RO-3-8316B/9316B
- 350ns Maximum Access Time: RO-3-9316C
- Three-Stage Outputs—under the control of three mask-programmable Chip Select inputs to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs.
- Glass Passivation Protection.

DESCRIPTION

The General Instrument RO-3-8316A/8316B and RO-3-9316A/9316B/9316C are 16,384 static Read Only Memories organized as 2048 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-8316A/8316B and RO-3-9316A/9316B/9316C offer the best combination of high performance, large bit storage, and simple interfacing.

The RO-3-8316A/8316B are direct replacements in pin connection and operation for the Intel 8316A and 2316A.

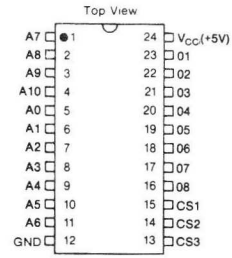
The RO-3-9316A/9316B/9316C pin configuration is identical to that of the Intel 2716 16K EPROM.

A separate publication, "RO-3-8316/9316 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming.

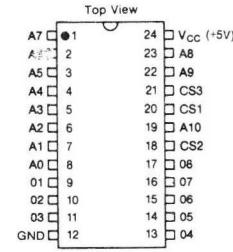
PIN CONFIGURATION

24 LEAD DUAL IN LINE

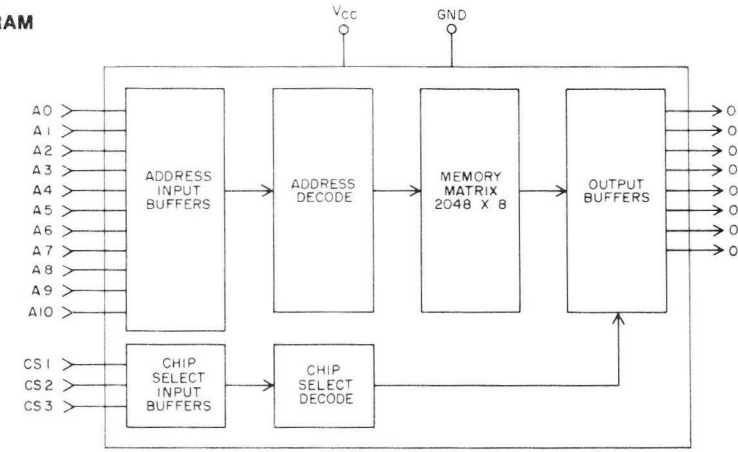
RO-3-8316A/8316B



RO-3-9316A/9316B/9316C



BLOCK DIAGRAM



MEMORY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 100pF.

RO-3-8316A/9316A, RO-3-8316B/9316B, and RO-3-9316C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 100uA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-8316A/9316A	I_{CC}	—	50	85	mA	Outputs open
RO-3-8316B/9316B	I_{CC}	—	65	95	mA	Outputs open
RO-3-9316C	I_{CC}	—	—	105	mA	Outputs open
RO-3-8316A/9316A						
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=IMHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	T_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=IMHz
RO-3-8316B/9316B						
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=IMHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=IMHz
RO-3-9316C						
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=IMHz
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=IMHz

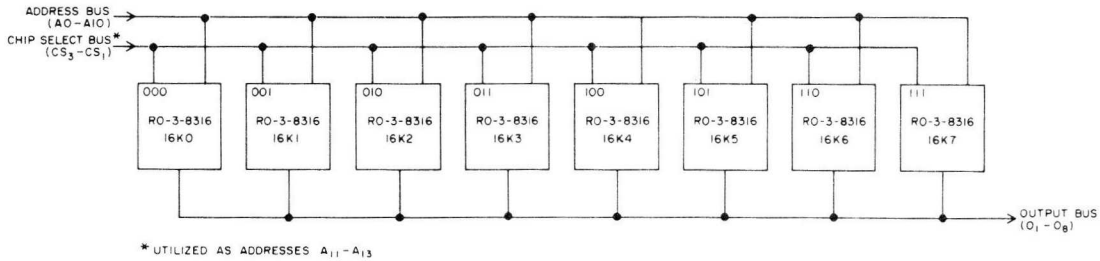
**Typical values are at +25°C and nominal voltages.

TYPICAL SYSTEM APPLICATION

A complete system of 16K words of ROM (8 bits/word) is easily obtained without any external address decoding by making use of programmable chip select features and by wiring the outputs of eight different RO-3-8316's as shown in the figure below.

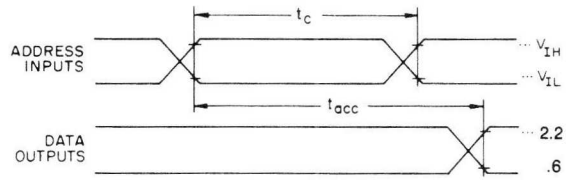
CHIP SELECT TABLE

CS 3	CS 2	CS 1	DEVICE SELECTED
0	0	0	16K0
0	0	1	16K1
0	1	0	16K2
0	1	1	16K3
1	0	0	16K4
1	0	1	16K5
1	1	0	16K6
1	1	1	16K7

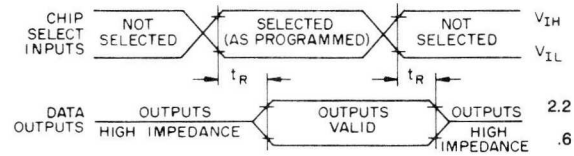


MEMORY

TIMING DIAGRAMS

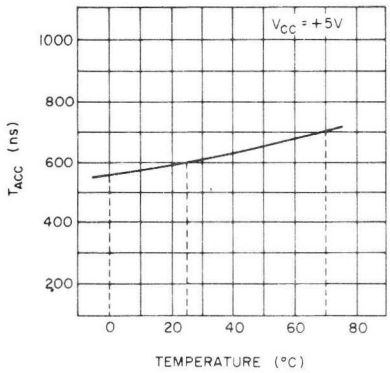


ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)

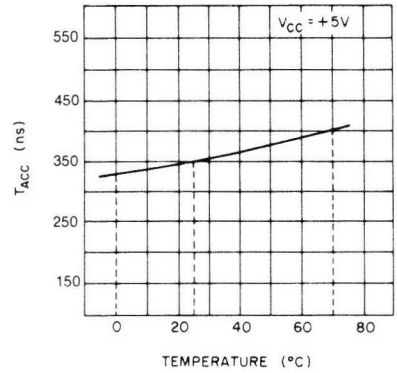


CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

TYPICAL CHARACTERISTIC CURVES

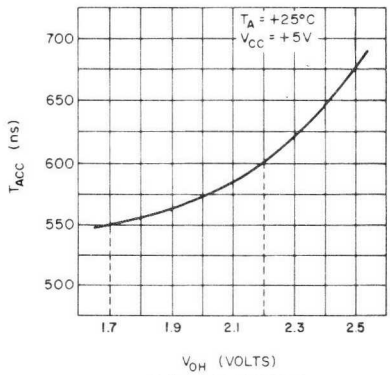


RO-3-8316A/9316A

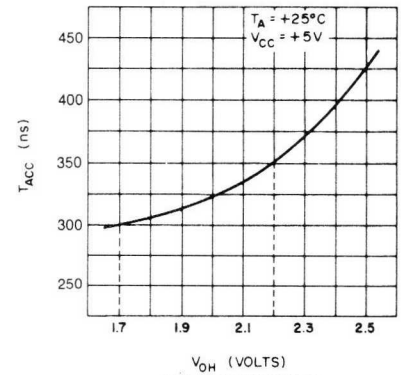


RO-3-8316B/9316B

Fig.1 ACCESS TIME VS. TEMPERATURE

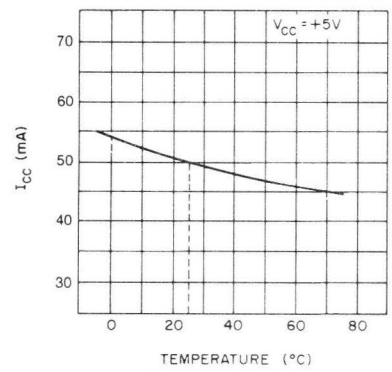


RO-3-8316A/9316A

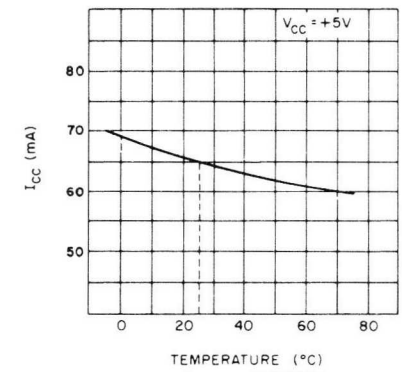


RO-3-8316B/9316B

Fig.2 ACCESS TIME VS. OUTPUT VOLTAGE



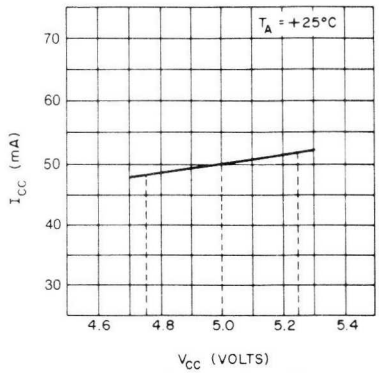
RO-3-8316A/9316A



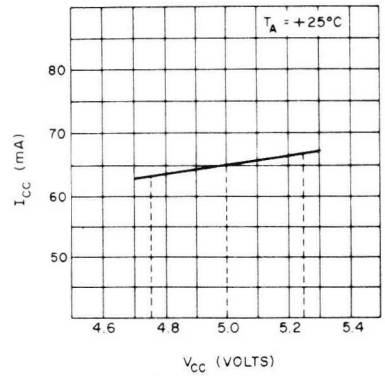
RO-3-8316B/9316B

Fig.3 POWER SUPPLY CURRENT VS. TEMPERATURE

TYPICAL CHARACTERISTIC CURVES

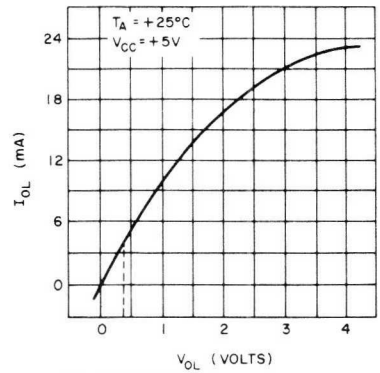


RO-3-8316A/9316A



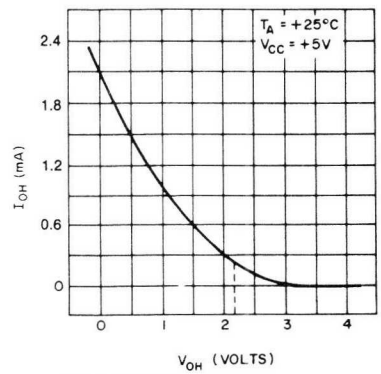
RO-3-8316B/9316B

Fig.4 POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.5 OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.6 OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

MEMORY

RO-3-9332A
RO-3-9332B
RO-3-9332C

32768 Bit Static Read Only Memory

FEATURES

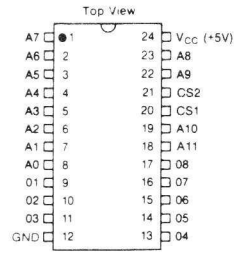
- 4096×8 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs.
- Static Operation—no clocks required.
- 850ns Maximum Access Time: RO-3-9332A
- 450ns Maximum Access Time: RO-3-9332B
- 350ns Maximum Access Time: RO-3-9332C
- Three-State Outputs—under the control of two mask-programmable Chip Select inputs to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs.
- Glass Passivation Protection.

DESCRIPTION

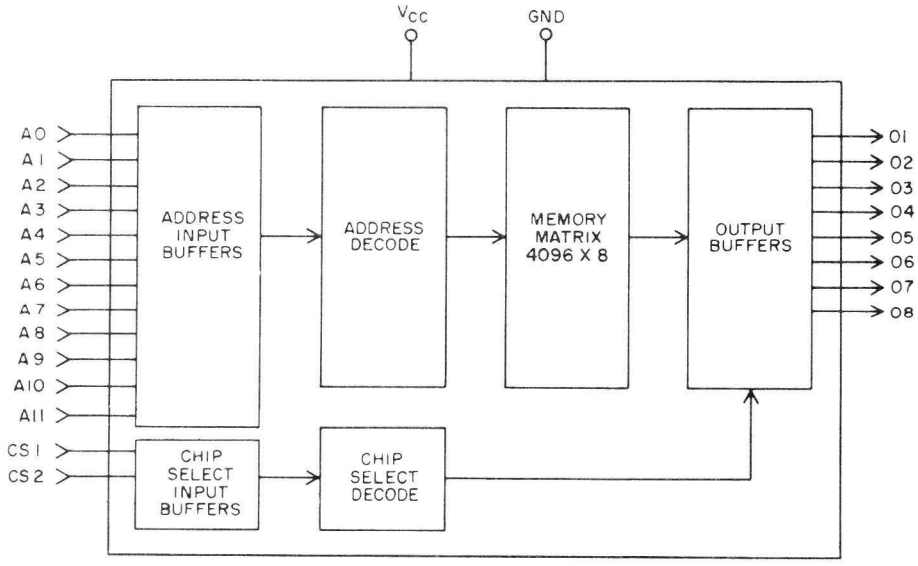
The General Instrumaent RO-3-9332A/9332B/9332C are 32,768 bit static Read Only Memories organized as 4096 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advance GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9332A/9332B/9332C offer the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memories available today.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±10%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pF

RO-3-9332A/9332B/9332C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9332A	I_{CC}	—	—	60	mA	Outputs open
RO-3-9332B	I_{CC}	—	—	125	mA	Outputs open
RO-3-9332C	I_{CC}	—	—	140	mA	Outputs open

RO-3-9332A

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	T_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

RO-3-9332B

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	450	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

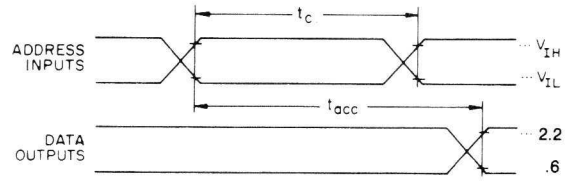
RO-3-9332C

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

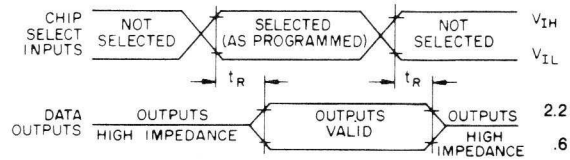
**Typical values are at +25°C and nominal voltages.

MEMORY

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

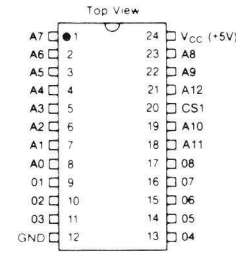
65536 Bit Static Read Only Memory

FEATURES

- 8192×8 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs.
- Edge-activated
- 450ns Maximum Access Time
- Three-State Outputs
- Totally Automated Custom Programming.
- Zener Protected Inputs.
- Glass Passivation Protection.

PIN CONFIGURATION

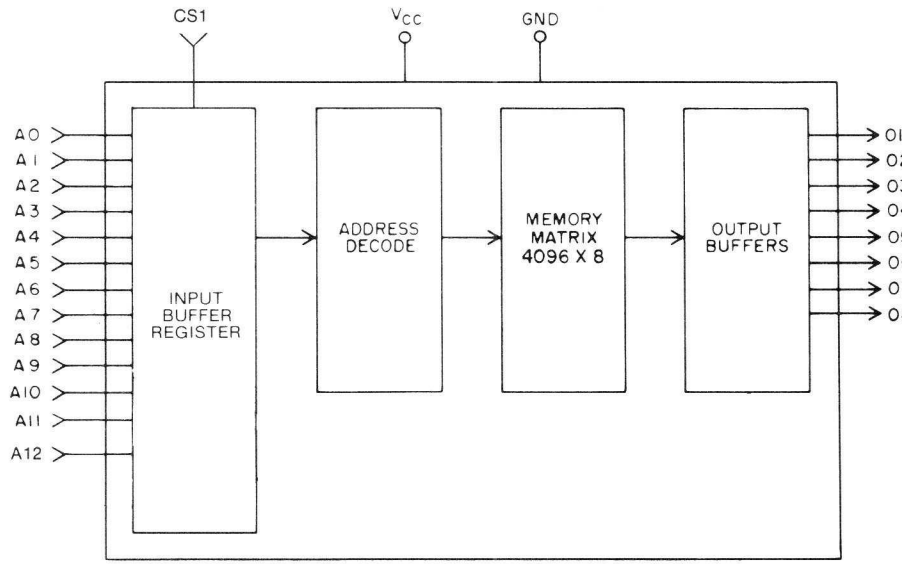
24 LEAD DUAL IN LINE



DESCRIPTION

The General Instrument RO-3-9364B is a 65,536 bit static Read Only Memory organized as 8192 eight bit words and is ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9364B offers the best combination of high performance, large bit storage, and simple interfacing.

BLOCK DIAGRAM



MEMORY

RO-3-16384

16384 Bit Static Read Only Memory

FEATURES

- 4096×4 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- Address/Chip Select Latch Input—may be used to gate in new Address or Chip Select Inputs
- 1 μs Maximum Access Time
- 250 mW Typical Power
- Three-State Outputs—under control of 3 programmable Chip Select Inputs.
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

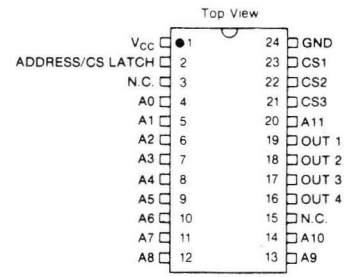
DESCRIPTION

The General Instrument RO-3-16384 is a 16,384 bit static Read-Only-Memory. It is organized as 4096 four bit words and requires 12 bits of addressing. Three programmable Chip Select inputs are provided to simplify the connection of several ROMs to a common bus. The RO-3-16384 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

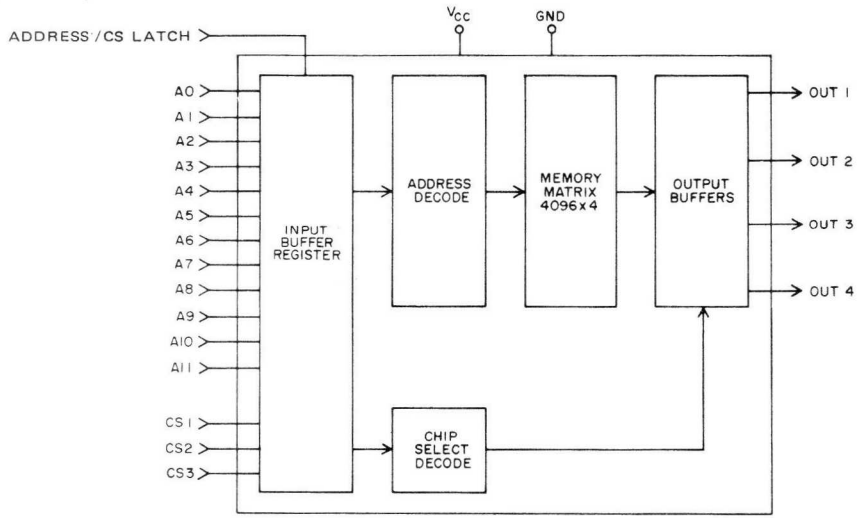
A separate publication, "RO-3-16384 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-16384 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

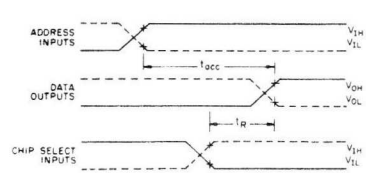
Standard Conditions: (unless otherwise noted)

V_{CC} = +5 Volts ± 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, C_L total = 50 pF.

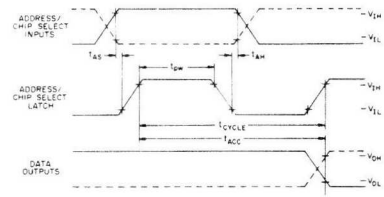
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select, Latch Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current	I_{CC}	—	50	65	mA	Outputs open
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	1.0	—	—	μs	
Set-up Time	t_{AS}	0	—	—	ns	
Hold Time	t_{AH}	200	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Latch Input						
Pulse Width	t_{PW}	200	—	—	ns	
Data Outputs						
Access Time	t_{ACC}	—	0.7	1.0	μs	
Chip Select Response Time	t_R	—	200	300	ns	Latch at +5V
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

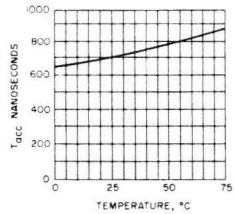


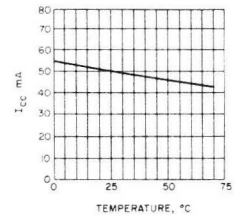
WITH LATCH INPUT HELD AT +5V

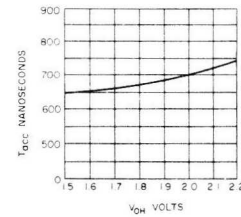


WITH LATCH INPUT UTILIZED

TYPICAL CHARACTERISTIC CURVES







MEMORY

MICRO ELECTRONICS

KEYBOARD ENCODERS/ CHARACTER GENERATORS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits	AY-5-2376	4-64
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	AY-5-3600	4-69
		AY-5-3600-PRO	4-75
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	AY-3-4592	4-78
CHARACTER GENERATORS	2,240 bits organized as 64 - 5 x 7 characters.	RO-5-2240S	4-88
	2,560 bits organized as 64 - 5 x 8 characters.	RO-3-2513	4-92
	5,184 bits organized as 64 - 9 x 9 characters.	RO-5-5184	4-97

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- External control provided for output polarity selection.
- External control provided for selection of odd or even parity.
- Two key roll-over operation.
- N-key lockout.
- Programmable coding with a single mask change.
- Self-contained oscillator circuit.
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

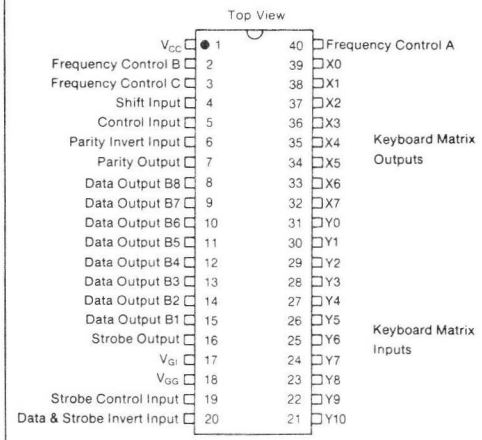
DESCRIPTION

The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

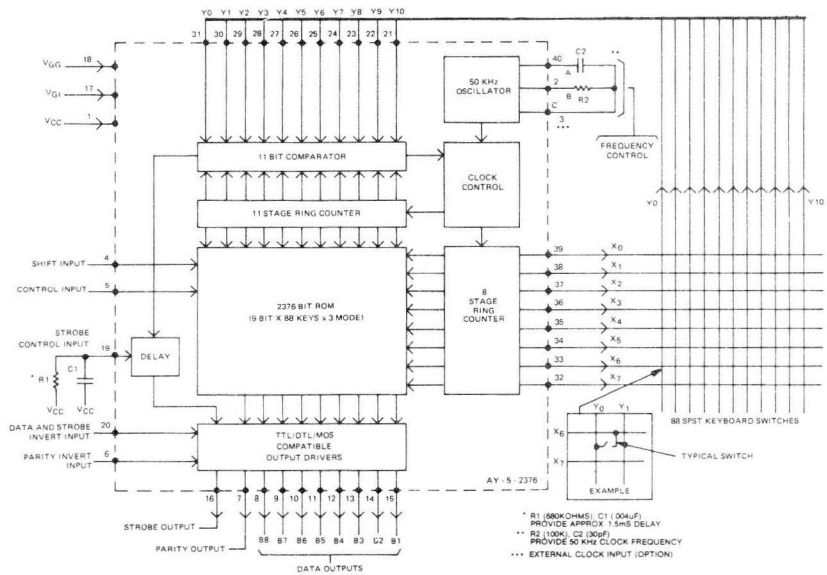
The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The AY-5-2376 contains (see Block Diagram), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

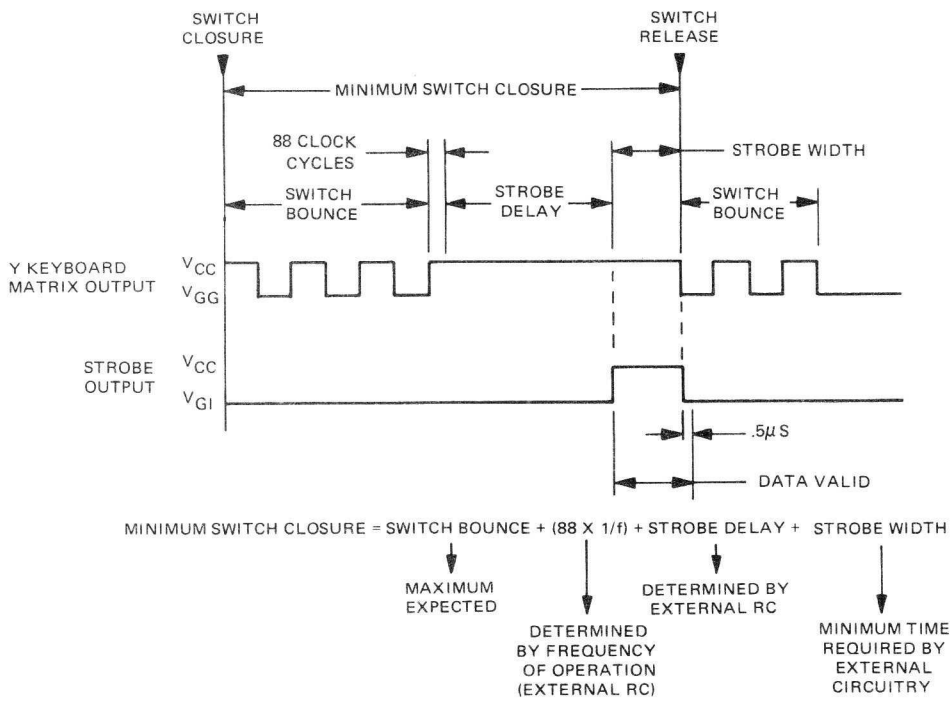
The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

MEMORY

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . −20V to +0.3V
Storage Temperature . . . . . −65° C to +150° C
Operating Temperature Range . . . . . 0° C to +70° C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

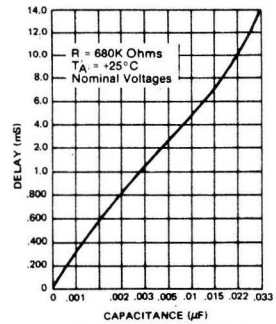
V_{CC} = +5 Volts ± 0.5 Volts, (V_{CC} = Substrate Voltage)
V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. Operating Temperature (T_A) = 0° C to +70° C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	60	μA	V_I=+5V
		8	16	30	μA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	μA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{X1}	—	0	—	μA	$V_{OUT} = V_{CC}$
		80	150	400	μA	$V_{OUT} = V_{CC}$ −1.3V
		140	300	800	μA	$V_{OUT} = V_{CC}$ −2.0V
		250	700	1500	μA	$V_{OUT} = V_{CC}$ −5V
		500	1500	3000	μA	$V_{OUT} = V_{CC}$ — 10V
Logic "0" Output Current	I_{XO}	15	30	80	μA	$V_{OUT} = V_{CC}$
		13	27	65	μA	$V_{OUT} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{OUT} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{OUT} = V_{CC}$ −5V
		—	1	20	μA	$V_{OUT} = V_{CC}$ −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1
						Note 2
Selected Y Input Current	I_{YS}	30	60	160	μA	$V_{IN} = V_{CC}$
		26	54	130	μA	$V_{IN} = V_{CC}$ −1.3V
		24	50	120	μA	$V_{IN} = V_{CC}$ −2.0V
		10	20	80	μA	$V_{IN} = V_{CC}$ −5V
		—	2	20	μA	$V_{IN} = V_{CC}$ −10V
Unselected Y Input Current	I_{YU}	15	30	80	μA	$V_{IN} = V_{CC}$
		13	27	65	μA	$V_{IN} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{IN} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{IN} = V_{CC}$ −10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680K to V_{SS}
Data Output (B_1-B_9)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}−100μa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

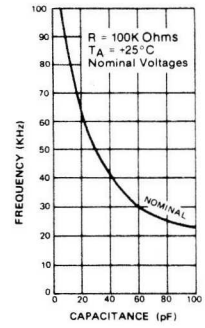
**Typical values at +25° C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

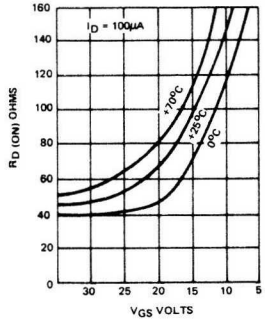
TYPICAL CHARACTERISTIC CURVES



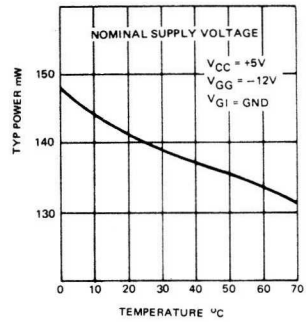
STROBE DELAY VS. C_1



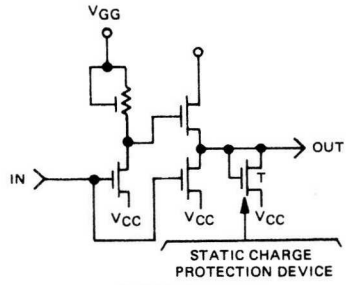
OSCILLATOR FREQUENCY VS. C2



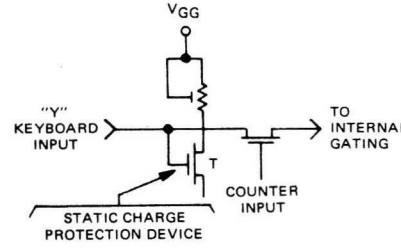
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



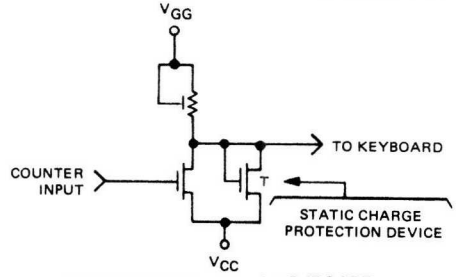
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (C°)



OUTPUT DRIVER



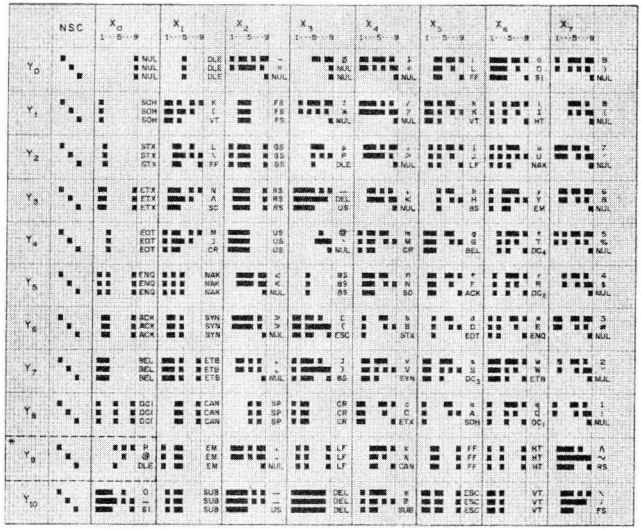
"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

MEMORY

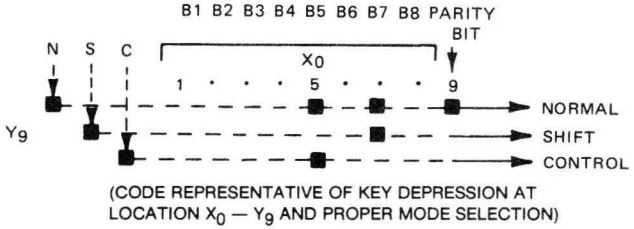
STANDARD CODE ASSIGNMENT CHART



Illustrated using a Logic "O" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

*EXAMPLE



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X_0 — Y_9 AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1" (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

$\overline{S}$ $\overline{C}$ = N
S $\overline{C}$ = S
$\overline{S}$ C = C
S C = C

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly.
- N key rollover or lock out operation.
- Quad mode operation.
- Lock out/rollover selection under external control (option).
- Self-contained or slave oscillator circuit.
- 10 output data bits available.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- Output data buffer register included.
- Output enable provided (option).
- External data complement control provided (option).
- Pulse or level data ready output signal provided (option).
- "Any Key Down" output provided (option).
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Programmable coding with a single mask change.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

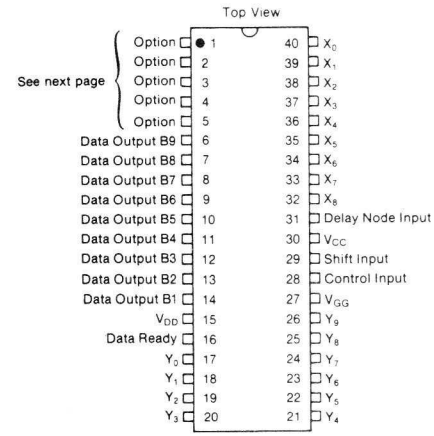
DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

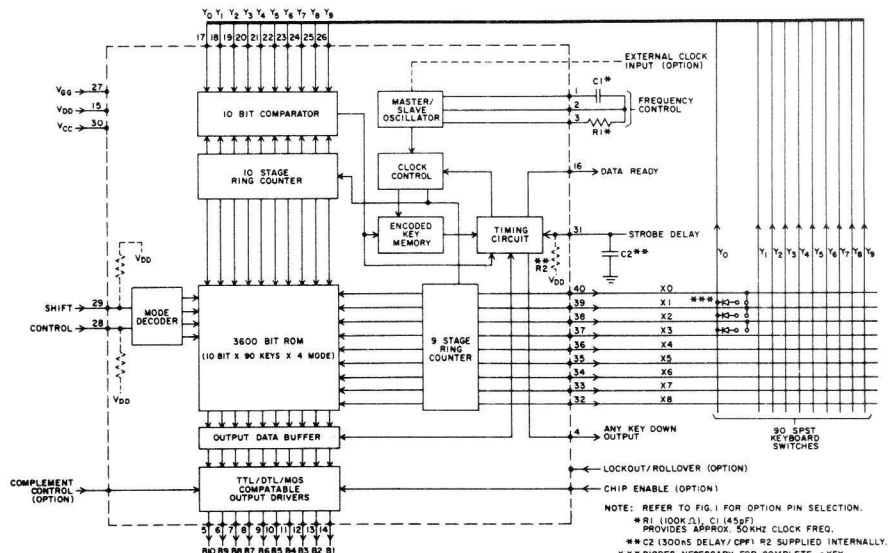
The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



MEMORY

CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock
—requires one package pin to input an external clock source.
Internal Oscillator
—requires three package pins interconnected with an external RC network to develop the clock required.
Lockout/Rollover (LO/RO)
—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.
Complement Control (CC)
—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.
Chip Enable (CE)
—requires one package in to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.
Any Key Output (AKO)
—requires one package pin to indicate a key depression.
Output Data Bit 10 (B10)
—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:
External Clock + 4 of the following functions
OR
Internal Oscillator + 2 of the following functions
LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
V_{GG} = −12 Volts ±1.0 Volts, V_{DD} = GND
(V_{CC} = Substrate Voltage)
Operating Temperature (T_A)= 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Data & Clock Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}–1.5	—	V_{CC}+0.3	V	
Shift & Control Input Current	I_{NSC}	75	95	120	μA	V_I = +5V
X Output (X_0-X_8)						
Logic "1" Output Current	I_{XI}	40	170	400	μA	V_{OUT} = V_{CC} (See Note 2)
		600	1300	2500	μA	V_{OUT} = V_{CC}–1.3V
		900	1600	3500	μA	V_{OUT} = V_{CC}–2.0V
		1500	3800	6000	μA	V_{OUT} = V_{CC}–5V
		3000	6000	10000	μA	V_{OUT} = V_{CC}–10V
Logic "0" Output Current	1_{XO}	8	15	50	μA	V_{OUT} = V_{CC}
		6	11	35	μA	V_{OUT} = V_{CC}–1.3V
		5	10	30	μA	V_{OUT} = V_{CC}–2.0V
		2	5	15	μA	V_{OUT} = V_{CC}–5V
		—	0.5	5	μA	V_{OUT} = V_{CC}–10V
Y Input (Y_0-Y_9)						
Trip Level	V_Y	V_{CC}–5	V_{CC}–3	V_{CC}–2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV_Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I_{YS}	18	36	100	μA	V_{IN} = V_{CC}
		14	28	90	μA	V_{IN} = V_{CC}–1.3V
		13	25	80	υA	V_{IN} = V_{CC}–2.0V
		6	12	60	μA	V_{IN} = V_{CC}–5V
		—	1	30	μA	V_{IN} = V_{CC}–10V
Unselected Y Input Current	I_{YU}	9	18	50	μA	V_{IN} = V_{CC}
		7	14	45	μA	V_{IN} = V_{CC}–1.3V
		6	13	40	μA	V_{IN} = V_{CC}–2.0V
		3	6	30	μA	V_{IN} = V_{CC}–5V
		—	0.5	15	μA	V_{IN} = V_{CC}–10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	φP	1500	3500	5000	μA	V = V_{CC}
		200	600	1500	μA	V = V_{CC}–5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V_{SD}	V_{CC}–4	V_{CC}–3	V_{CC}–2	V	
Hysteresis	V_{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		–3	–5	–9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6m A
Logic "1"	—	V_{CC}–1	—	—	V	I_{OH} = 1.0m A
	—	V_{CC}–2	—	—	V	I_{OH} = 2.2m A
Power						
I_{CC}	—	—	8	12	mA	V_{CC} = +5V
I_{GG}	—	—	8	12	mA	V_{GG} = –12V

**Typical values are at +25° C and nominal voltages.

NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

MEMORY

OPERATION

The AY-5-3600 contains (see Block Diagram), a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

TIMING DIAGRAM

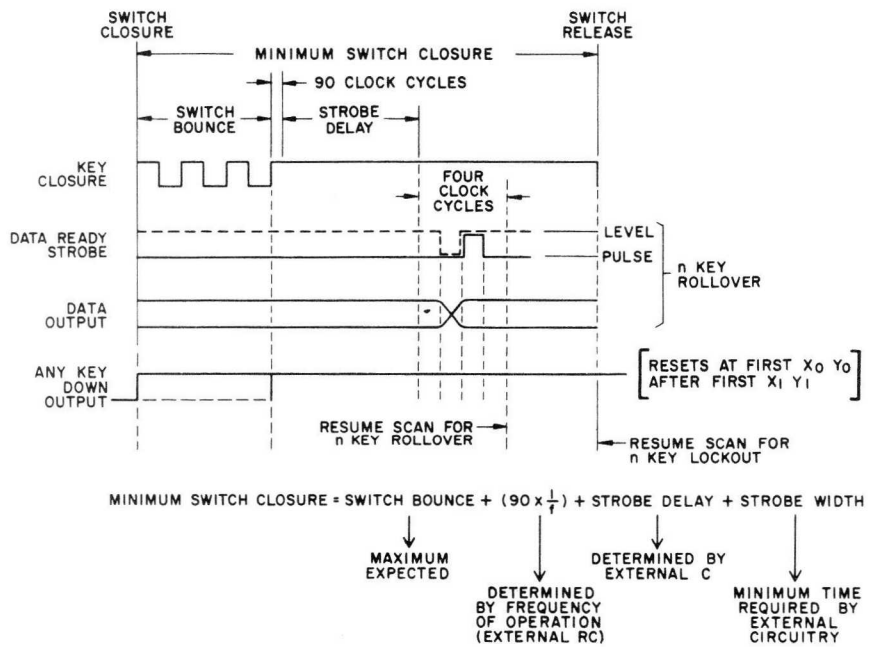


Fig.1

SYMBOL	MODE			
	N	S	C	SC
@		X1 Y0, X0 Y8		
A		X0 Y2		X1 Y2
B		X5 Y3		X2 Y2
C		X2 Y3		X3 Y2
D		X2 Y2		X4 Y2
E		X2 Y1		X5 Y2
F		X3 Y2		X6 Y2
G		X4 Y2		X7 Y2
H	X0 Y5	X0 Y5, X5 Y2	X0 Y5	X0 Y5
I		X7 Y1		X0 Y4
J		X6 Y2		X6 Y6
K		X7 Y2		X3 Y6
L	X2 Y6	X2 Y6, X8 Y2	X2 Y6	X2 Y6
M		X7 Y3		X3 Y5
N		X6 Y3		X4 Y5
O		X8 Y1		
P		X6 Y6		X0 Y2, X0 Y3
Q		X0 Y1		X1 Y3
R		X3 Y1		X2 Y3
S		X1 Y2		X4 Y3
T		X4 Y1		X5 Y3
U		X0 Y1		X6 Y3
V		X4 Y3		X7 Y3
W		X1 Y1		X6 Y5
X		X1 Y3		X8 Y2
Y		X5 Y1		X5 Y6
Z		X0 Y3		X5 Y5
a	X0 Y2		X0 Y2	
b	X5 Y3		X5 Y3	
c	X2 Y3		X2 Y3	
d	X2 Y2		X2 Y2	
e	X2 Y1		X2 Y1	
f	X3 Y2		X3 Y2	
g	X4 Y2		X4 Y2	
h	X5 Y2		X5 Y2	
i	X7 Y1		X7 Y1	
j	X6 Y2		X6 Y2	
k	X7 Y2, X2 Y9		X7 Y2	
l	X8 Y2		X8 Y2	
m	X7 Y3, X1 Y6		X7 Y3	
n	X6 Y3, X1 Y8		X6 Y3	
o	X8 Y1		X8 Y1	
p	X6 Y6, X0 Y8		X6 Y6	
q	X0 Y1		X0 Y1	
r	X3 Y1		X3 Y1	
s	X1 Y2		XJ Y2	
t	X4 Y1		X4 Y1	
u	X6 Y1		X6 Y1	
v	X4 Y3		X4 Y3	
w	X1 Y1		X1 Y1	
x	X1 Y3		X1 Y3	
y	X5 Y1		X5 Y1	
z	X0 Y3		X0 Y3	
[		X8 Y6, X2 Y9		X4 Y6, X8 Y6
\				X1 Y1
]	X8 Y6	X1 Y6	X8 Y6	X8 Y1
^		X1 Y8		X2 Y4
_	X4 Y7, X8 Y7		X4 Y7, X8 Y7	X4 Y7
`	X3 Y6	X3 Y6	X3 Y6	
{	X4 Y5	X4 Y5	X4 Y5	
~				X6 Y4
DEL			X2 Y9	X2 Y9
NULL	X5 Y7	X5 Y7	X5 Y7, X0 Y8	X5 Y7, X0 Y8

SYMBOL	MODE			
	N	S	C	SC
SOH			X0 Y9	X5 Y0, X0 Y9
STX			X1 Y9	X4 Y0, X1 Y9
ETX	X4 Y4	X4 Y4	X4 Y4	X4 Y4, X6 Y0
EOT				X4 Y1
ENQ				X3 Y1
ACK			X2 Y8	X7 Y1, X2 Y8
BEL			X3 Y8	X6 Y1, X3 Y8
BS				X3 Y4
HT	X0 Y4	X0 Y4	X0 Y4, X8 Y9	X8 Y9
LF	X7 Y6	X7 Y6	X7 Y6	
VT	X3 Y7	X3 Y7	X3 Y7	X3 Y7
FF	X7 Y8		X7 Y8	X7 Y8
CR	X3 Y5	X3 Y5	X3 Y5, X1 Y6	X1 Y6
SO	X0 Y7		X0 Y7, X1 Y8	X0 Y7, X1 Y8
SI	X1 Y7	X1 Y7	X1 Y7	X1 Y7
DLE				X0 Y1
DC1				X5 Y1
DC2				X6 Y7
DC3				X2 Y1
DC4				X3 Y0
NAK				X2 Y0
SYN				X5 Y4
ETB				X1 Y0
CAN	X3 Y4		X3 Y4	
EM				X8 Y0
SUB				X0 Y0
ESC				X7 Y0
FS				X1 Y4
GS				X7 Y6
RS	X1 Y4	X1 Y4	X1 Y4	
US	X2 Y7	X2 Y7	X2 Y7	X2 Y7
SP	X3 Y3, X4 Y9	X4 Y9, X3 Y3	X4 Y9, X3 Y3	X4 Y9, X3 Y3
!	X5 Y9	X5 Y9, X0 Y9	X5 Y9	X5 Y9
"	X3 Y9	X3 Y9, X7 Y5, X1 Y9	X3 Y9	X3 Y9, X7 Y5
#	X6 Y9	X6 Y9, X2 Y0	X6 Y9	X6 Y9
$	X2 Y5	X2 Y5, X3 Y0	X2 Y5	X2 Y5
%	X1 Y5	X1 Y5, X4 Y0	X1 Y5	X1 Y5
&	X6 Y8	X6 Y0, X6 Y8, X2 Y8	X6 Y8	X6 Y8
'	X7 Y5	X3 Y8	X7 Y5	X7 Y4
(	X7 Y9	X7 Y4, X3 Y4, X8 Y0	X7 Y9	X7 Y9
)	X4 Y8	X4 Y8, X6 Y7, X8 Y9	X4 Y8	X4 Y8
*	X5 Y8	X5 Y8, X7 Y0, X5 Y4	X5 Y8	X5 Y8
+	X0 Y6	X0 Y6, X5 Y6, X7 Y7	X0 Y6	X0 Y6, X7 Y7
,	X8 Y3	X8 Y3	X8 Y3	X8 Y3
—	X2 Y4	X2 Y4, X8 Y7	X2 Y4	X8 Y7
.	X8 Y4	X8 Y4	X8 Y4	X8 Y4
/	X7 Y4		X7 Y4	
0	X6 Y7, X8 Y8	X8 Y8	X6 Y7, X8 Y8	X8 Y8
1	X0 Y0, X0 Y9		X0 Y0	
2	X1 Y0, X1 Y9		X1 Y0	
3	X2 Y6		X2 Y0	
4	X3 Y0		X3 Y0	
5	X4 Y0		X4 Y0	
6	X5 Y0, X2 Y8		X5 Y0	
7	X6 Y0, X3 Y8		X0 Y0	
8	X7 Y0		X7 Y0	
9	X8 Y0, X8 Y9		X8 Y0	
:	X5 Y4	X8 Y5	X5 Y4	X8 Y5
;	X8 Y5, X5 Y6		X8 Y5, X5 Y6	
<	X6 Y5	X7 Y8, X6 Y5, X0 Y0	X6 Y5	
=	X6 Y4, X7 Y7	X7 Y7, X6 Y4, X4 Y7	X6 Y4	
>	X5 Y5	X5 Y5, X5 Y0, X0 Y7	X5 Y5	
?	X4 Y6	X4 Y6, X7 Y4	X4 Y6	

Note 1. Bits 1 to 6 and bit 8 of the AY-5-3600 correspond to bits 1 to 7 of ASC II.

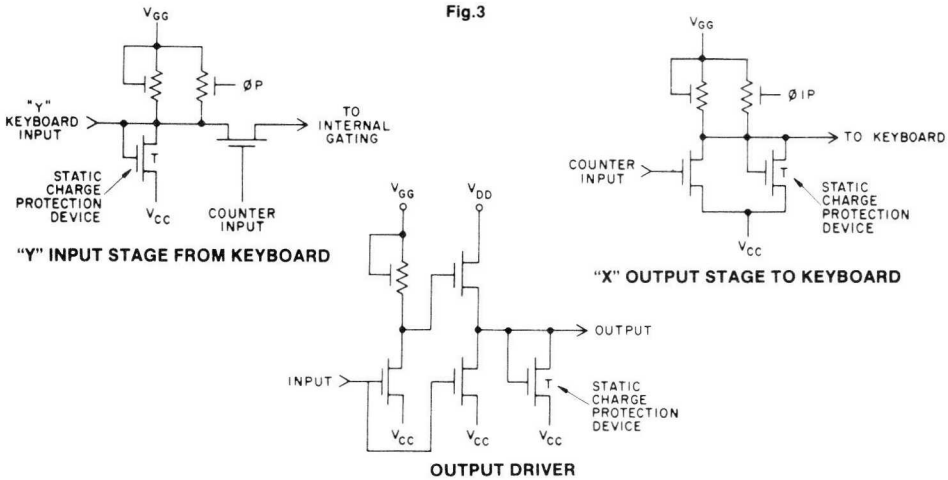
Note 2. Codes 0000011 and 0011111 are not present in the standard AY-5-3600 pattern.

Fig.2 STANDARD AY-5-3600 CODE ASSIGNMENTS ASCII CODE

OPTIONS PROVIDED WITH STANDARD ENCODER

- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3.
- Any Key Output on Pin No. 4.
  Any Key Output True (Logic 1) During Key Depression.
- Output Data Bit B10 on Pin No. 5.
- N-Key Rollover Only.
- True Outputs Only.
- Pulse Data Ready Signal.
- Internal Resistor to V_{DD} on Shift/Control Pin.
- Plastic Package.

Fig.3



NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}.

TYPICAL CHARACTERISTIC CURVES

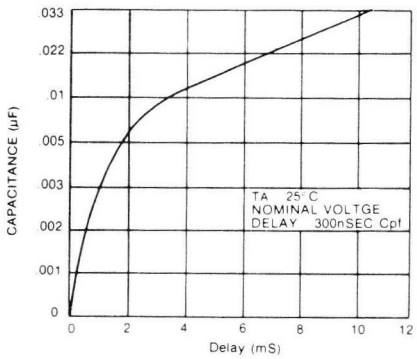


Fig.4 STROBE DELAY vs. C_1

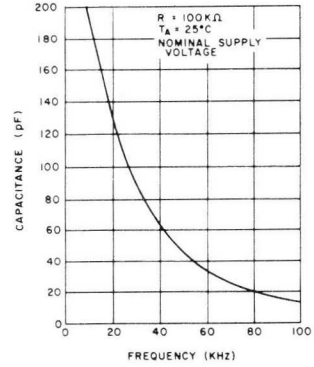


Fig.5 OSCILLATOR FREQUENCY vs. C_2

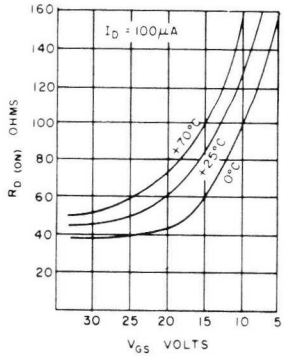


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

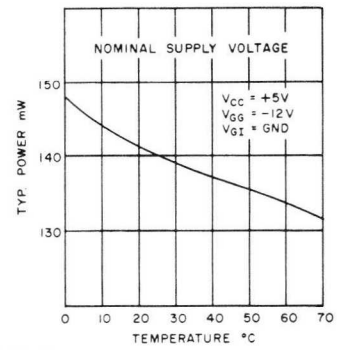
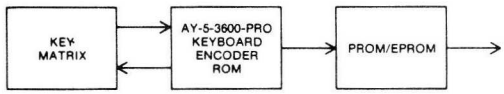


Fig.7 TYPICAL POWER CONSUMPTION (mW)

Keyboard Encoder and PROM/EPROM Application

The AY-5-3600-PRO is pre-programmed during manufacture to provide specific yet simple binary coded outputs thus allowing the purchase of off-the-shelf devices (distributors, etc.). To enhance the device flexibility, the binary outputs have been organized to provide direct interface with a PROM/EPROM.



The PROM (Programmable Read Only Memory) permits the programming of the required output code in the factory or the field within minutes, thus making it extremely suitable for small quantity, fast turnaround keyboard requirements. The EPROM (Erasable Programmable Read Only Memory) is ideally suited for prototyping, where patterns are quite variable, allowing the EPROM to be erased and reprogrammed repeatedly. Similar advantages are realized in the field where pattern changes are necessary in order to respond to redefined requirements or to subtle system peculiarities not previously encountered.

Technical Description

The AY-5-3600-PRO is a binary coded MOS-LSI device programmed to furnish 360 unique 9-bit codes (90 keys × 4 modes × 9 bits). Option selections include such popular functions as Internal Oscillator, Lockout/Rollover and an Any Key Down output. For further, more explicit device characteristics refer to the preceding pages. The internal oscillator is a self contained (on-chip) circuit option which eliminates the need for any external clock source. For applications necessitating an external clock source the internal oscillator input pins may be utilized to function in the slave mode of operation. Lockout or Rollover is selectable via an input pin, thus allowing the versatility required on various keyboard applications. The Any Key Down output performs the function of a gating signal by acknowledging both a key depression and release, making it a convenient signal for use in a repeat application.

For ease of translation, each key is assigned an X-Y coordinate and, in turn, each X-Y coordinate has been identified with a specific yet simple binary coded output. Two formats are described: the first for application with a 64 key 4 mode keyboard and the second for a 90 key 4 mode keyboard.

The 64 key 4 mode application as illustrated in Fig. 8 utilized keyboard encoder addresses X0 Y0 thru X6 Y3. A unique combination of one input (Y) and one output (X) is assigned to each key, for a total coverage of 64 keys. Binary coded outputs B2-B9 have been arranged to provide the necessary 8-bit address inputs to the PROM/EPROM, with B2 and B3 representing the variable mode identification and B4-B9 each specific key closure.

When a key is depressed a path is completed between one X line and one Y line thus addressing that specific X-Y ROM coordinate in the AY-5-3600-PRO. The 8-bit binary code for that X-Y location (ref. Truth Table page 14-15) is transferred into a one character 8-bit output latch (B2-B9) thus providing the appropriate 8-bit address to the 256×8 PROM/EPROM.

Expansion to a 90 key 4 mode operation (see Fig. 9) is identical to the 64 key 4 mode except: the 90 key 4 mode version utilizes the full complement of addresses X0 Y0 thru X8 Y9 (90 keys). The 8-bit binary code (B2-B9) previously produced to address the 256×8 PROM/EPROM is now expanded to a 9-bit binary code (B1-B9) for addressing to a 512×8 PROM/EPROM. With expansion to a 90 key 4 mode application outputs B1-B3 now serve as the variable mode identification.

The interface to a PROM/EPROM enables the custom programming of the required output data in the PROM/EPROM to directly coincide to the specific address inputs from the AY-5-3600-PRO. Any PROM whether it be bipolar, ultraviolet erasable or electrically alterable, may be employed to provide a wide variety of "off-the-shelf" keyboards. Once the keyboard assembly has gone beyond the prototyping stage, and assuming the quantity/cost permit, the PROM/EPROM data can be converted to the standard AY-5-3600 data format (ref. AY-5-3600 Custom Coding Information sheet) and produced in production quantities. This eliminates the PROM/EPROM expense while assuring the absence of undefined coding changes.

Summary of Important Features

- Ability to deliver complete keyboard assemblies within days without sacrificing the features offered in the AY-5-3600 Keyboard Encoder.
- Ability to buy off-the-shelf devices (distributor, etc.)
- Ability to verify the specific pattern format using a PROM/EPROM prior to a 'custom' encoder commitment.

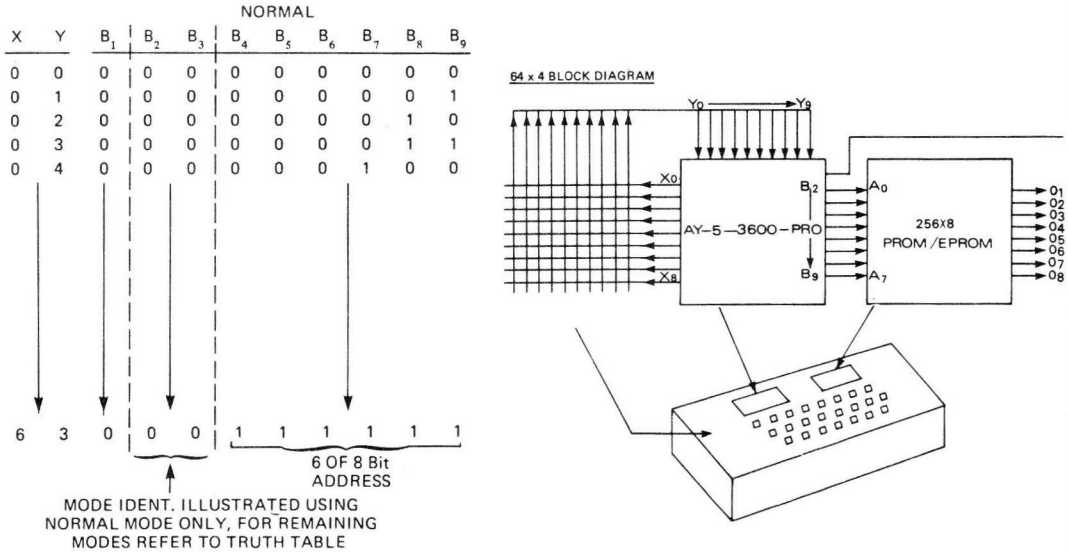


Fig.8 64 KEY 4 MODE KEYBOARD APPLICATION

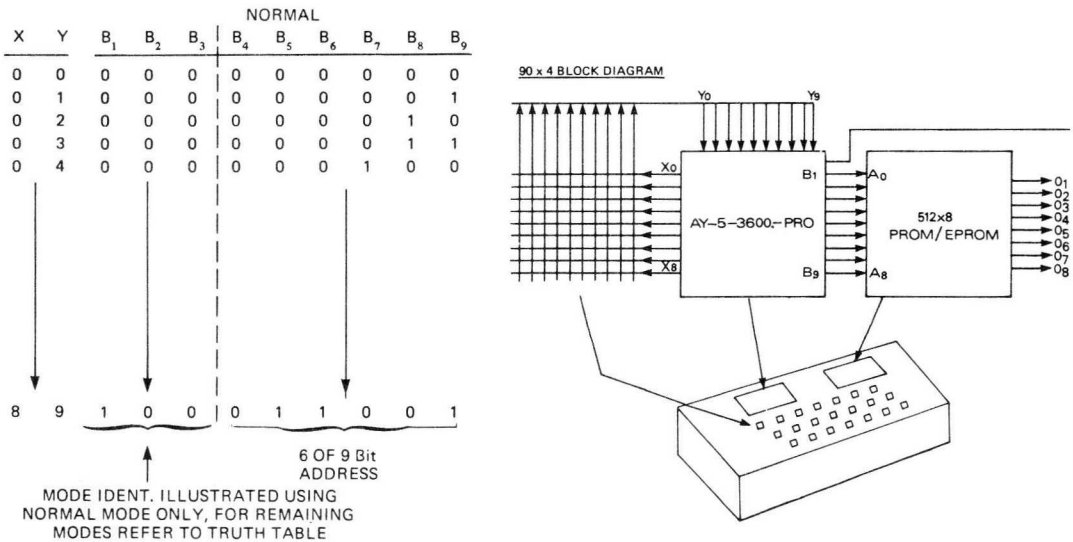


Fig.9 90 KEY 4 MODE KEYBOARD APPLICATION

OPTIONS

- Device Marking: AY-5-3600-PRO
- Internal Oscillator on Pin Nos. 1, 2, 3
- Lockout/Rollover on Pin No. 4
  Internal Resistor to V_{DD} on Lockout/Rollover Pin
- True Outputs Only
- Any Key Output on Pin No. 5.
  Any Key Output True (Logic 1) During Key Depression
- Pulse Data Ready Signal
- Plastic Package
- Internal Resistor to V_{DD} on Shift/Control Pin

XY	NORMAL	SHIFT	CONTROL	SHFT/CTR	XY	NORMAL	SHIFT	CONTROL	SHFT/CTR
0	000000000	001000000	010000000	011000000	45	000101101	001101101	010101101	011101101
1	000000001	001000001	010000001	011000001	46	000101110	001101110	010101110	011101110
2	000000010	001000010	010000010	011000010	47	000101111	001101111	010101111	011101111
3	000000011	001000011	010000011	011000011	48	000110000	001110000	010110000	011110000
4	000000100	001000100	010000100	011000100	49	000110001	001110001	010110001	011110001
5	000000101	001000101	010000101	011000101	50	000110010	001110010	010110010	011110010
6	000000110	001000110	010000110	011000110	51	000110011	001110011	010110011	011110011
7	000000111	001000111	010000111	011000111	52	000110100	001110100	010110100	011110100
8	000001000	001001000	010001000	011001000	53	000110101	001110101	010110101	011110101
9	000001001	001001001	010001001	011001001	54	000110110	001110110	010110110	011110110
10	000001010	001001010	010001010	011001010	55	000110111	001110111	010110111	011110111
11	000001011	001001011	010001011	011001011	56	000111000	001111000	010111000	011111000
12	000001100	001001100	010001100	011001100	57	000111001	001111001	010111001	011111001
13	000001101	001001101	010001101	011001101	58	000111010	001111010	010111010	011111010
14	000001110	001001110	010001110	011001110	59	000111011	001111011	010111011	011111011
15	000001111	001001111	010001111	011001111	60	000111100	001111100	010111100	011111100
16	000010000	001010000	010010000	011010000	61	000111101	001111101	010111101	011111101
17	000010001	001010001	010010001	011010001	62	000111110	001111110	010111110	011111110
18	000010010	001010010	010010010	011010010	63	000111111	001111111	010111111	011111111
19	000010011	001010011	010010011	011010011	64	100000000	101000000	110000000	111000000
20	000010100	001010100	010010100	011010100	65	100000001	101000001	110000001	111000001
21	000010101	001010101	010010101	011010101	66	100000010	101000010	110000010	111000010
22	000010110	001010110	010010110	011010110	67	100000011	101000011	110000011	111000011
23	000010111	001010111	010010111	011010111	68	100000100	101000100	110000100	111000100
24	000011000	001011000	010011000	011011000	69	100000101	101000101	110000101	111000101
25	000011001	001011001	010011001	011011001	70	100000110	101000110	110000110	111000110
26	000011010	001011010	010011010	011011010	71	100000111	101000111	110000111	111000111
27	000011011	001011011	010011011	011011011	72	100001000	101001000	110001000	111001000
28	000011100	001011100	010011100	011011100	73	100001001	101001001	110001001	111001001
29	000011101	001011101	010011101	011011101	74	100001010	101001010	110001010	111001010
30	000011110	001011110	010011110	011011110	75	100001011	101001011	110001011	111001011
31	000011111	001011111	010011111	011011111	76	100001100	101001100	110001100	111001100
32	000100000	001100000	010100000	011100000	77	100001101	101001101	110001101	111001101
33	000100001	001100001	010100001	011100001	78	100001110	101001110	110001110	111001110
34	000100010	001100010	010100010	011100010	79	100001111	101001111	110001111	111001111
35	000100011	001100011	010100011	011100011	80	100010000	101010000	110010000	111010000
36	000100100	001100100	010100100	011100100	81	100010001	101010001	110010001	111010001
37	000100101	001100101	010100101	011100101	82	100010010	101010010	110010010	111010010
38	000100110	001100110	010100110	011100110	83	100010011	101010011	110010011	111010011
39	000100111	001100111	010100111	011100111	84	100010100	101010100	110010100	111010100
40	000101000	001101000	010101000	011101000	85	100010101	101010101	110010101	111010101
41	000101001	001101001	010101001	011101001	86	100010110	101010110	110010110	111010110
42	000101010	001101010	010101010	011101010	87	100010111	101010111	110010111	111010111
43	000101011	001101011	010101011	011101011	88	100011000	101011000	110011000	111011000
44	000101100	001101100	010101100	011101100	89	100011001	101011001	110011001	111011001

Capacitive Keyboard Encoder

FEATURES

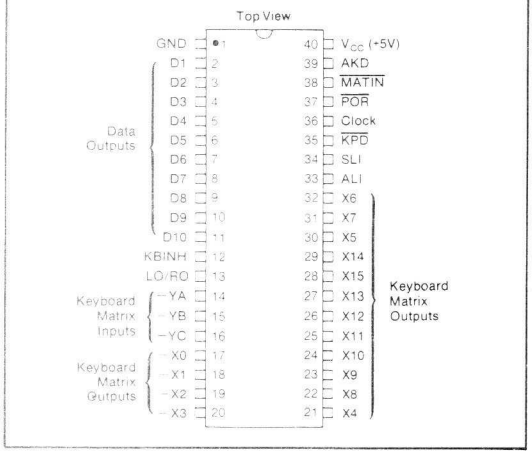
- 128 key keyboard encoder; 112 fully decoded keys, 16 discrete function keys.
- 112 keys with 4 modes, 10 bit output
- Key validation logic protects against bounce.
- N-key roll over or 2-key roll over.
- Internal ROM allows any keys to control SHIFT CTRL, SHIFT LOCK and ALPHA LOCK.
- ALPHA LOCK and SHIFT LOCK indicator lines
- Any key down (AKD) strobe.
- Single +5 Volt power supply.
- Programmable coding of standard and special function keys.
- Zener diode protection on all I/O pins.
- Low power consumption, less than 2 milliwatts per key
- Usable with capacitive, magnetic, inductive, Hall effect or mechanical keyboard switches.
- Inputs and outputs TTL and CMOS compatible.
- Internal Oscillator

DESCRIPTION

The G.I. AY-3-4592 is a unique dual pulse scanning encoder and keyboard controller for 112 keys in four modes and 16 programmable discrete function keys. ROM programming permits any keys to control the shift control and lock functions. The AY-3-4592 can be used with capacitive, inductive (magnetic) or switch closure type switches since it works on pulse detection.

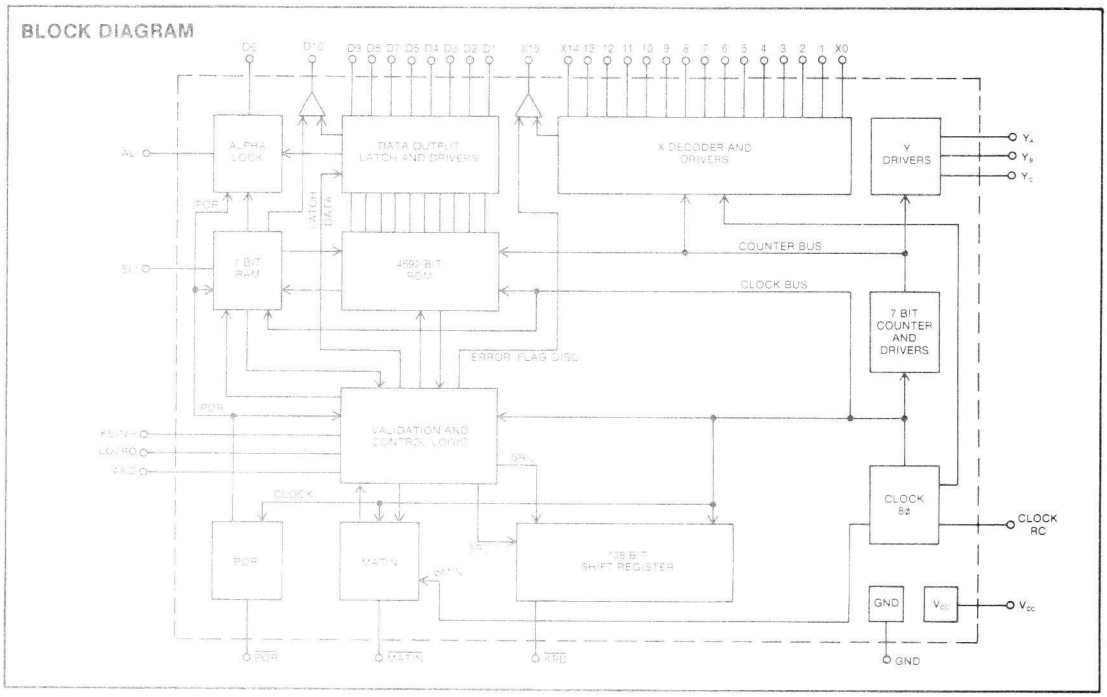
PIN CONFIGURATION

40 LEAD DUAL IN LINE



The AY-3-4592 is fabricated with N-channel MOS technology on a single chip containing a 4592 bit ROM, a 128 bit shift register and an internal oscillator.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	Ground	GND	Ground Pin
2-10	Data Out	D1-D9	Data Outputs, D1 through D9
11	Data Out	D10	Data Output D10. See "AY-3-4592 options" for complete description
12	Key Inhibit	KBINH	Logic "1" on KBINH will inhibit the processing of Key closures and prevent new output codes. See "AY-3-4592 options" for other custom options
13	Lockout/rollover	LO/RO	High for 2 Key Rollover operation, low for N Key Rollover operation. This input is a high impedance Schmitt trigger with thresholds of approximately ¼ (low) and ¾ (high) of V_{CC}. This allows easy interfacing with very slow RC circuits for such functions as "repeat delay". LO/RO is internally "anded" with AKD/STB; if either is low, N Key rollover is automatically selected.
14-16	Y-Address	YA, YB, YC	Y Address lines select one of eight Y inputs through external multiplexer. Scan sequence is Y7 to Y0
17-27, 30-32	X Outputs	X0-X13, X5-X7	X output drivers for Matrix scanning. Scan sequence is X15 to X0. Each driver generates 8 pairs of pulses each scanning cycle.
28, 29	X15, 14	X15, X14	X15 is programmed as a "discrete output" key in the standard part. Optionally it may be programmed as a error flag or as a Matrix drive line. See "AY-3-4592 options". Unlike X0-X13, neither X14 nor X15 have associated ROM output codes. These lines are used to enable separate discrete keys to be debounced using an addressable latch as illustrated in figure 2.
33	Alpha Lock Indicator	ALI	ALI will indicate if "op code" XX101 is selected. (See operation codes). In the standard device there is no other function. If alpha lock is selected as an option, op code XX101 will result in bit 6 being replaced by bit 9 when a key is depressed.
34	Shift Lock Indicator	SLI	SLI will indicate if "op code" XX011 is selected. (See "operation codes"). In the standard device this op code will also select the shift lock function.
35	Key Pressed	$\overline{KPD}$	$\overline{KPD}$ is used to shift the threshold of the external sense amplifier in order to provide hysteresis to improve noise immunity. In addition $\overline{KPD}$ may be inverted to provide the data input to the 8 bit latches for decoding X14 and X15. When a key closure is detected $\overline{KPD}$ is generated causing the 8 bit latch output to go high. See figure 2.
36	CLOCK	CLK	Resistor/capacitor tie point for the internal oscillator. Nominal frequencies and scan times are shown below:

	C = 150pf		C = 220pf		C = 500pf	
R	Freq	Scan time	Freq	Scan time	Freq	Scan time
5K	1.3 MHz	1.5 msec	1.2 MHz	1.7 msec	.71 MHz	2.8 msec
10K	.8 MHz	2.3 msec	.8 MHz	2.7 msec	.45 MHz	4.3 msec
25K	.4 MHz	4.8 msec	.3 MHz	6.0 msec	.20 MHz	10.0 msec

37	Reset	$\overline{POR}$	Reset clears all internal registers and flip flops. Suggested circuit for power on reset is illustrated in Figure 1.
38	Matrix Input	$\overline{MATIN}$	Input from external multiplexer. Senses signal from X-Y scan of depressed key.
39	Any Key Down Strobe	AKD	AKD is low when no key is depressed. When a key is depresed AKD goes high. If while one key is held, a second key is depressed AKD will go low for 2 clock cycles.
40	Power	V_{CC}	Power supply input; +5 Volts

OPERATION

Keys are connected in a 16 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an external, multiplexer. The encoder provides a 3 bit binary address (YA, YB, YC) used to scan each of eight possible sense lines (Y-lines). The drive lines (X-lines) are each pulsed low by the encoder. If a key is closed, the pulse is coupled from the drive to the sense lines, amplified and sent to the encoder. When used to encode reactive switches, a detection circuit is necessary between the output of the multiplexer and the $\overline{\text{MATIN}}$ input to the encoder. In this manner, each matrix cross-point is interrogated in turn. Each matrix cross-point is given a unique binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes (such as ASCII or other customer defined codes). The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure. Only the cross-points on X0 through X13 can have output codes: X14 and X15 can be used for scanning discrete keys.

An internal oscillator controls the matrix scanning rate. The minimum scanning time is 1.7 msec, at a 1.2 MHz clock. This allows a burst typing speed equivalent to over 250 words/min. When a key is depressed, a matrix address from an X driver and Y input line representing that key is loaded into a 7 bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10 bit word at that address is loaded into the data holding register. This data remains valid until the next key is depressed. The internal error flag is set, if this option was utilized, whenever there is a mismatch between 7 bit addresses.

Two negative pulses must be detected during the $\overline{\text{MATIN}}$ timing window for the depression to be recognized.

Keyboard Selection

The AY-3-4592 keyboard encoder can be used with a wide variety of available keyboards. An external multiplexing circuit and one external sense amplifier can be tailored to the user's specific requirements. As shown in Figure 1, the sense amplifier detects changes in voltage caused by variations in the switch impedance as a key is depressed and released. Given the key switch impedances for depressed and released states, the values of Rx and Rh can be chosen to guarantee switch closure detection and noise margins. Rx is chosen to match the capacitor or reactor time constants. For example, given a variable capacitance keyboard switch with C1 = 100pf, and C2 = 10pf for depressed and released positions respectively, with a 1.5 MHz oscillator and Rx = 10 Kohm, a depressed key would make a 4.7 volt pulse while a raised key would produce a 2.6 volt pulse. The potentiometer would then be set for best noise immunity with minimum pulse width, 90 ns for all keys. The hysteresis resistor, Rh, is chosen at roughly ten times the value of Rx to provide increased noise immunity for detected key depressions.

Operation Codes

Depending on the internal programming of the AY-3-4592, keys may have one of three different functions. Keys on matrix lines X0 through X13 have in addition to the output code bits a function flag bit (FFB). If the FFB is programmed as a zero, the key produces a data output when depressed.

When FFB is a one, the key is a "function" key for which bits 1-5 determine the function. These bits are referred to as the "op code" and are used to provide special functions such as shift, shift lock, alpha lock etc. Bits 6-10 are not used.

Op codes may be programmed to provide data outputs as well as change the mode of operation. Data when outputted is not latched as are normal coded outputs.

Bits 1-3 indicate what operation the key will perform; per table 1.

Bit 4 programmed as one indicates a "down-coded" key, for which the 10 data bits programmed in the shift mode level of ROM are outputted when the key is depressed.

Bit 5 programmed as one indicates an "up-coded" key for which the 10 data bits programmed in the control mode level of ROM are outputted when the key is released.

Neither bit 4 or 5 will have any effect on the operational control of bits 1-3.

Table 1

Op-Code					Function
5	4	3	2	1	
X	X	0	0	0	Function key (with up/down codes)*
X	X	0	0	1	Right Shift Key
X	X	0	1	0	Left Shift Key
X	X	0	1	1	Shift Lock Key or Discrete Key (output SLI)
X	X	1	0	0	Control Key
X	X	1	0	1	Alpha Lock Key or Discrete Key (output ALI)
X	0	1	1	0	Error Reset Key or discrete key (output X15)
X	X	1	1	1	Discrete Key (output D10)

*If the op-code is 00000 the key has no internal function but $\overline{\text{KPD}}$ will go low when it is processed.

OPTIONS

Pin or Function	Option
X15	X15 may be programmed as 1) an X-output to provide a second set of 8 discrete lines 2) a "discrete output" which indicates when a function key with op code XX110 is depressed 3) an Error Flag Indicator (EFI). See "Error Flag" In the AY-3-4592 STD X15 is a discrete output
Error Flag	When this option is selected, the AY-3-4592 has the capability of detecting multiple key depressions during the same scan cycle. When selected, the error flag may be programmed to generate KBINH and or appear at the X15 output. The error flag may be reset by three methods. If the "automatic reset" is selected/the flag will be reset when the error causing Key is released. Op-code XX110 may be programmed on a function key to reset the error flag. If pin 12 is programmed for KBINH error flag will be reset by pulsing pin 12 high. The reset will occur on the negative edge of the KBINH signal; the pulse must be at least 16 clock cycles. In the AY-3-4592 STD, error flag causes KBINH and is automatically reset.
Alpha Lock	When programmed for Alpha lock, the function key with op-code XX101 will cause the bit 6 output to be replaced by bit 9. Bit 9 is not altered. Alpha lock is normally used to force printing of upper case characters irrespective of the shift function. Op Code XX101 will also cause an output on ALI (pin 33). When Alpha lock is not programmed, op code XX101 will simply result in an output on ALI (pin 33). Op code XX101 may be programmed for momentary action, or latched push-on, push-off alternating action. ALI may be programmed for normally low or high output. Op code XX101 is momentary action. ALI is normally low. The AY-3-4592 STD is not programmed for Alpha lock, although there will be an output on ALI.
Shift Lock	When programmed for shift lock, the function key with op-code XX011 will cause normal electronic shift action. Op code XX011 will also cause an output on SLI (pin 34). If shift lock is not programmed, op code XX011 will simply cause an output on SLI. SLI may be programmed for normally low or high output. The AY-3-4592 STD is programmed for shift lock operation with SLI normally low.
KBINH	KBINH, Keyboard Inhibit, may be programmed to be caused by Pin 12 high, by the error flag, or both. In addition, function keys with up or down codes may be programmed, as a group, to be inhibited by KBINH. This is the "KCI Out" option. When pin 12 is programmed to cause KBINH, a "high" input on pin 12 will inhibit processing of common keys. If a key is depressed while the KBINH signal is present, output and output strobe will be generated when KBINH is released. The AY-3-4592 STD has KBINH actuated by pin 12 high, and by the error flag. The "KCI In" option is used, that is, the function key operation is independent of KBINH.
D10	D10, pin 11, may be programmed as the output for the memory bit 10 or as a "discrete" output. As a discrete output pin 10 is switched from its normal state (programmable as high or low) by the function key with op-code XX111. The AY-3-4592 STD is programmed for D10 as a discrete key, normally low.
Key Type	Keys may be either normally open or normally closed. The AY-3-4592 STD is designed for normally open keys.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} ..... -0.3 Volts to +7.0 Volts
Maximum voltage with respect to V_{CC} ..... +0.3 Volts
Storage Temperature ..... 65°C to +150°C
Operating Temperature ..... 0 to 70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

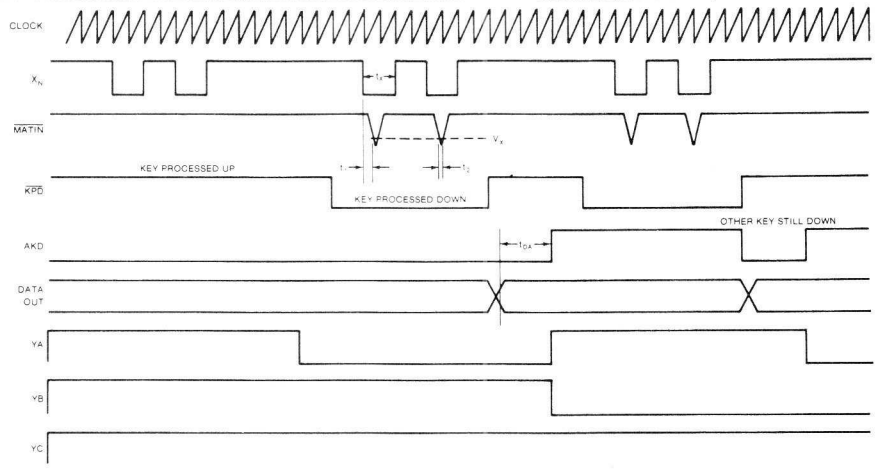
Standard Conditions (unless otherwise noted)

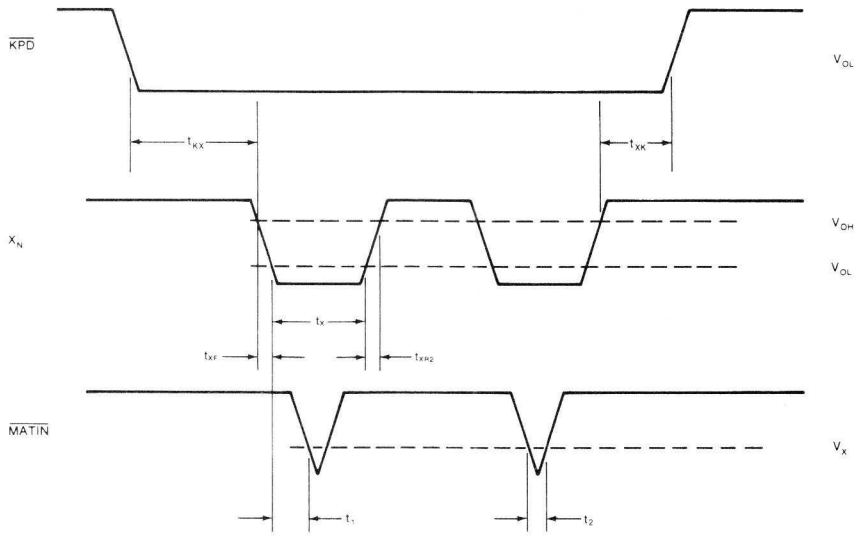
V_{CC} = 5.0V ±5%
T_A = 0° to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Unit	Condition
Data Output "1" Voltage	V_{OH}	3.5	-	-	V	I_{OH} = 50μA, 25pF
Data Output "0" Voltage	V_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
All Inputs "1" Voltage	V_{IH}	2.2	-	-	V	except $\overline{POR}$, 2KRO
All Inputs "0" Voltage	V_{IL}	-	-	0.8	V	except $\overline{POR}$, 2KRO
All Inputs Leakage	I_{IH}	-	-	10	μA	V_{in} = 5V
X Output "1" Voltage	X_{OH}	3.5	-	-	V	I_{OH} = 50μA, 100pF
X Output "0" Voltage	X_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
AKd Output Voltage	V_A	-	-	0.6	V	I_{OL} = 3.2mA
$\overline{MATIN}$ Input Voltage	V_X	-	-	0.4	V	
$\overline{POR}$, 2KRO high threshold	V_{SH}	-	1.3	-	V	Schmitt trigger
$\overline{POR}$, 2KRO low threshold	V_{SL}	-	3.7	-	V	Schmitt trigger
Power Supply Current	I_{CC}	-	35	60	mA	Vcc = 5.3V
Clock Frequency	ϕ	200	-	1200	kHz	
Matrix Delay	t_1	-	-	250	ns	
Input pulse width	t_2	90	-	-	ns	
X Output pulse width	t_x	1.7	-	-	μs	
X Output fall time	t_{XF}	-	-	150	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
X Output rise time	t_{XR1}	-	-	150	ns	V_{OH} = 2.4V, V_{OL} = 0.4V
X Output rise time	t_{XR2}	-	-	500	ns	V_{OH} = 3.5V, V_{OL} = 0.4V
X Output rise time	t_{XR3}	-	-	1500	ns	V_{OH} =4.3V, V_{OL} = 0.4V
$\overline{KPD}$-X Output set time	T_{KX}	500	-	-	ns	
X Output-$\overline{KPD}$ hold time	t_{XK}	100	-	-	ns	
Data out to AKD time	t_{OA}	1.7	-	-	μs	

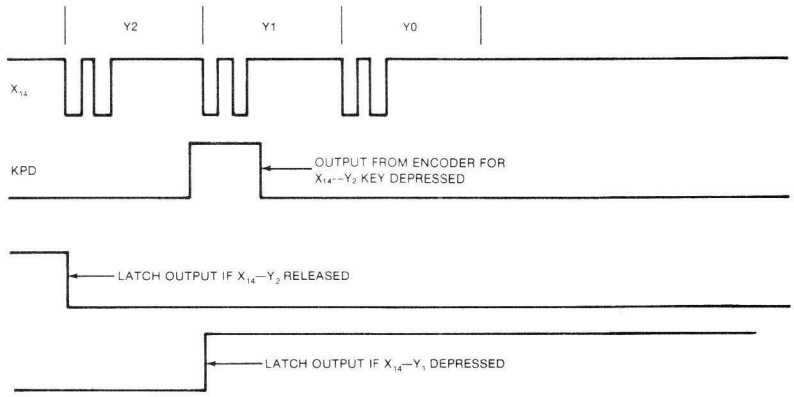
**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





Discrete Function Key



MEMORY

CODE CHART / AY-3-4592-STD

XXY	F	-----NORMAL-----			------ SHIFT ------			---- CONTROL-----			--SHIFT/CONTROL--		
	B	HEX	BINARY		HEX	BINARY		HEX	BINARY		HEX	BINARY	
000	1	001	0000000001	Right Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
001	1	002	0000000010	Left Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
002	1	003	0000000011	Shift Lock	3FF	1111111111		3FF	1111111111		3FF	1111111111	
003	1	004	0000000100	Control	3FF	1111111111		3FF	1111111111		3FF	1111111111	
004	1	005	0000000101	ALI	3FF	1111111111		3FF	1111111111		3FF	1111111111	
005	1	006	0000000110	X15	3FF	1111111111		3FF	1111111111		3FF	1111111111	
006	1	007	0000000111	D10	3FF	1111111111		3FF	1111111111		3FF	1111111111	
007	0	0CE	0011001110	1	0DE	0011011110	!	0CE	0011001110	!	0DE	0011011110	!
010	0	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ES
011	0	0CD	0011001101	2	1BF	0110111111	@	0CD	0011001101	2	1FF	0111111111	NUL
012	0	0CD	0011001101	2	0DD	0011011101	"	0CD	0011001101	2	0DD	0011011101	"
013	0	188	0110001000	W	1A8	0110101000	W	1E8	0111101000	ETB	1E8	0111101000	ETB
014	0	18E	0110001110	9	1AE	0110101110	Q	1EE	0111101110	DC1	1EE	0111101110	DC1
015	0	18C	0110001100	S	1AC	0110101100	S	1EC	0111101100	DC3	1EC	0111101100	DC3
016	0	19E	0110011110	a	18E	0110111110	A	1FE	0111111110	SOH	1FE	0111111110	SOH
017	0	185	0110000101	Z	1A5	0110100101	Z	1E5	0111100101	SUB	1E5	0111100101	SUB
020	0	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL
021	0	0CB	0011001011	4	0DB	0011011011	$	0CB	0011001011	4	0DB	0011011011	$
022	0	0CC	0011001100	3	0DC	0011011100	#	0CC	0011001100	3	0DC	0011011100	#
023	0	18D	0110001101	r	1AD	0110101101	R	1ED	0111101101	DC2	1ED	0111101101	DC2
024	0	19A	0110011010	e	18A	0110111010	E	1FA	0111111010	ENQ	1FA	0111111010	ENQ
025	0	198	0110011011	d	188	0110111011	D	1FB	0111111011	EOT	1FB	0111111011	EOT
026	0	187	0110000111	x	1A7	0110100111	X	1E7	0111100111	ETB	1E7	0111100111	ETB
027	0	19C	0110011100	c	18C	0110111100	c	1FC	0111111100	ETX	1FC	0111111100	ETX
030	0	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH
031	0	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX
032	0	0CA	0011001010	5	0DA	0011011010	%	0CA	0011001010	5	0DA	0011011010	%
033	0	18B	0110001011	t	1AB	0110101011	T	1E8	0111101011	DC4	1E8	0111101011	DC4
034	0	199	0110011001	f	1B9	0110111001	F	1F9	0111111001	ACK	1F9	0111111001	ACK
035	0	198	0110011000	g	1B8	0110111000	G	1F8	0111111000	BEL	1F8	0111111000	BEL
036	0	189	0110001001	v	1A9	0110101001	V	1E9	0111101001	SYN	1E9	0111101001	SYN
037	0	19D	0110011101	b	1BD	0110111101	B	1FD	0111111101	STX	1FD	0111111101	STX
040	0	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX
041	0	0C8	0011001000	7	0D9	0011011001	(	0C8	0011001000	7	0D9	0011011001	(
042	0	0C9	0011001001	6	0D9	0011011001	(	0C9	0011001001	6	0D9	0011011001	(
043	0	186	0110000110	y	1A6	0110100110	Y	1E6	0111100110	EM	1E6	0111100110	EM
044	0	197	0110010111	h	187	0110110111	H	1F7	0111110111	BS	1F7	0111110111	BS
045	0	191	0110010001	n	1B1	0110110001	N	1F1	0111110001	SO	1F1	0111110001	SO
046	0	0C9	0011001001	6	0C3	0011000011	<	0C9	0011001001	6	0C3	0011000011	<
047	0	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP
050	0	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT
051	0	0C7	0011000111	8	0D5	0011010101	*	0C7	0011000111	8	0D5	0011010101	*
052	0	0C8	0011001000	7	0D8	0011011000	'	0C8	0011001000	7	0D8	0011011000	'
053	0	18A	0110001010	u	1AA	0110101010	u	1EA	0111101010	NAK	1EA	0111101010	NAK
054	0	195	0110010101	J	1B5	0110110101	J	1F5	0111110101	ENQ	1F5	0111110101	ENQ
055	0	194	0110010100	k	1B4	0110110100	K	1F4	0111110100	VT	1F4	0111110100	VT
056	0	192	0110010010	m	1B2	0110110010	M	1F2	0111110010	CR	1F2	0111110010	CR
057	0	0D3	0011010011	.	0C3	0011000011	<	0D3	0011010011		0C3	0011000011	<
060	0	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ
061	0	0C6	0011000110	9	0D7	0011010111	(	0C6	0011000110	9	0D7	0011010111	(
062	0	0C7	0011000111	8	0D7	0011010111	(	0C7	0011000111	8	0D7	0011010111	(
063	0	196	0110010110	i	1B6	0110110110	I	1F6	0111110110	HT	1F6	0111110110	HT
064	0	190	0110010000	o	1B0	0110110000	O	1F0	0111110000	SI	1F0	0111110000	SI
065	0	194	0110010100	K	1A4	0110100100	[	1F4	0111110100	VT	1E4	0111100100	ESC
066	0	193	0110010011	l	1B3	0110110011	L	1F3	0111110011	FF	1F3	0111110011	FF
067	0	192	0110010010	m	1A2	0110100010	]	1F2	0111110010	CR	1E2	0111100010	GS
070	0	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK
071	0	0CF	0011001111	ø	0D6	0011010110	)	0CF	0011001111	ø	0D6	0011010110	)
072	0	0C6	0011000110	9	0D6	0011010110	)	0C6	0011000110	9	0D6	0011010110	)
073	0	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL

CODE CHART / AY-3-4592-STD

XXY	F B	NORMAL HEX	NORMAL BINARY		SHIFT HEX	SHIFT BINARY		CONTROL HEX	CONTROL BINARY		SHIFT/CONTROL HEX	SHIFT/CONTROL BINARY	
074	0	18F	0110001111	P	1AF	0110101111	P	1EF	0111101111	DLE	1EF	0111101111	DLE
075	0	0C4	0011000100	;	0C5	0011000101	:	0C4	0011000100	;	0C5	0011000101	:
076	0	193	0110010011	L	1A3	0110100011	\	1F3	0111110011	FF	1E3	0111100011	FS
077	0	0D1	0011010001	.	0C1	0011000001	>	0D1	0011010001	.	0C1	0011000001	>
080	0	0D2	0011010010	–	1A0	0110100000	–	0D2	0011010010	–	1A0	0110100000	–
081	0	191	0110010001	n	1A1	0110100001	^	1F1	0111110001	SI	1E1	0111100001	RS
082	0	18F	0110001111	P	1BF	0110111111	@	1EF	0111101111	DLE	1FF	0111111111	NUL
083	0	1A4	0110100100	[	1A2	0110100010	]	1E4	0111100100	ESC	1E2	0111100010	GS
084	0	0D8	0011011000	'	0DD	0011011101	"	0D8	0011011000	'	0DD	0011011101	"
085	0	0C4	0011000100	;	0D4	0011010100	+	0C4	0011000100	;	0D4	0011010100	+
086	0	0D0	0011010000	/	0C0	0011000000	?	0D0	0011010000	/	0C0	0011000000	?
087	0	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS
090	0	0C2	0011000010	=	0D4	0011010100	+	0C2	0011000010	=	0D4	0011010100	+
091	0	0C5	0011000101	:	0D5	0011010101	*	0C5	0011000101	:	0D5	0011010101	*
092	0	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT
093	0	1A3	0110100011	\	083	0010000011	!	1E3	0111100011	FS	1E3	0111100011	FS
094	0	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF
095	0	1A4	0110100100	[	084	0010000100	$	1E4	0111100100	ESC	1E4	0111100100	ESC
096	0	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR
097	0	1A2	0110100010	]	082	0010000010	}	1E2	0111100010	GS	1E2	0111100010	GS
100	0	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL
101	0	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT
102	0	0D2	0011010010	_	1A0	0110100000	—	1E0	0111100000	US	1E0	0111100000	US
103	0	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS
104	0	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF
105	0	1BF	0110111111	@	1A3	0110100011	\	1FF	0111111111	NUL	1FF	0111111111	NUL
106	0	1A1	0110100001	^	0B1	0010000001	~	1E1	0111100001	RS	1E1	0111100001	RS
107	0	1A0	0110100000	—	0C2	0011000010	=	1A0	0110100000	—	0C2	0011000010	=
110	0	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR
111	0	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT
112	0	0D2	0011010010	-	0C2	0011000010	=	0D2	0011010010	–	0C2	0011000010	=
113	0	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO
114	0	190	0110010000	o	1A0	0110100000	–	1F0	0111110000	SI	1E0	0111100000	US
115	0	1A4	0110100100	[	1A2	0110100010	]	1A4	0110100100	[	1A2	0110100010	]
116	0	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS
117	0	160	0101100000	US	160	0101100000	US	160	0101100000	US	160	0101100000	US
120	0	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI
121	0	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7
122	0	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT
123	0	16F	0101101111	DLE	16F	0101101111	DLE	16F	0101101111	DLE	16F	0101101111	DLE
124	0	0CB	0011001011	4	0C9	0011001011	4	0CB	0011001011	4	0CB	0011001011	4
125	0	0D3	0011010011	,	0D3	0011010011	,	0D8	0011010011	,	0D3	0011010011	,
126	0	0CE	0011001110	!	0CE	0011001110	1	0CE	0011001110	!	0CE	0011001110	!
127	0	0CF	0011001111	Ø	0CF	0011001111	Ø	0CF	0011001111	Ø	0CF	0011001111	0
130	0	16E	0101101110	DC1	16E	0101101110	DC1	16E	0101101110	DC1	16E	0101101110	DC1
131	0	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9
132	0	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8
133	0	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5
134	0	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6
135	0	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2
136	0	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3
137	0	0D1	0011010001		0D1	0011010001		0D1	0011010001	.	0D1	0011010001	

OPTIONS ARE: Error Flag — Programmed
X15 — Discrete output, normally low
KBINH — Set by high on pin 12 or error flag. Function keys not inhibited by KBINH
Error Flag — Reset by releasing error-causing key
Shift Lock — Operational. SLI normally low
Alpha Lock — Inhibited. ALI normally low, set by OP code XX101
D10 — Discrete output, normally low
Key Type — Normally open

NOTE: Bit 9 — Programmed to allow alpha lock implementation using external logic
Bit 8 — Programmed low for "mono mode" keys, for which the output is the same in all modes.
Bits 1-7 — "Inverted" ASCII data bits

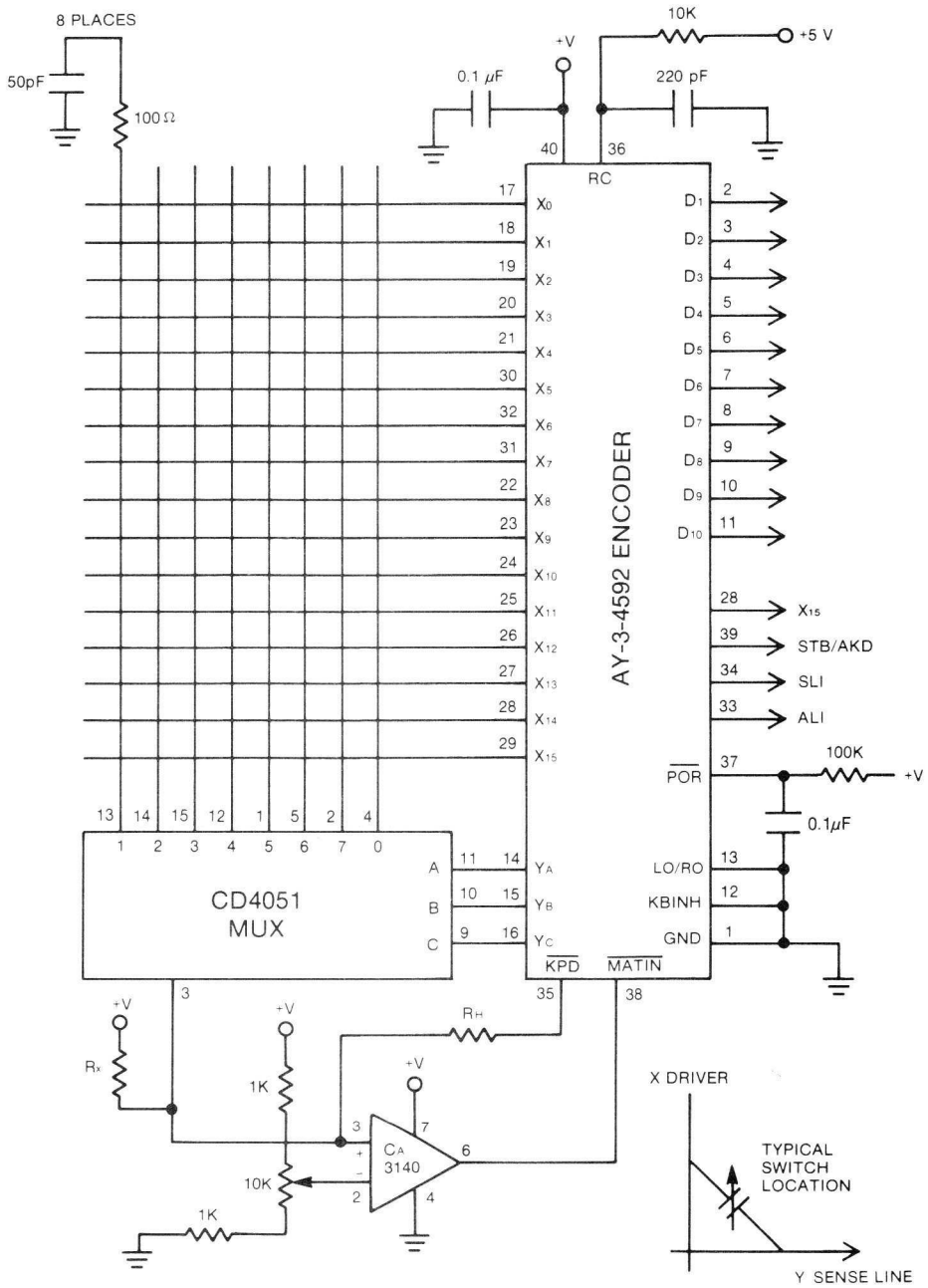


Fig. 1 SAMPLE KEYBOARD DESIGN ROM CODED KEYS

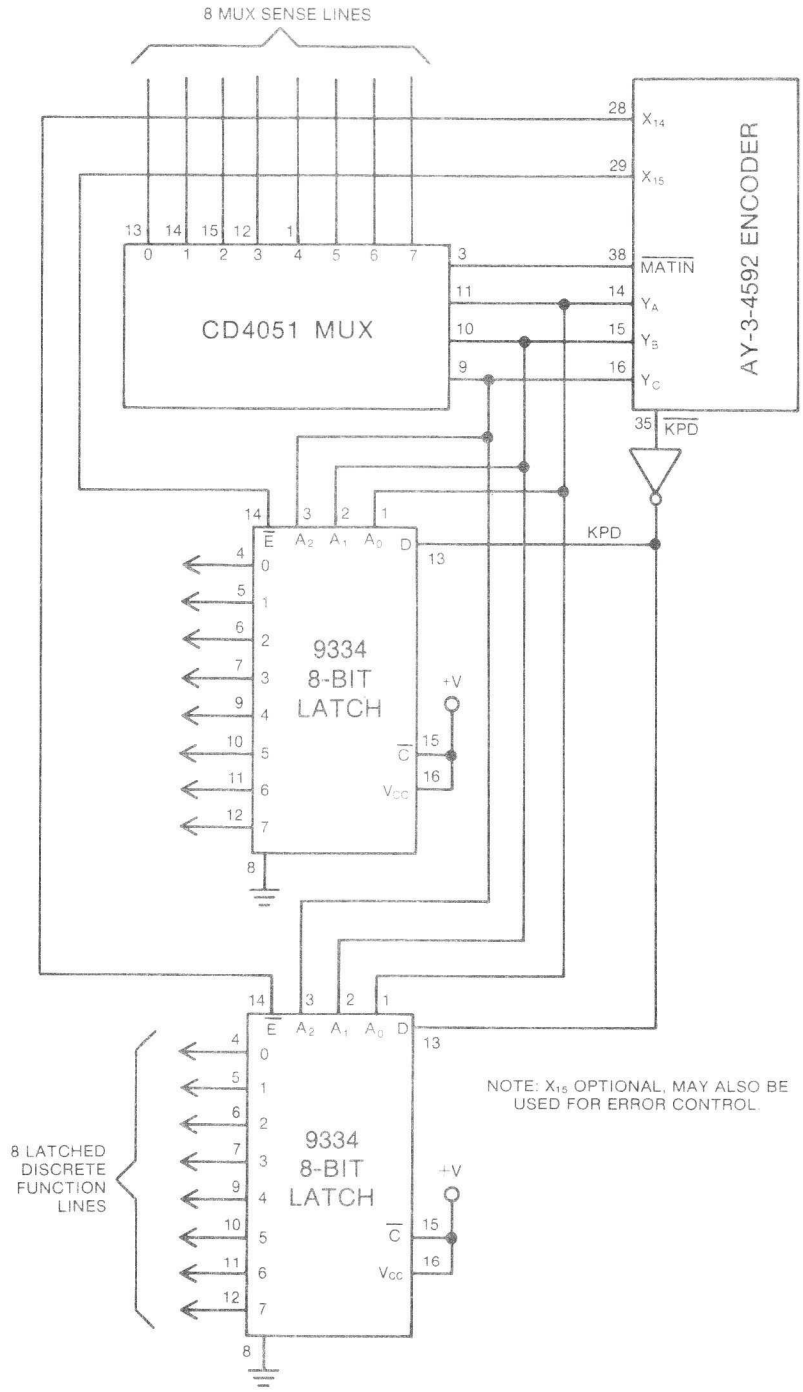


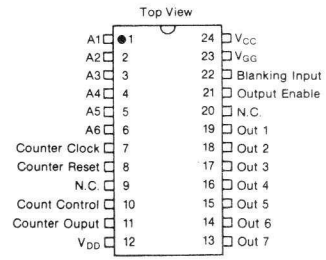
Fig. 2 SAMPLE KEYBOARD DESIGN DISCRETE FUNCTION KEYS

Character Generator

FEATURES

- FULL TTL/DTL COMPATIBILITY
  No external interfacing components required.
- 1 μs TYP. ACCESS TIME/STATIC OPERATION
  The output data remains valid as long as the input data/internal counter remain unchanged.
- COLUMN OUTPUT
  2240 bits of storage organized as 64 5×7 dot matrix characters with column by column output.
- INTERNAL COUNTER
  Provides sequential column selection from a single counter clock input.
- COUNT CONTROL
  Allows the selection of either one or two column intercharacter spacing.
- COUNTER OUTPUT
  Provides an "update" signal for external character address registers.
- BLANKING AND OUTPUT ENABLE
  Provide full output control without affecting any other ROM function.
- ZENER PROTECTED INPUTS
- GLASS PASSIVATION PROTECTION

PIN CONFIGURATION
24 LEAD DUAL IN-LINE

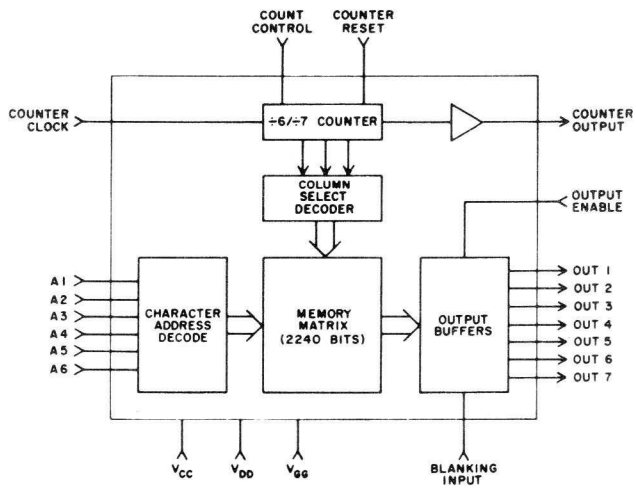


DESCRIPTION

The General Instrument RO-5-2240S is a 2240 bit Read Only Memory organized as a 320 words × 7 bits character generator (64 characters, each having 5 columns of 7 bits). Column by column character data is provided for vertical scan display applications. An internal counter and a full complement of control signals allow for the greatest system design flexibility. The RO-5-2240S is constructed on a single monolithic chip utilizing P-channel enhancement mode transistors.

The memory is available with custom character coding or preprogrammed with ASCII encoded characters having the fonts shown on Page 2 of this data sheet.

BLOCK DIAGRAM



OPERATING DESCRIPTION

Character selection is achieved by presenting a six-bit binary word at the Character Address inputs. Column selection is achieved by clocking an internal counter from the Counter Clock input. Column information appears sequentially at the seven Data Outputs, beginning with the left-most column.

Two additional column positions, aside from the five required for character presentation, are available for spacing between adjacent characters. The Count Control input is used to determine whether one or both positions will be used. Between characters, the Data Outputs are high (+5V), the "no-dot" condition. The Counter Reset input is available to reset the counter into the last (sixth or seventh) state.

The Counter Output is provided to synchronize other system components to the ROM internal counter. An output appears corresponding to the last (sixth or seventh) counter state and can be conveniently used to clock an external input data register.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM function. Data Outputs can also be open-circuited for wire-ORed operation by use of the Output Enable input.

Memory operation is static; refresh clocks are not required to maintain output information. The Counter Clock input is used only to select columns and need not be pulsed continuously.

OPERATING NOTES

The following table summarizes the RO-2240S input control states and corresponding drive levels:

Count Control
÷ 6 ..... −12
÷ 7 ..... +5V

Counter Reset
Operate ..... +5V
Reset ..... OV

Blanking Input
Unblank ..... +5V
Blank* ..... OV

Output Enable
Enable ..... +5V
Disable** ..... OV

* All data outputs high (+5V)
**All data outputs open-circuited

TIMING DIAGRAMS

Timing diagram (1) shows the time relationships between character address, data output, counter clock and counter output during typical operation of an RO-5-2240S character generator. An output sequence from the RO-5-2240S-001 is shown to help clarify operation. This sequence can be seen from the top rows (OUT_1) of the characters "I" and "N".

	"I"						"N"				
OUT_1	1	0	0	0	1	1	1	0	1	1	1	0
	1	1	0	1	1	1	1	0	1	1	1	0
	1	1	0	1	1	1	1	0	0	1	1	0
	1	1	0	1	1	1	1	0	1	0	1	0
	1	1	0	1	1	1	1	0	1	1	0	0
	1	1	0	1	1	1	1	0	1	1	1	0
OUT_7	1	0	0	0	1	1	1	0	1	1	1	0
	COUNT OF 7											

All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control, +5V
Counter Reset, +5V
Blanking Input, +5V
Output Enable, +5V

Had the Count Control input been at −12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.

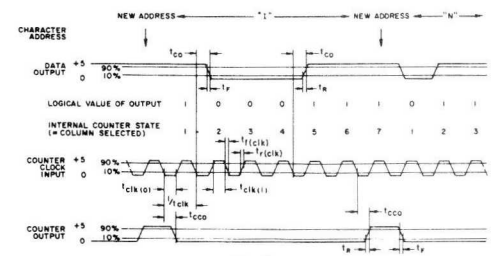


Fig.1

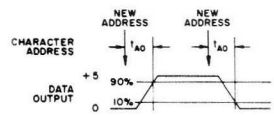


Fig.2

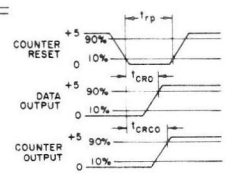


Fig.3

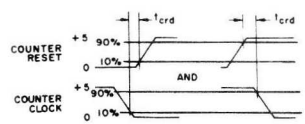


Fig.4

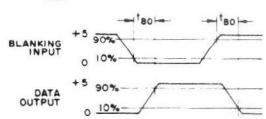


Fig.5

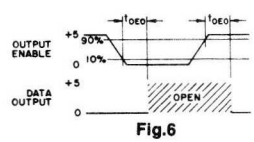


Fig.6

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{DD} with respect to V_{CC} . . . . . −20V to +0.3V
Inputs with respect to V_{CC} . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.25 Volts (V_{CC} is the substrate voltage)
V_{GG} = −12 Volts ±0.6 Volts
V_{DD} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 15 pF)

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs (Note 1)						
Logic 1 Level	V_{IH}	V_{CC}−1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$−6V, T_A = 25°C
Count Control						
÷6 Operation	V_{ICC}	−12.6	−12.0	−11.4	Volts	Returned to V_{GG} for ÷ 6 operation.
÷ 7 Operation	V_{ICC}	+4.75	+5.0	+5.25	Volts	Returned to V_{CC} for ÷ 7 operation
Leakage	I_{LCC}	—	—	10	μA	$V_{in} = V_{CC}$ − 6V, T_A = 25°C
Outputs (Note 2)						
Logic 1 Level	V_{OH}	2.8	—	—	Volts	I_{OH} = 100 μA
Logic 0 Level	V_{OL}	—	—	0.4	Volts	I_{OL} = 1.6 mA
Power						
Supply Current	I_{GG}	—	20	40	mA	Outputs unconnected,
Supply Current	I_{SS}	—	20	40	mA	f_{clk} = 200 kHz
AC CHARACTERISTICS						
Counter Clock						
Frequency	f_{clk}	DC	—	200	kHz	
Pulse Width	$t_{clk(0)}$	2.0	—	—	μs	
Pulse Delay	$t_{clk(1)}$	2.0	—	—	μs	$t_{f(clk)} + t_{clk(0)} + t_{r(clk)}$
Rise and Fall Times	$t_{r(clk)}, t_{f(clk)}$	—	—	100	ns	$+t_{clk}(0) \geqslant 5\mu$sec
Counter Reset						
Pulse Width	t_{rp}	1.0	—	—	μs	
Pulse Delay	t_{crd}	0.4	—	—	μs	Note (3)
Capacitance (Note 1)	C_{in}	—	—	10	pF	1 MHz, T_A = +25°C
Outputs						
Address to Output Delay	t_{AO}	—	1.0	1.5	μs	
Clock to Output Delay	t_{CO}	—	1.0	1.5	μs	
Clock to Counter Output Delay	t_{CCO}	—	1.0	1.5	μs	
Blanking/Unblanking Delay	t_{BO}	—	1.0	1.5	μs	
Output Enable/Disable Delay	t_{OEO}	—	1.0	1.5	μs	
Counter Reset Delay	t_{CRO}	—	1.0	1.5	μs	
Reset to Counter Output Delay	t_{CRCO}	—	1.0	1.5	μs	
Output Rise and Fall Time	t_r, t_f	—	—	0.3	μs	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
2. These parameters apply to both the data outputs and counter output.
3. The counter clock must not make a negative transition within the period t_{crd}, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

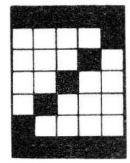
CODING AND CHARACTER FONTS

The RO-5-2240S-001 is a pre-programmed member of the RO-5-2240S series with ASCII encoding and the character fonts shown on the right. A logic "1" represents an input or output voltage equal to V_{SS} (+5V) and a logic "0" represents a voltage equal to V_{DD} (0V).

An example demonstrating the correspondence of device outputs and sequence to the 5×7 dot matrix fonts is shown below:

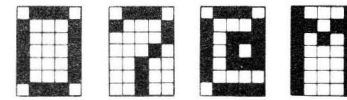
	1	2	3	4	5
OUT_1 →	0	0	0	0	0
OUT_2 →	1	1	1	1	0
OUT_3 →	1	1	1	0	1
OUT_4 →	1	1	0	1	1
OUT_5 →	1	0	1	1	1
OUT_6 →	0	1	1	1	1
OUT_7 →	0	0	0	0	0

output sequence



The RO-5-2240S-002 is pre-programmed with a character font identical to the font for the RO-5-2240S-001 below with the exception of the characters '0', '?', '@', and 'M'.

The RO-5-2240S-002 font for these characters is shown below:



RO-5-2240S-001				A_6	1	1	0	0
				A_5	0	1	0	1
A_4	A_3	A_2	A_1	COL	2	3	4	5
				ROW				
0	0	0	0	0				
0	0	0	1	1				
0	0	1	0	2				
0	0	1	1	3				
0	1	0	0	4				
0	1	0	1	5				
0	1	1	0	6				
0	1	1	1	7				
1	0	0	0	8				
1	0	0	1	9				
1	0	1	0	10				
1	0	1	1	11				
1	1	0	0	12				
1	1	0	1	13				
1	1	1	0	14				
1	1	1	1	15				

RO-3-2513

Character Generator

FEATURES

- 64×8×5 Organization — ideal for systems requiring a row scan 5×7 dot matrix character generator
- Single +5 Volt Supply
- TTL Compatible — all inputs and outputs
- Static Operation — no clocks required
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs — under the control of an 'Output Inhibit' input to simplify memory expansion
- Standard ASCII (RO-3-2513/CGR-001) or Totally Automated Custom Programming Available
- Zener Protected Inputs
- Glass Passivation Protection

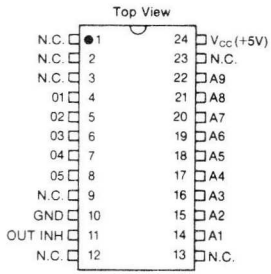
DESCRIPTION

The General Instrument RO-3-2513 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for use as a Character Generator. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2513 can store, for high speed raster scan CRT displays, a full 64 characters in a standard 5×7 dot matrix format.

The RO-3-2513 is available pre-programmed with ASCII encoded 5×7 characters (GI part no. RO-3-2513/CGR-001) a direct replacement in pin connection, operation, and character font for the Signetics 2513/CM2140. The RO-3-2513 is also available pre-programmed with lower case ASCII encoded 5×7 characters (GI part no. RO-3-2513/CGR-005), a direct replacement for the Signetics 2513/CM3021.

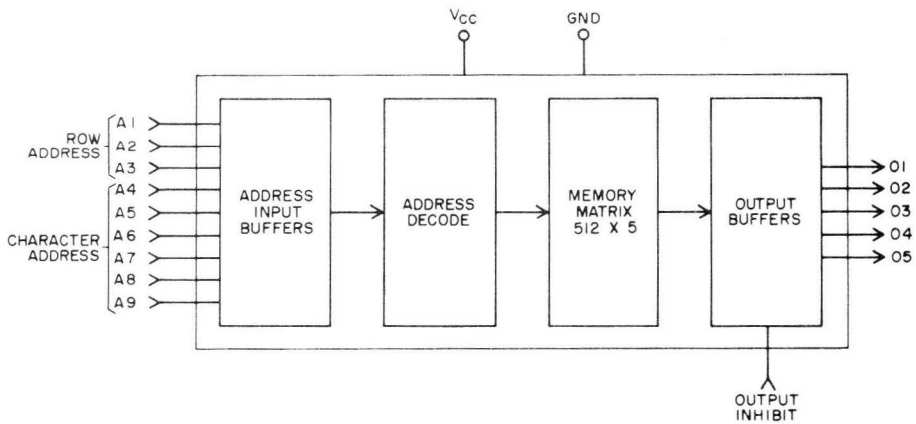
PIN CONFIGURATION

24 LEAD DUAL IN LINE



A separate publication, "RO-3-2513 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2513 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

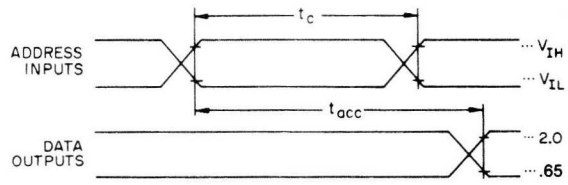
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF.

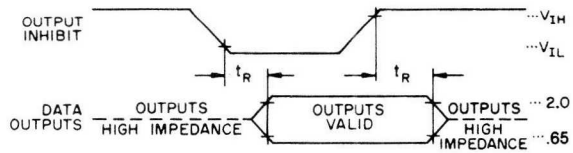
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	25	33	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



A. ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



B. INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

MEMORY

RO-3-2513-001 STANDARD PATTERN CHARACTER FORMAT (Upper Case ASCII)

The RO-3-2513/CGR-001 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5×7 dot matrix font is shown below:

CHARACTER ADDRESS

RO-3-2513/CGR-001 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII upper case "S" Character	0	1	0	0	1	1

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0

RO-3-2513/CGR-001 CHARACTER ADDRESS A_6 A_5 A_4	A_9 A_8 A_7 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

RO-3-2513-005 STANDARD PATTERN CHARACTER FORMAT (Lower Case ASCII)

The RO-3-2513/CGR-005 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5×7 dot matrix font is shown below.

CHARACTER ADDRESS

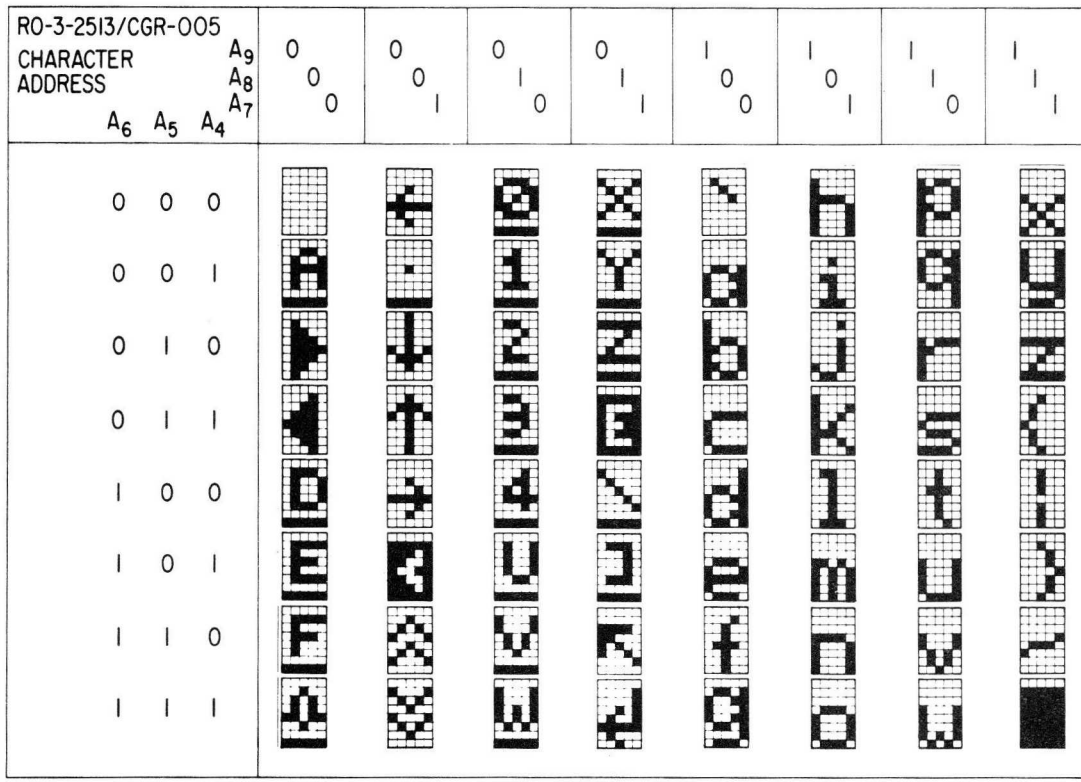
RO-3-2513/CGR-005 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII lower case 's' Character	1	1	0	0	1	1

ROW ADDRESS

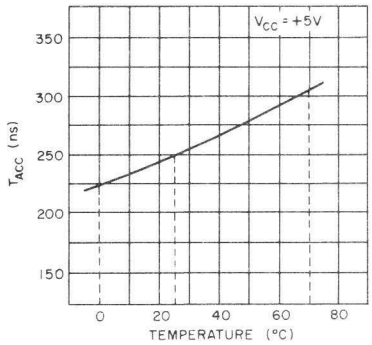
A3	A2	A1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

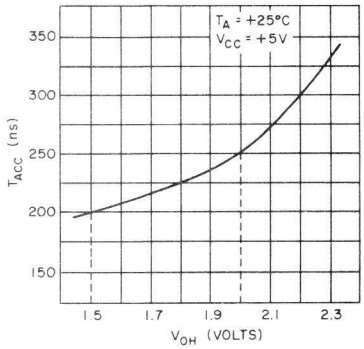
05	04	03	02	01
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	1	1	0
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	1	1	1	0



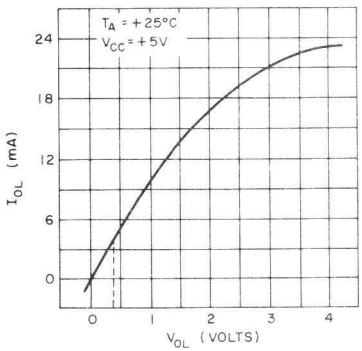
TYPICAL CHARACTERISTIC CURVES



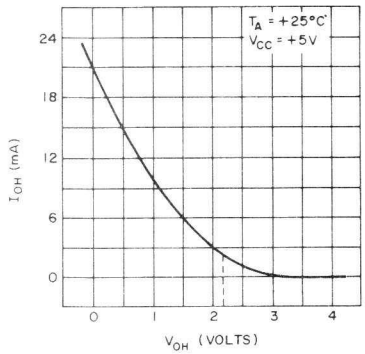
ACCESS TIME vs. TEMPERATURE



ACCESS TIME vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

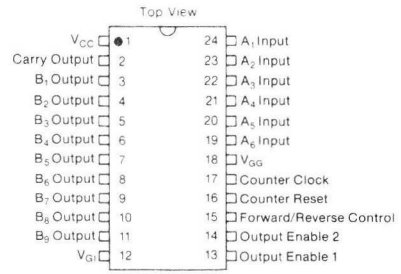
Character Generator

FEATURES

- Designed to drive Needle Printers.
- Internal counter provides sequential column scanning.
- Forward/Reverse Control for left to right and right to left printing capability.
- Carry Output available for synchronization.
- Three-State output configuration.
- Two mask programmable Output Enable pins to allow memory expansion.
- ASC II coded standard part, RO-5-5184-3000.
- Mask programmable counter length to allow flexibility in character organization.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



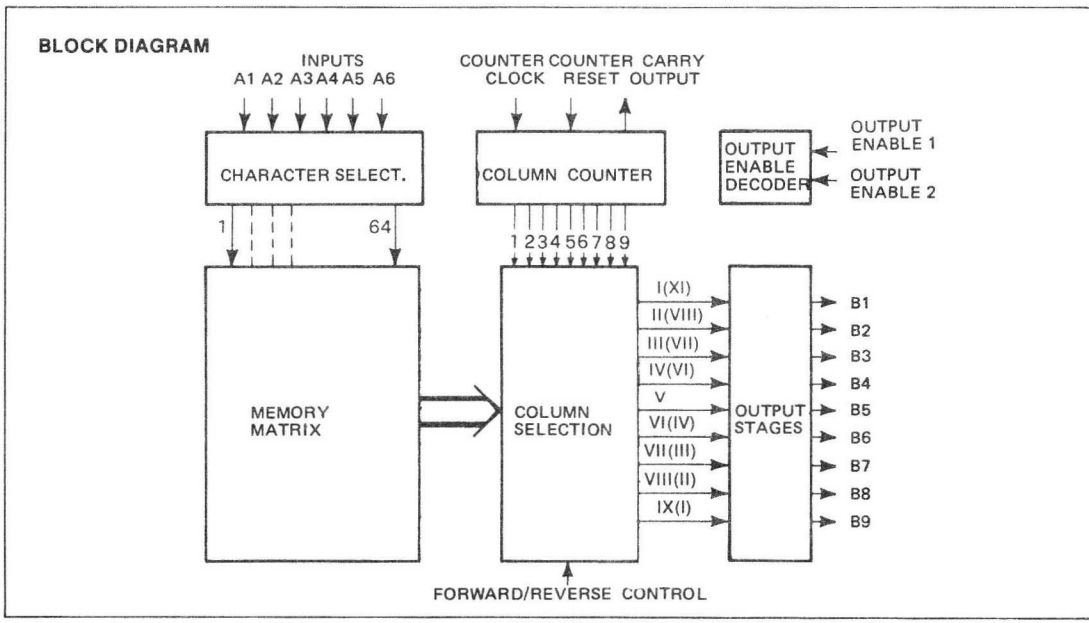
DESCRIPTION

The RO-5-5184 is a 5184 bit Static Read Only Memory organized as 64 permanent storage locations of 81 bits each (9 × 9 character matrix). Six address lines are used for the selection of 64 different characters. An internal ring counter is provided for column scanning; column information appears sequentially on the 9 output lines. A Counter Reset Input is available to initialize the sequential scanning. A Carry Output is provided to synchronize external circuitry to the internal column counter. The Forward/Reverse Control allows scanning from left to right or from right to left.

The 9 output lines have tri-state configuration. Two mask programmable Output Enable pins are provided for expansion up to a 5184 × 4 bit system without external logic.

Low threshold P-channel enhancement mode metal gate technology is used for input/output direct TTL compatibility. All inputs are zener protected.

BLOCK DIAGRAM



MEMORY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC} . . . . . −20V to +0.3V
Temperature Range . . . . . −55°C to +125°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied — operating conditions are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±0.5V
V_{GI} = GND
V_{GG} = −12V ±1V

Characteristics apply over temperature range unless otherwise stated.

Characteristic	Min	Typ**	Max	Units	Conditions
Counter Clock Input					
Repetition Rate	D.C.	350	200	kHz	
Pulse Width, ϕw	1.2	—	—	μs	At a logic '1' level
Pulse Separation, ϕs	1.2	—	—	μs	At a logic '0' level
Rise & Fall Times, tr, tf	—	—	1.0	μs	
Logic '0' Level, V_{IL}	—	—	+0.8	Volts	
Logic '1' Level, V_{IH}	V_{CC}−1.5	—	—	Volts	
Input Leakage, I_{IN}	—	—	10	μA	Measured at $V_{IN} = V_{CC}$−10V at 25°C
Input Capacitance, C_{IN}	—	10	—	pF	$V_{IN} = V_{CC}$, f = 1MHz
Address Inputs					
Logic '0' Level, V_{IL}	—	—	+0.8	Volts	
Lotic '1' Level, V_{IH}	V_{CC}−1.5	—	—	Volts	
Input Leakage, I_{IN}	—	—	10	μA	Measured at $V_{IN} = V_{CC}$−10V at 25°C
Input Capacitance, C_{IN}	—	10	—	pF	$V_{IN} = V_{CC}$, f= 1MHz
Reset Input					
Counter Clock to Reset					
Pulse delay, t_{CRD}.	1.0	—	—	μs	Fig.1
Reset pulse width	3.0	—	—	μs	Fig.2
Data Outputs					
Logic '0' Level, V_{OL}	—	—	0.4	Volts	I_{OL} = 1.6mA
Logic '1' Level, V_{OH}	V_{CC}−1.0	—	—	Volts	I_{OH} = 100 μA
Clock to Output delay time, t_{CO}	—	2.5	3.5	μs	
Clock to Carry Output delay time, t_{CC}	—	1.5	2.5	μs	Figs. 3,4,5,6,7, & 8
Address to Output delay time, t_{AO}	—	2.5	3.5	μs	1 TTL, 10pF load
Reset to Output delay time, t_{RES}	—	2.5	5.0	μs	T_A = 25°C
Forward/Reverse to Output delay time, t_{FRO}	—	2.5	3.5	μs	
Output Enable delay time, t_{OEO}	—	1.5	2.5	μs	
Power Consumption, P_D	—	250	—	mW	T_A = 25°C

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

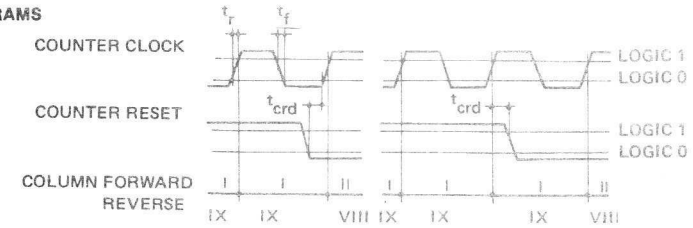


Fig.1 CLOCK TO RESET DELAY TIME

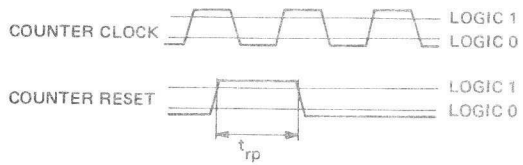


Fig.2 RESET PULSE WIDTH

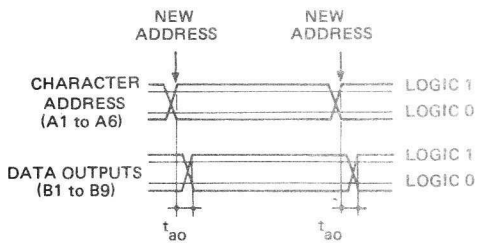


Fig.3 ADDRESS TO OUTPUT DELAY TIME

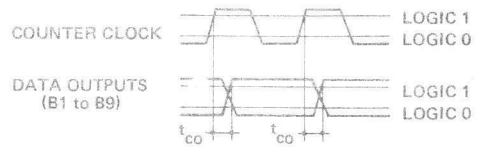


Fig.4 CLOCK TO OUTPUT DELAY TIME

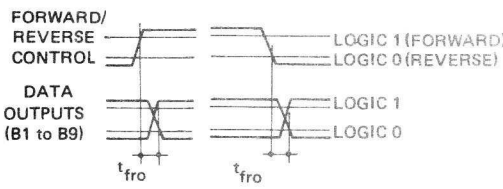


Fig.5 FORWARD/REVERSE TO OUTPUT DELAY TIME

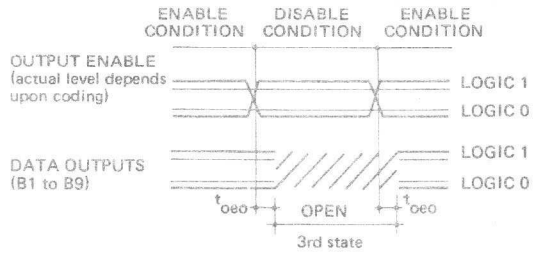


Fig.6 OUTPUT ENABLE TO OUTPUT DELAY TIME

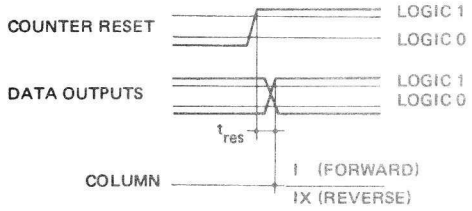


Fig.7 RESET TO OUTPUT DELAY TIME

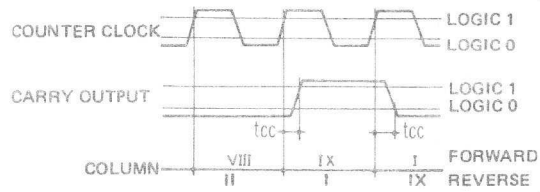


Fig.8 CLOCK TO CARRY DELAY TIME

MEMORY

OPERATION

CHARACTER SELECTION

Six address inputs are provided for selection of the 64 different characters. The address inputs are binary weighted (A_1 is the LSB).

COLUMN SELECTION

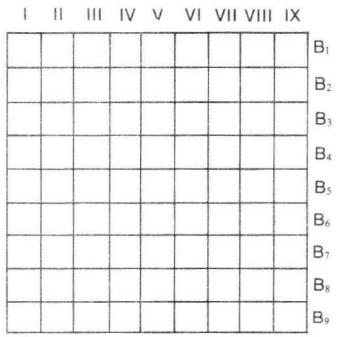
Column selection depends upon Forward/Reverse Control which permits the scanning of characters either from the first (I) to the last (IX) or from the last (IX) to the first (I) column as shown in fig.9. By changing line by line the logic value of Forward/Reverse control printing alternatively left to right or right to left is possible (see fig.10).

This feature allows faster printing by eliminating the fly back dead time between lines. The logic level of Forward/Reverse Control has to be constant "1" for left to right scanning and constant "0" for right to left scanning.

Fig.9 COLUMN SELECTION

FORWARD				REVERSE			
Count Reset	Column Count. State	Charact. Column	Carry Outp.	Count Reset	Column Count. State	Charact. Column	Carry Outp.
0	1	I	0	0	1	IX	0
0	2	II	0	0	2	VIII	0
0	3	III	0	0	3	VII	0
0	4	IV	0	0	4	VI	0
0	5	V	0	0	5	V	0
0	6	VI	0	0	6	IV	0
0	7	VII	0	0	7	III	0
0	8	VIII	0	0	8	II	0
0	9	IX	1	0	9	I	1
0	1	I	0	0	1	IX	0
0	2	II	0	0	2	VIII	0
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
0	8	VIII	0	0	8	II	0
0	9	IX	1	0	9	I	1
1	1	I	0	1	1	IX	0
1	1	I	0	1	1	IX	0
1	1	I	0	1	1	IX	0

CHARACTER MATRIX



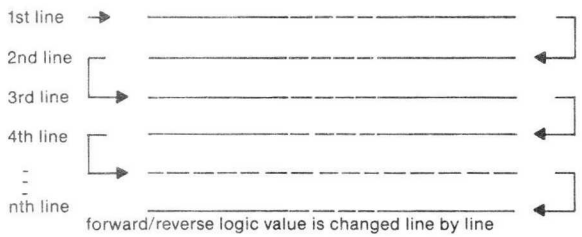


Fig.10 FORWARD/REVERSE PRINTING

OUTPUT ENABLE DECODER

Two Output Enable lines are provided for chip selection, when a chip is not selected the outputs are disabled (high impedance).

Output Enable signals are internally decoded by a mask programmable decoder to minimize logic for memory expansion.

The output enable code assigned to different RO-5-5184 is permanently programmed into the ROM at the same time as the custom data pattern.

A system of $4 \times 5184 = 20736$ bit character generator needing no external enable logic is easily obtained wiring the outputs of four different RO-5-5184 together as shown on fig.11.

OUTPUT ENABLE CODING						
RO-5-5184	Output Enable 1	Output Enable 2	DEVICE SELECTION			
			A	B	C	D
A	0	0	selected	—	—	—
B	1	0	—	selected	—	—
C	0	1	—	—	selected	—
D	1	1	—	—	—	selected

COLUMN COUNTER

This counter operates on the positive going edges of the Counter Clock.

Each counter cell is implemented with a cross coupled flip-flop so that the counter position is fully static.

Carry Output is active (logic '1') when the counter is in the last position, to indicate that a character has been fully scanned.

When active (logic '1') the Counter Reset Input resets the counter in the first position to initialise the scanning.

The counting length is mask programmable, it is possible to program any length between five and nine.

OUTPUT STAGES

Nine TTL compatible Outputs (B_1 to B_9) are provided to show the memory content.

The Tri-state configuration of output stages allows bus structure for memory expansion under the control of Output Enable signals.

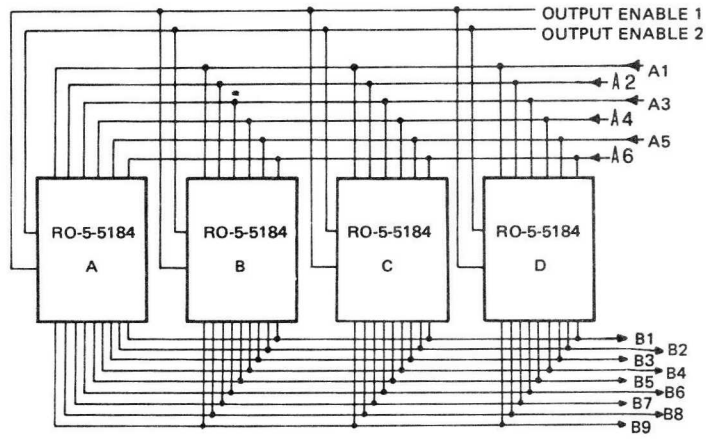


Fig. 11

RO-5-5184-050 STANDARD PATTERN CHARACTER FORMAT

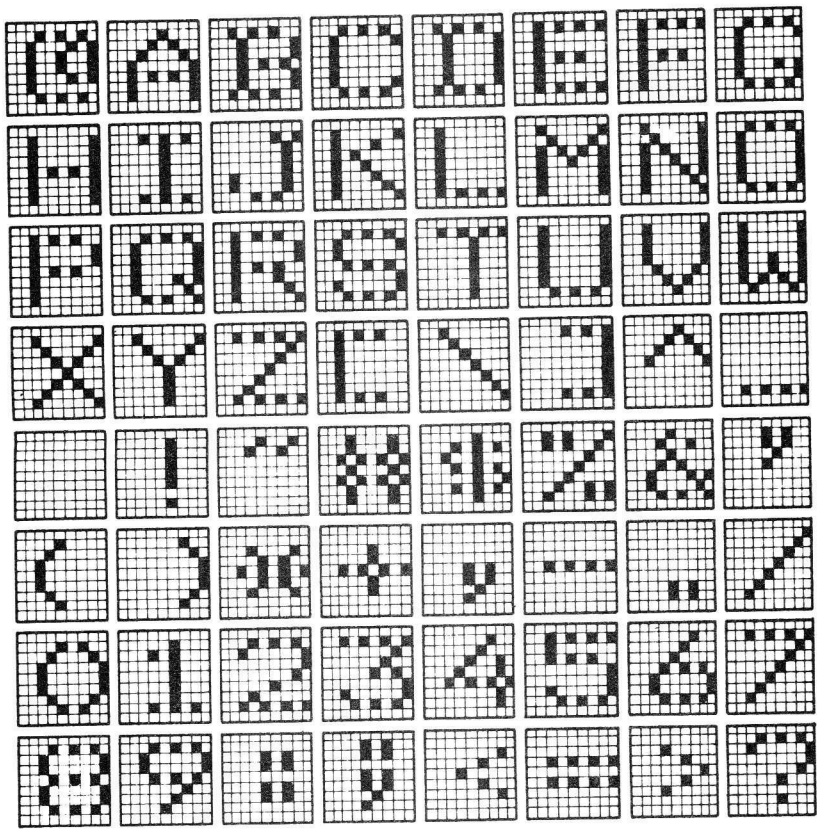
INPUT ADDRESS									
	A 1	0	1	0	1	0	1	0	1
	A 2	0	0	1	1	0	0	1	1
	A 3	0	0	0	0	1	1	1	1

A6 A5 A4

COUNTER STATE → 123456789 123456789 123456789 123456789 123456789 123456789 123456789 123456789

OUTPUT ↓ 987654321

000 001 010 011 100 101 110 111



SHADED SQUARE	+5	0
BLANK SQUARE	0	+5
DESIRED OUTPUT VOLTAGE	X	

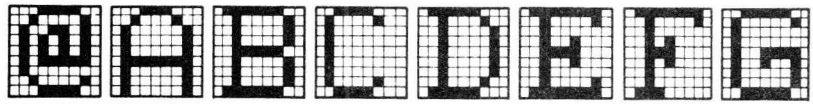
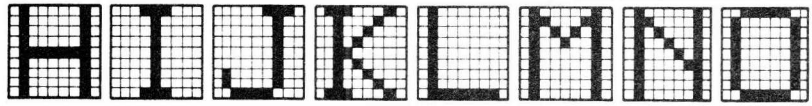
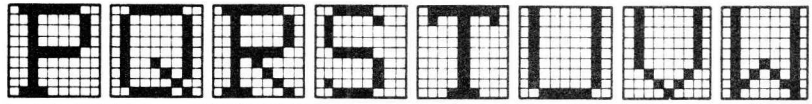
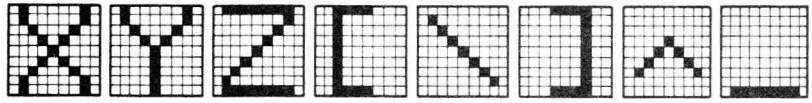
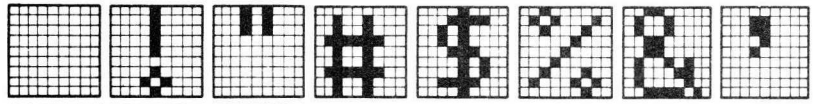
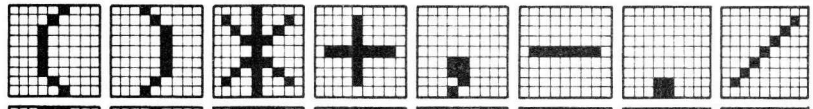
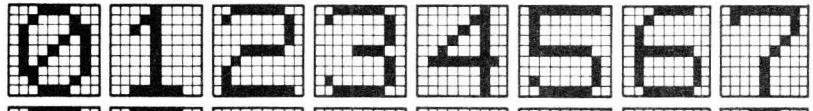
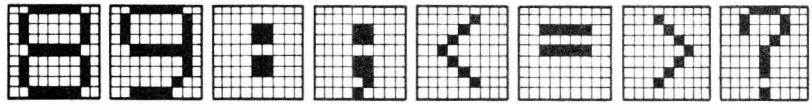
OUTPUT ENABLE 1	0	+5	0	+5
OUTPUT ENABLE 2	0	0	+5	+5
DEVICE SELECTED	X			

RO-5-5184-3000 STANDARD PATTERN CHARACTER FORMAT

INPUT ADDRESS									
A1	0	1	0	1	0	1	0	1
A2	0	0	1	1	0	0	1	1
A3	0	0	0	0	1	1	1	1

COUNTER STATE → 123456789 123456789 123456789 123456789 123456789 123456789 123456789 123456789

OUTPUT ↓ 987654321

A6 A5 A4	
0 0 0	
0 0 1	
0 1 0	
0 1 1	
1 0 0	
1 0 1	
1 1 0	
1 1 1	

SHADED SQUARE	+5	0
BLANK SQUARE	0	+5
DESIRED OUTPUT VOLTAGE		×

OUTPUT ENABLE 1	0	+5	0	+5
OUTPUT ENABLE 2	0	0	+5	+5
DEVICE SELECTED				×

MEMORY

STATIC SHIFT REGISTERS

FUNCTION	DESCRIPTION	PART NUMBER			PAGE NO.
		0 to 70° C	–55 to +125° C	0 to 70° C	
VARIABLE	32 bit variable length	SS-5-1032	SS-6-1032	—	4-106
DUAL REGISTERS	Dual 16 bit	SS-5-8211	SS-6-8211	SS-7-2016	4-124
		SS-5-8212	SS-6-8212	SS-7-8212	4-126
	Dual 50 bit	SL-5-2050	SL-6-2050	SL-7-2050	4-108
	Dual 64 bit	SL-5-2064	SL-6-2064	SL-7-2064	4-110
	Dual 100 bit	SL-5-C2100	—	SL-7-C2100	4-112
	Dual 128 bit	SL-5-2128	—	SL-7-2128	4-114
		SL-5-C2128	—	—	4-116
QUAD REGISTERS	Quad 16 bit	SL-5-4016	—	SL-7-4016	4-118
	Quad 25 bit	SL-5-4025	SL-6-4025	SL-7-4025	4-120
	Quad 32 bit	SL-5-4032	SL-6-4032	SL-7-4032	4-122

SS-5-1032
SS-6-1032

Variable Length Static Shift Registers

FEATURES

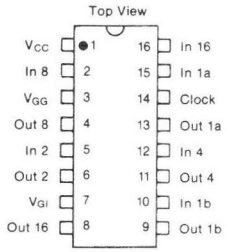
- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SS-5: 0°C to +70°C
  SS-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

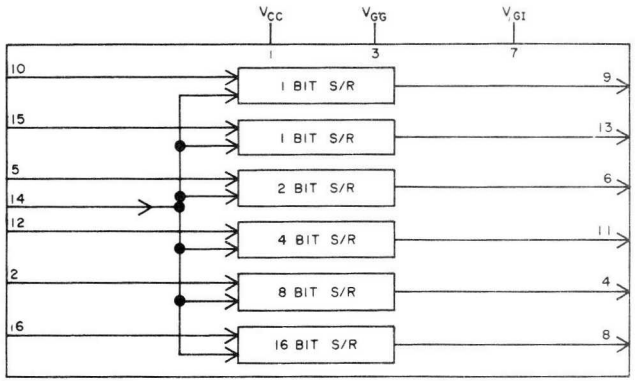
The SS-5-1032 and SS-6-1032 are 32-bit static shift registers consisting of 1, 1, 2, 4, 8 and 16-bit individual registers with common clock and separate data inputs and outputs. The device is constructed on a monolithic chip utilizing P-Channel enhancement mode transistors. It is compatible with TTL/DTL and MOS logic without the use of any special interface components.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



TIMING DIAGRAM

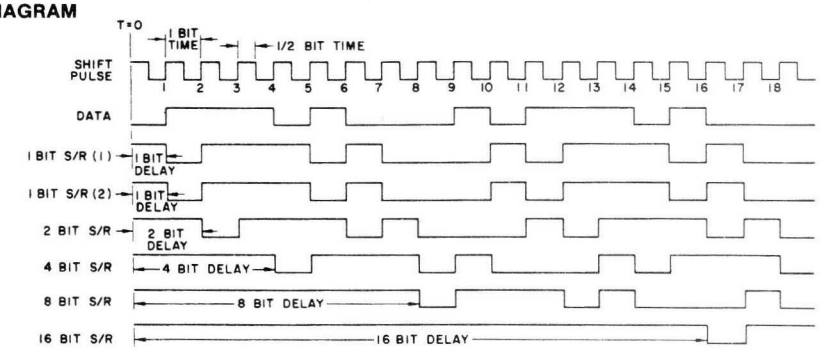


Fig.1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} and V_{GG} (with respect to V_{CC}) ..... -20V to +0.3V
Clock and Logic Input Voltages (with respect to V_{CC}) ... -15V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature: SS-5-1032 ..... 0°C to +70°C
SS-6-1032 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

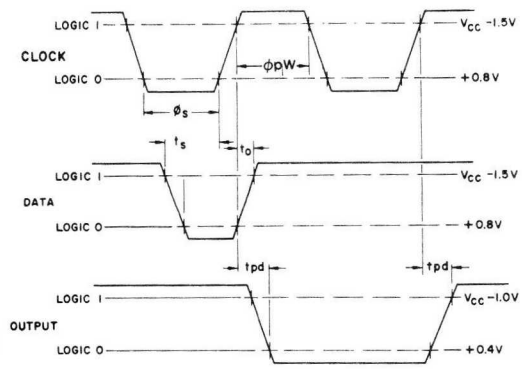
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} = Substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SS-5-1032)
= -55°C to +125°C (SS-6-1032)

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input (See Fig.2)					
Repetition Rate	DC	—	1	MHz	
Clock Pulse Width (ϕpW)	450	—	—	ns	
Pulse Separation (ϕs)	450	—	—	ns	
Logic Levels					
Logic '0'	—	—	+0.8	V	
Logic '1'	(V_{CC}-1.5)	—	—	V	
Input Capacitance	—	10	20	pF	Measured at V_{in} = V_{CC}
Input Impedance	1.0	—	—	MΩ	
Rise and Fall Time	—	—	1	μs	
Noise Immunity	+0.4	—	—	V	
Data Input (See Fig.2)					
Pulse Width (SD_W)	200	—	—	ns	
Set Up Time, t_s	200	—	—	ns	
Data Overlap, t_o	25	—	—	ns	
Logic Levels					
Logic '0'	—	—	+0.8	V	
Logic '1'	(V_{CC}-1.5)	—	—	V	
Input Capacitance	—	5	10	pF	Measured at V_{in} = V_{CC}
Input Impedance	1.0	—	—	MΩ	
Noise Immunity	+0.4	—	—	V	
Data Output (See Fig.2)					
Logic '0'	—	—	+0.4	V	1_{OL} = 1.6mA
Logic '1'	(V_{CC}-1.0)	—	—	—	1_{OH} = 100 μA
Propagation Delay,	—	—	450	ns	See Fig.2
Total Power Consumption	—	200	—	mW	Nominal Power Supply

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



The data is clocked in during the Logic "0" state of the clock and should be present and stable in its required state for 200 nsec with 25 nsec after the clock changes from logic "0" to "1". The data in the register will shift toward the output upon the positive transition of the clock.

Fig.2

MEMORY

SL-5-2050
SL-6-2050
SL-7-2050*

Dual 50-Bit Static Shift Registers

FEATURES

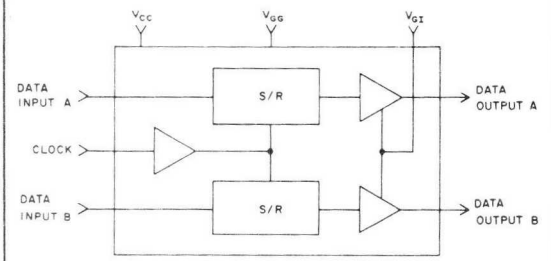
- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SL-5 & SL-7: 0°C to +70°C
  SL-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The SL-5-2050, SL-6-2050 and SL-7-2050 are dual 50-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent common clock 50-bit DC to 1MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

*Available only in Europe (14 Lead Plastic DIP)

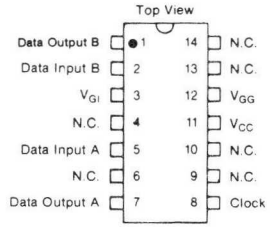
BLOCK DIAGRAM



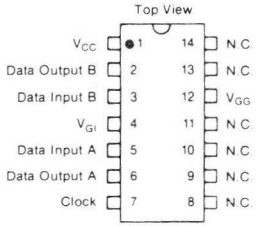
PIN CONFIGURATIONS

14 LEAD DUAL IN-LINE

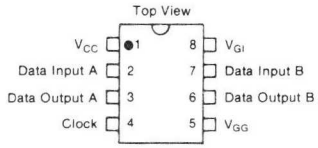
SL-5-2050, SL-6-2050



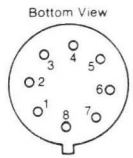
SL-7-2050*



8 LEAD DUAL IN-LINE



8 LEAD TO-78



1 Data Input A
2 Data Output A
3 Clock
4 V_{CC}
5 V_{GG}
6 Data Output B
7 Data Input B
8 V_{GI}

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: SL-5-2050, SL-7-2050 .... 0°C to +70°C
SL-6-2050 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

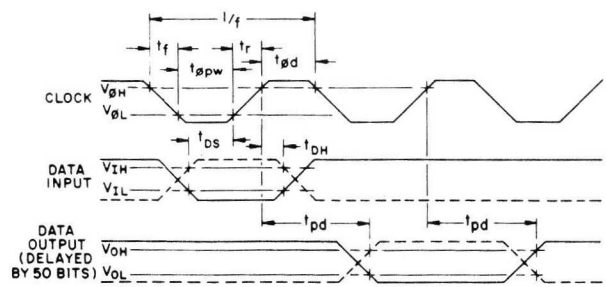
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SL-5-2050, SL-7-2050)
= -55°C to +125°C (SL-6-2050)
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	200	275	mW	SL-5-2050, SL-7-2050
	—	—	200	300	mW	SL-6-2050
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	1.0	MHz	
Pulse Width	$t_{\phi pw}$	450	250	—	ns	$t_f + t_{\phi pw} + t_r$
Pulse Delay	$t_{\phi d}$	450	—	—	ns	$\pm t_{\phi d} \geq 1$ μsec
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	20	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	350	250	—	ns	
Hold Time	t_{DH}	10	0	—	ns	
Capacitance	C_I	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	300	400	ns	SL-5-2050, SL-7-2050
	t_{pd}	—	300	500	ns	SL-6-2050

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



MEMORY

SL-5-2064
SL-6-2064
SL-7-2064*

Dual 64-Bit Static Shift Registers

FEATURES

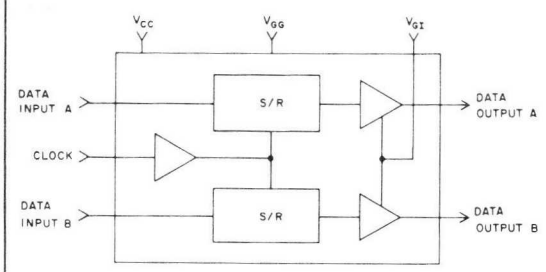
- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SL-5 & SL-7: 0°C to +70°C
  SL-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The SL-5-2064, SL-6-2064 and SL-7-2064 are dual 64-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent common clock 64-bit DC to 1MHz shift register, constructed on a single monolithic chip utilizing MTNS P—Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

*Available only in Europe (14 Lead Plastic DIP)

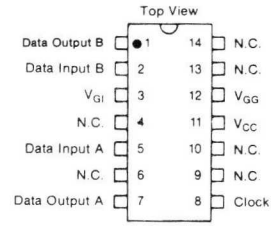
BLOCK DIAGRAM



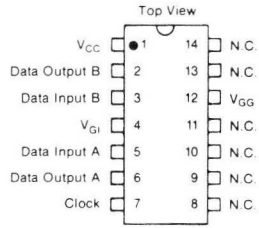
PIN CONFIGURATIONS

14 LEAD DUAL IN-LINE

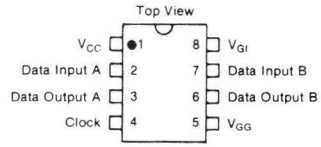
SL-5-2064, SL-6-2064



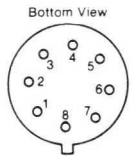
SL-7-2064*



8 LEAD DUAL IN-LINE



8 LEAD TO-78



1 Data Input A
2 Data Output A
3 Clock
4 V_{CC}
5 V_{GG}
6 Data Output B
7 Data Input B
8 V_{GI}

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: SL-5-2064, SL-7-2064 ... 0°C to +70°C
SL-6-2064 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

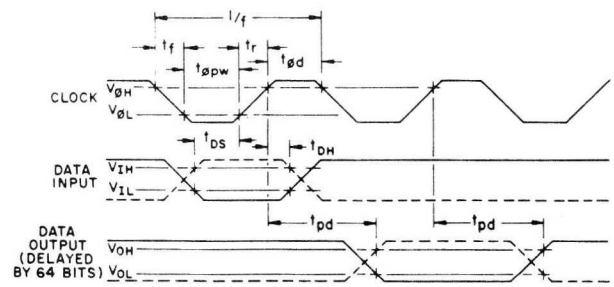
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SL-5-2064, SL-7-2064)
= -55°C to +125°C (SL-6-2064)
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100 μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	200	275	mW	SL-5-2064, SL-7-2064
	—	—	200	300	mW	SL-6-2064
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	1.0	MHz	
Pulse Width	$t_{\phi pw}$	450	250	—	ns	$t_f + t_{\phi pw} + t_r$
Pulse Delay	$t_{\phi d}$	450	—	—	ns	$+t_{\phi d} \geq 1$ μsec
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	20	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	350	250	—	ns	
Hold Time	t_{DH}	10	0	—	ns	
Capacitance	C_I	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	300	400	ns	SL-5-2064, SL-7-2064
	t_{pd}	—	300	500	ns	SL-6-2064

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



SL-5-C2100
SL-7-C2100*

Dual 100-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Zener Protected Inputs
- Glass Passivation Protection

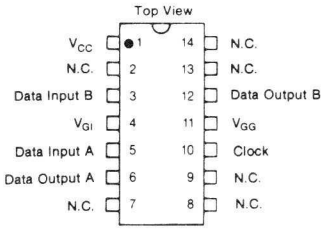
DESCRIPTION

The SL-5-C2100 and SL-7-C2100 are dual 100-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. This device contains two independent common clock 100-bit DC to 2MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transistion.

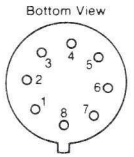
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATIONS

14 LEAD DUAL IN-LINE

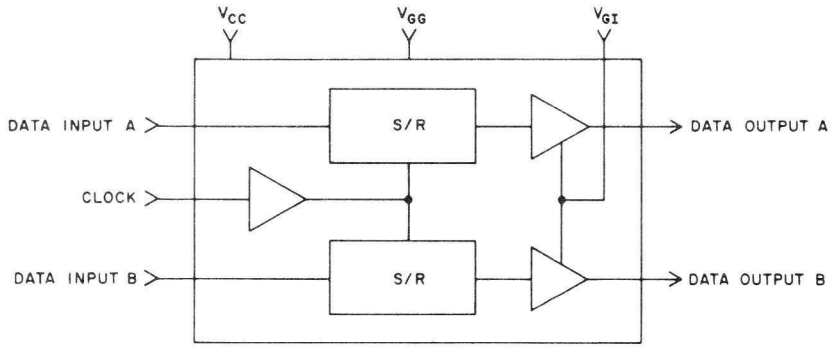


8 LEAD TO-99



1 Data Input A
2 Data Output A
3 Clock
4 V_{CC}
5 V_{GG}
6 Data Output B
7 Data Input B
8 V_{GI}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

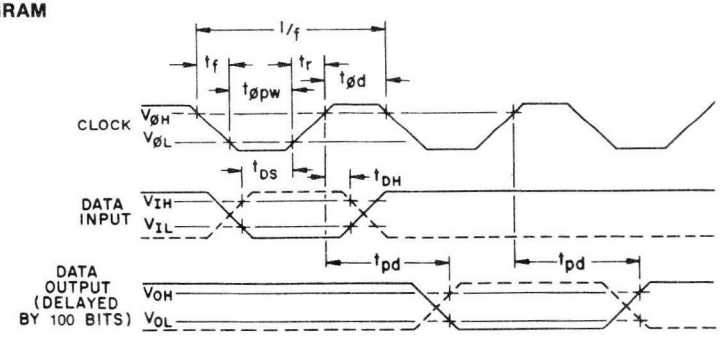
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	350	—	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	
Pulse Width	$t_{\phi pw}$	230	—	—	ns	$t_f + t_{\phi pw} + t_r$
Pulse Delay	$t_{\phi d}$	230	—	—	ns	$+t_{\phi d} \geq 1$ μsec
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	15	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	100	—	—	ns	
Hold Time	t_{DH}	50	—	—	ns	
Capacitance	C_I	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	200	—	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



MEMORY

SL-5-2128
SL-7-2128*

Dual 128-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Zener Protected Inputs
- Glass Passivation Protection

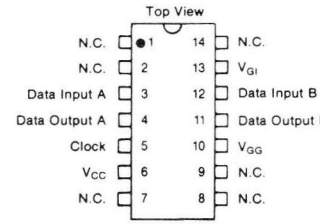
DESCRIPTION

The SL-5-2128 and SL-7-2128 are dual 128-static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent common clock 128-bit DC to 1MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

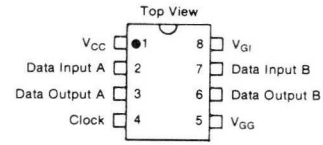
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATIONS

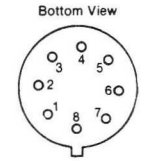
14 LEAD DUAL IN-LINE



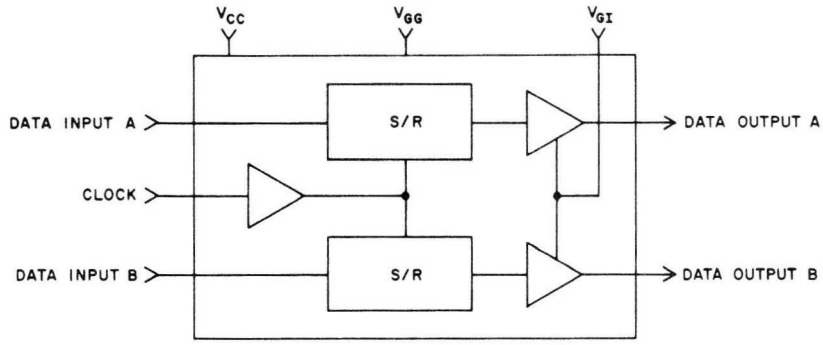
8 LEAD DUAL IN-LINE



8 LEAD TO-78



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

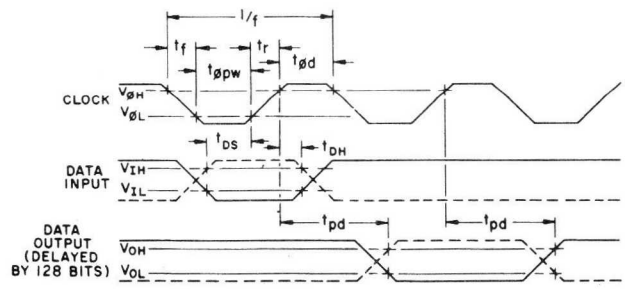
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	325	425	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	1.0	MHz	
Pulse Width	$t_{\phi pw}$	450	350	—	ns	$t_f + t_{\phi pw} + t_r + t_{\phi d} \geq 1$ μsec
Pulse Delay	$t_{\phi d}$	450	—	—	ns	
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	30	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	200	150	—	ns	
Hold Time	t_{DH}	100	50	—	ns	
Capacitance	C_I	—	10	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	300	400	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



MEMORY

Dual 128-Bit Static Shift Register

FEATURES

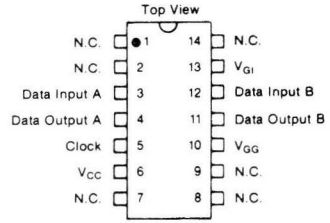
- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

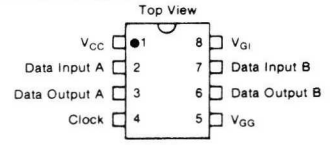
The SL-5-C2128 is a dual 128-bit static shift register with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. This device contains two independent common clock 128-bit DC to 2MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition

PIN CONFIGURATIONS

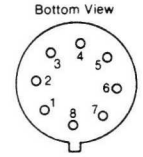
14 LEAD DUAL IN-LINE



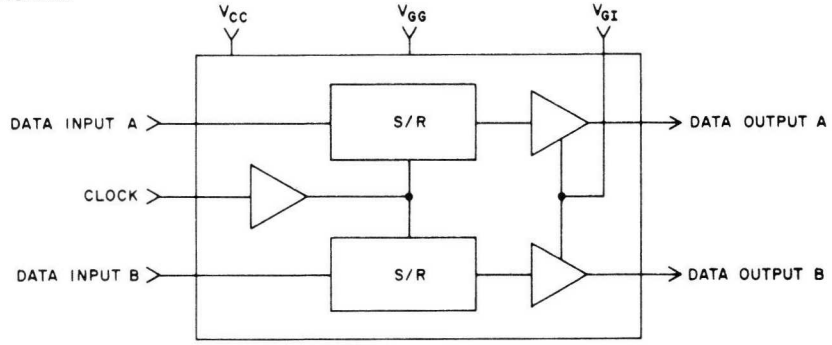
8 LEAD DUAL IN-LINE



8 LEAD TO-99



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functions operation of this device and these conditions is not implied—operating ranges are specified below.

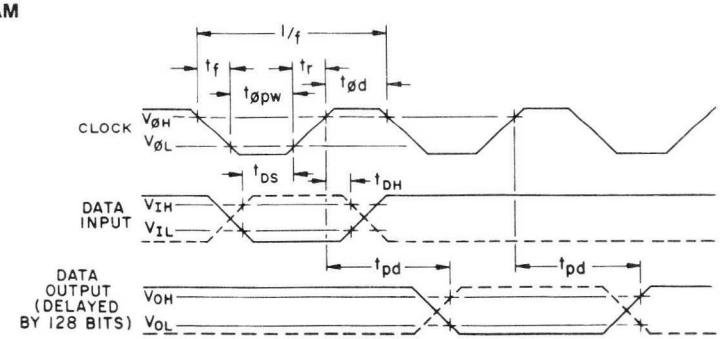
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100 μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	500	—	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	
Pulse Width	$t_{\phi pw}$	230	—	—	ns	$t_f + t_{\phi pw} + t_r$
Pulse Delay	$t_{\phi d}$	230	—	—	ns	$+t_{\phi d} \geq 1$ μsec
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	15	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	200	—	—	ns	
Hold Time	t_{DH}	25	—	—	ns	
Capacitance	C_I	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	—	300	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



MEMORY

SL-5-4016
SL-7-4016*

Quad 16-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Temperature Range:
  0°C to +70°C
- Zener Protected Inputs
- Glass Passivation Protection

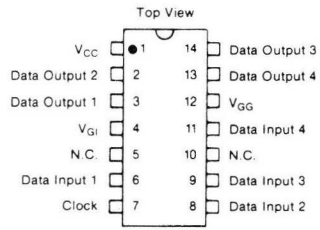
DESCRIPTION

The SL-5-4016 and SL-7-4016 are quad 16-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. This device contains four independent common clock 16-bit DC to 2MHz shift registers constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardles of the logic level of the clock. A single phase clock input is provided for all registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

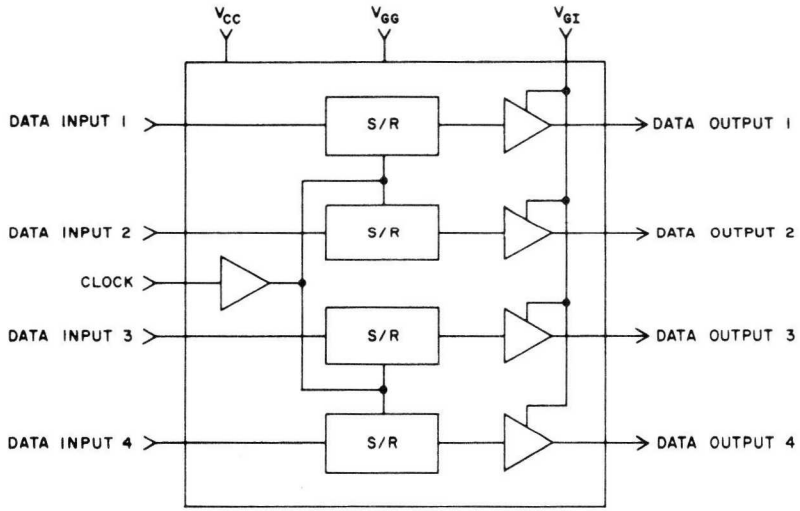
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATION

14 LEAD DUAL IN-LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

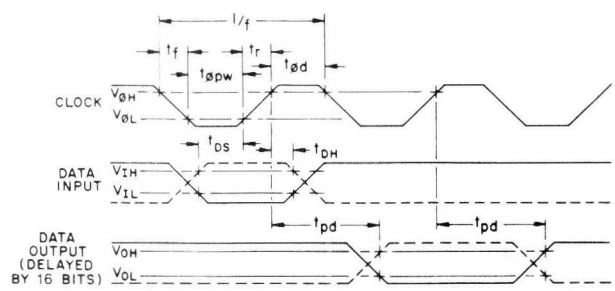
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100 μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	450	—	mW	
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	
Pulse Width	$t_{\phi pw}$	200	—	—	ns	$t_f + t_{\phi pw} + t_r$
Pulse Delay	$t_{\phi d}$	450	—	—	ns	$+t_{\phi d} \geq 1$ μsec
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	15	—	pF	1MHz, T_A = +25 C
Data Input						
Set Up Time	t_{DS}	150	—	—	ns	
Hold Time	t_{DH}	25	0	—	ns	
Capacitance	C_I	—	5	—	pF	1MHz, T_A = +25 C
Data Output						
Propagation Delay	t_{pd}	—	250	—	ns	

**Typical values are at +25 C and nominal voltages.

TIMING DIAGRAM



SL-5-4025
SL-6-4025
SL-7-4025*

Quad 25-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SL-5 & SL-7: 0°C to +70°C
  SL-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

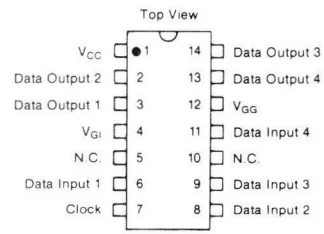
DESCRIPTION

The SL-5-4025, SL-6-4025 and SL-7-4025 are quad 25-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices each contain four independent common clock 25-bit DC to 1MHz shift registers respectively, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for all registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

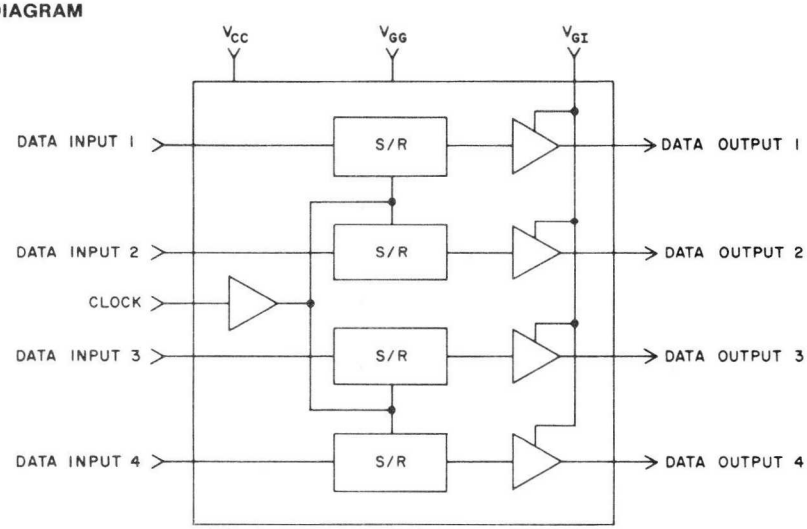
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATION

14 LEAD DUAL IN-LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: SL-5-4025, SL-7-4025.... 0°C to +70°C
SL-6-4025 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

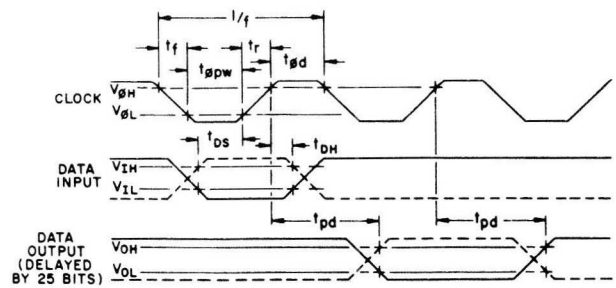
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SL-5-4025, SL-7-4025)
= -55°C to +125°C (SL-6-4025)
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	225	300	mW	SL-5-4025, SL-7-4025
	—	—	225	325	mW	SL-6-4025
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	1.0	MHz	
Pulse Width	$t_{\phi pw}$	450	350	—	ns	$t_f + t_{\phi pw} + t_r$ + $t_{\phi d} \geq 1$ μsec
Pulse Delay	$t_{\phi d}$	450	—	—	ns	
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	20	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	350	250	—	ns	
Hold Time	t_{DH}	10	0	—	ns	
Capacitance	C_I	—	8	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	250	350	ns	SL-5-4025, SL-7-4025
	t_{pd}	—	250	450	ns	SL-6-4025

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



SL-5-4032
SL-6-4032
SL-7-4032*

Quad 32-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SL-5 & SL-7: 0°C to +70°C
  SL-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

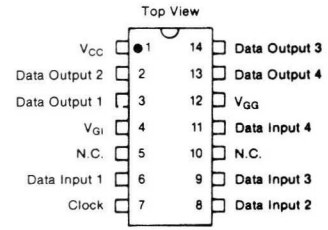
DESCRIPTION

The SL-5-4032, SL-6-4032 and SL-7-4032 are quad 32-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices each contain four independent common clock 32-bit DC to 1MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for all registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

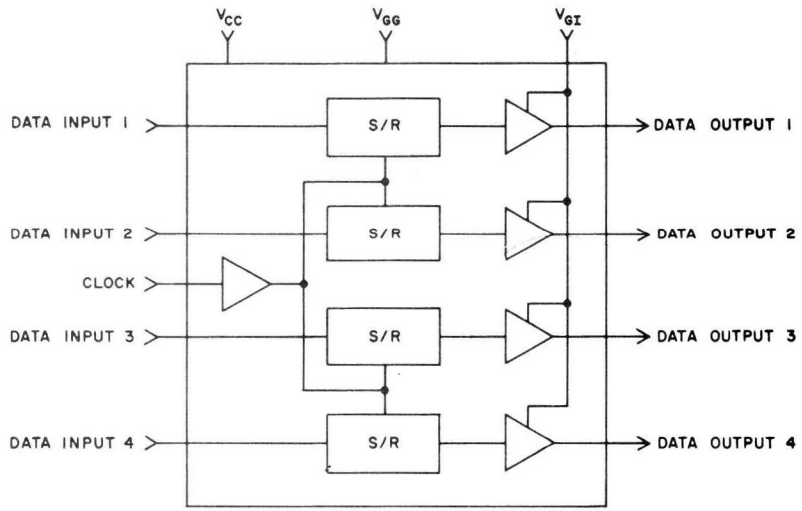
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATION

14 LEAD DUAL IN-LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature: SL-5-4032, SL-7-4032 ... 0°C to +70°C
SL-6-4032 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

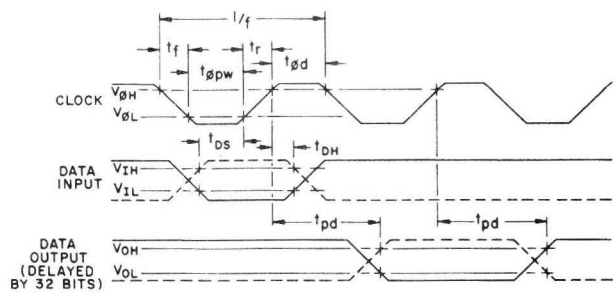
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SL-5-4032, SL-7-4032)
= -55°C to +125°C (SL-6-4032)
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	225	300	mW	SL-5-4032, SL-7-4032
	—	—	225	325	mW	SL-6-4032
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	1.0	MHz	
Pulse Width	$t_{\phi pw}$	450	350	—	ns	$t_f + t_{\phi pw} + t_r + t_{\phi d} \geq 1$ μsec
Pulse Delay	$t_{\phi d}$	450	—	—	ns	
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	20	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	350	250	—	ns	
Hold Time	t_{DH}	10	0	—	ns	
Capacitance	C_I	—	8	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	250	350	ns	SL-5-4032, SL-7-4032
	t_{pd}	—	250	450	ns	SL-6-4032

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



MEMORY

SS-5-8211
SS-6-8211
SS-7-2016*

Dual 16-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SS-5 & SS-7: 0°C to +70°C
  SS-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

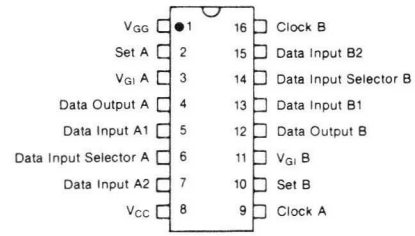
The SS-5-8211/SS-6-8211/SS-7-2016 are dual 16-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent 16-bit DC to 2MHz shift registers constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. Independent single phase clock inputs are provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition. Separate input data selector controls are provided on each shift register. They determine which of the two inputs shall be shifted into the register. Each shift register also has its own set input which forces all stages of the register to a "1" level.

*Available only in Europe (16 Lead Plastic DIP)

PIN CONFIGURATION

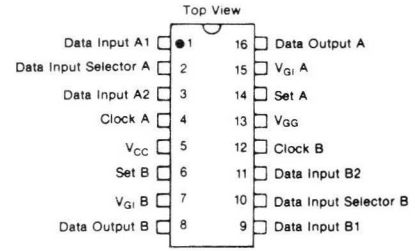
16 LEAD DUAL IN-LINE
SS-5-8211, SS-6-8211

Top View

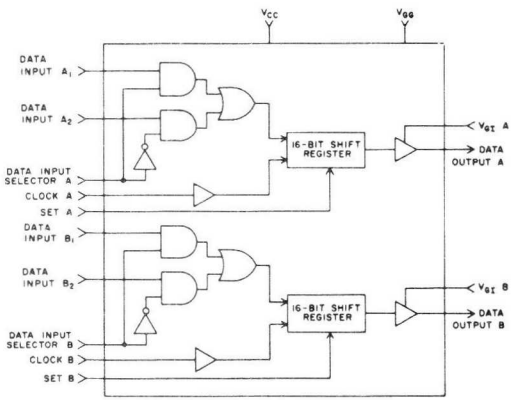


SS-7-2016*

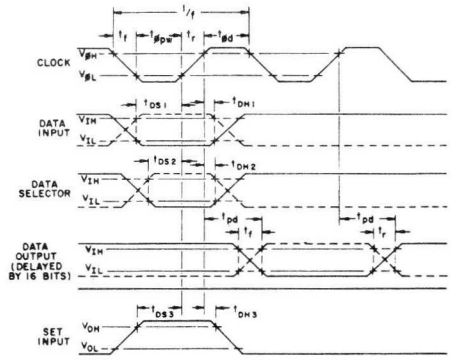
Top View



BLOCK DIAGRAM



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{GI} with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -20V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature Range: SS-5-8211, SS-7-2016.... 0°C to +70°C
SS-6-8211..... 55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} = Substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SS-5-8211, SS-7-2016)
= 55°C to +125°C (SS-6-8211)
One TTL load (C_L) total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	·10	μA	$V_{in} = V_{CC}$ -10V
Data Input, Data Selector, Set Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	125	160	mW	SS-5-8211, SS-7-2016
	—	—	125	200	mW	SS-6-8211
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	
Pulse Width	$t_{\phi pw}$	200	150	—	ns	$t_f + t_{\phi pw} + t_r + t_{\phi d} \geq 500$ns
Pulse Delay	$t_{\phi d}$	200	—	—	ns	
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	10	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DSI}	150	50	—	ns	
Hold Time	t_{DHI}	10	0	—	ns	
Capacitance	C_{inI}	—	5	—	pF	1MHz, T_A = +25°C
Data Selector						
Set Up Time	t_{DS2}	200	50	—	ns	
Hold Time	t_{DH2}	10	0	—	ns	
Capacitance	C_{in2}	—	5	—	pF	1MHz, T_A = +25°C
Set Input						
Set Up Time	t_{DS3}	400	—	—	ns	***
Hold Time	t_{DH3}	10	0	—	ns	
Capacitance	C_{in3}	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	180	250	ns	SS-5-8211, SS-7-2016
	t_{pd}	—	180	300	ns	SS-6-8211

**Typical values are at +25°C and nominal voltages.

***At least one clock cycle must occur during SET pulse (logic 1)

MEMORY

SS-5-8212
SS-6-8212
SS-7-8212*

Dual 16-Bit Static Shift Registers

FEATURES

- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-2MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SS-5 & SS-7: 0°C to +70°C
  SS-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

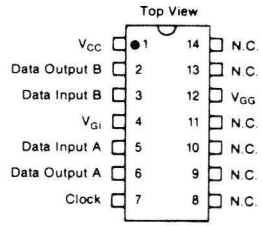
DESCRIPTION

The SS-5-8212, SS-6-8212 and SS-7-8212 are dual 16-bit static shift registers with clock and data inputs and outputs that interface directly with TTL/DTL logic arrays without the use of any special interface components. These devices contain two independent common clock 16-bit DC to 2MHz shift registers, constructed on a single monolithic chip utilizing MTNS P-Channel enhancement mode transistors. Each shift register bit is implemented with a cross coupled flip-flop, so that data is stored indefinitely regardless of the logic level of the clock. A single phase clock input is provided for both registers. Data on the input is sampled while the clock is at a "0" level and the register shifts on a "0" to "1" transition.

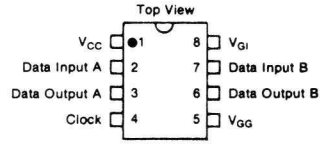
*Available only in Europe (14 Lead Plastic DIP)

PIN CONFIGURATIONS

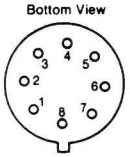
14 LEAD DUAL IN-LINE



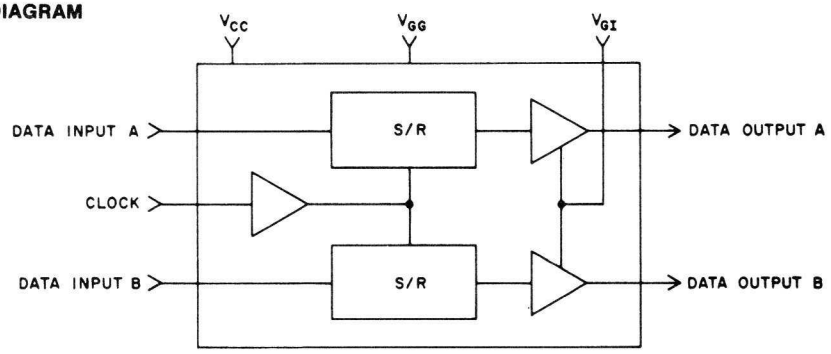
8 LEAD DUAL IN-LINE



8 LEAD TO-78



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_G with respect to V_{CC} ..... -20V to +0.3V
Clock and Data Inputs with respect to V_{CC} ..... -15V to +0.3V
Storage Temperature .....-65°C to +150°C
Operating Temperature: SS-5-8212, SS-7-8212 ... 0°C to +70°C
SS-6-8212 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

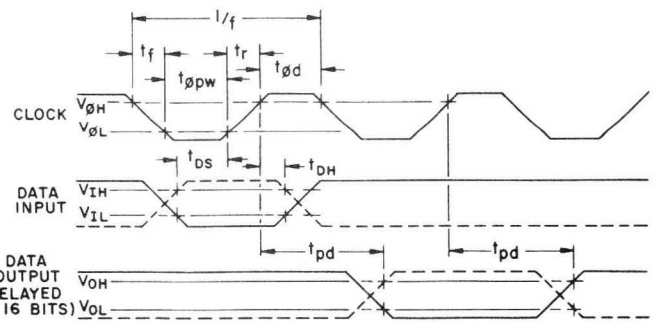
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} is the substrate voltage)
V_{GG} = -12 Volts ± 1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SS-5-8212, SS-7-8212)
= -55°C to +125°C (SS-6-8212)
One TTL load (C_L total = 10 pF)

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Input						
Logic 1 Level	$V_{\phi H}$	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	$V_{\phi L}$	—	—	+0.8	Volts	
Leakage	$I_{L\phi}$	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Input						
Logic 1 Level	V_{IH}	V_{CC}-1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$ -10V
Data Output						
Logic 1 Level	V_{OH}	V_{CC}-1.0	—	—	Volts	I_{OH} = 100 μA
Logic 0 Level	V_{OL}	—	—	+0.4	Volts	I_{OL} = 1.6mA
Power	—	—	125	160	mW	SL-5-8212, SL-7-8212
	—	—	125	200	mW	SL-6-8212
AC CHARACTERISTICS						
Clock Input						
Frequency	f	DC	—	2.0	MHz	
Pulse Width	$t_{\phi pw}$	200	150	—	ns	$t_f + t_{\phi pw} + t_r$
Pulse Delay	$t_{\phi d}$	200	—	—	ns	$+t_{\phi d} \geq 500$ns
Rise and Fall Times	t_r, t_f	—	—	1000	ns	
Capacitance	C_ϕ	—	15	—	pF	1MHz, T_A = +25°C
Data Input						
Set Up Time	t_{DS}	100	50	—	ns	
Hold Time	t_{DH}	10	0	—	ns	
Capacitance	C_I	—	5	—	pF	1MHz, T_A = +25°C
Data Output						
Propagation Delay	t_{pd}	—	150	225	ns	SL-5-8212, SL-7-8212
	t_{pd}	—	150	300	ns	SL-6-8212

**Typical values are at +25°C and nominal voltages.

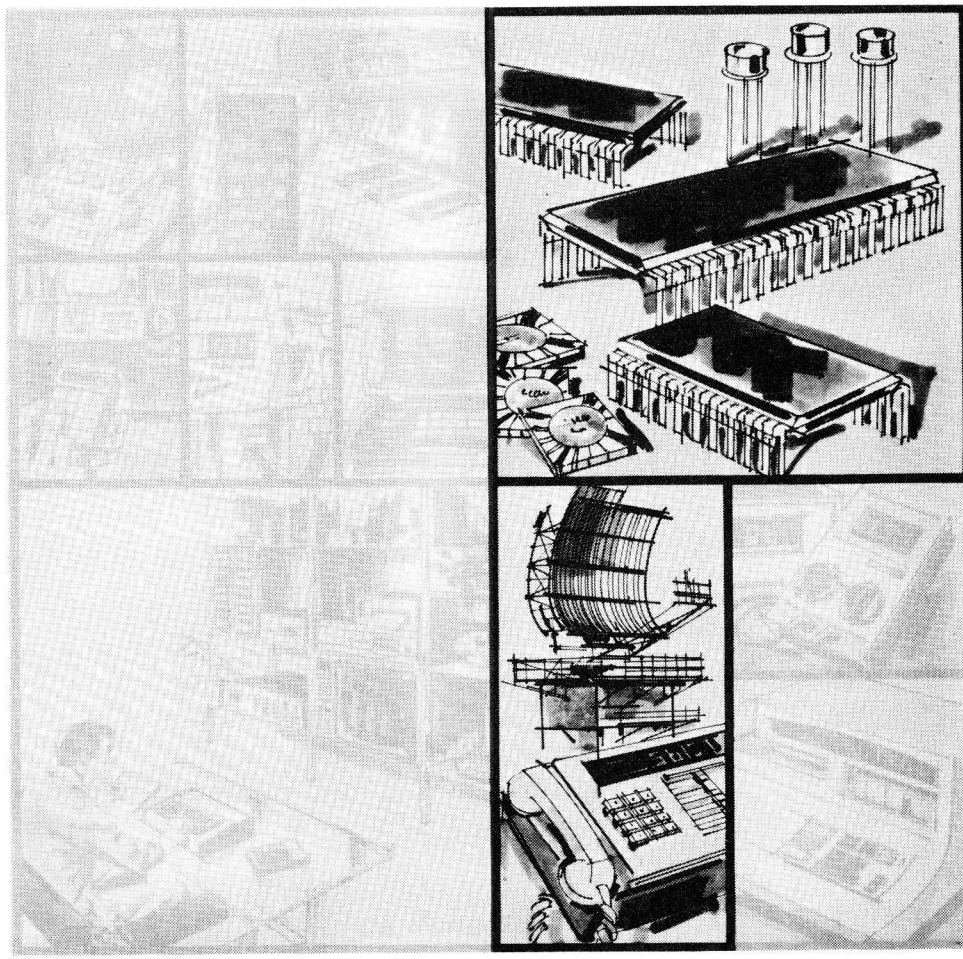
TIMING DIAGRAM



MEMORY

TELECOMMUNICATIONS 5

Telephony	5- 3
Telecom Hybrids	5-47
Data Communications	5-73



MICRO ELECTRONICS

TELEPHONY

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
5 CHANNEL RELAY DRIVER	Isolates +5V logic and exchange-powered relays.	AY-5-9050	5-4
PUSH BUTTON TELEPHONE DIALLERS	Converts push button input to rotary dial pulses.	AY-5-9100	5-7
		AY-5-9106	5-7
		AY-5-9110	5-7
		AY-5-9118	5-7
		AY-5-9120	5-7
		AY-5-9151/52	5-14
		AY-5-9153/54	5-14
		AY-9-9600	5-33
REPERTORY DIALLER	Stores ten 22 digit telephone numbers.	AY-5-9200	5-20
DUAL-TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	5-26
		AY-3-9401	5-26
		AY-3-9410	5-26
		AY-9-9086	5-6
CLOCK GENERATOR	Generates 2-phase clocks from a single power supply.	AY-5-9500	5-29
DUAL-TONE MULTI-FREQUENCY RECEIVERS	Detects and converts DTMF/tone telephone frequencies.	AY-5-9801/21	5-34
		AY-5-9802/22	5-34
		AY-5-9803/23	5-34
		AY-5-9804/24	5-34
		AY-5-9805/25	5-34
		AY-5-9806/26	5-34
		AY-5-9807/27	5-34
		AY-5-9808/28	5-34
CODEC	Duplex Delta-Sigma/PCM converter.	AY-3-9900	5-39
MICRO-COMPUTER DIALLER	A single-chip microcomputer pre-programmed for in-telephone applications.	TZ2001	5-45

Five Channel Relay Driver / High Voltage Interface

FEATURES

- Reference voltages generated and regulated on-chip from a single power supply
- High noise immunity
- High reliability and low cost using P-channel MTNS process (approved to BPO D4000)
- Defined output states under external fault conditions
- Provides isolation between +5V logic and exchange powered relays
- TTL compatible
- Supplies continuous load currents up to 250mA.

DESCRIPTION

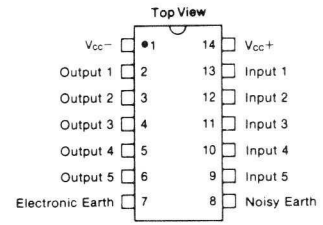
The circuit contains five individual channels, each comprising a logic section which switches a high current output driver. Delay circuitry is incorporated to improve rejection of noise interference on the inputs. The input logic levels are standard TTL compatible, and since only a very small input current is required a resistor of up to 10K may be connected in series to protect the preceding logic under fault conditions.

Each output driver is capable of supplying 50mA to a load connected directly to a nominal −48V exchange supply, and when higher currents and/or lower output voltages are required, channels may be paralleled externally to provide up to 250mA. Each driver operates as a buffer with a high impedance input and a high current output able to withstand large negative voltages in the OFF condition. In the ON condition, each output may be considered as a resistor of 40Ω maximum with a current rating of 50mA.

Isolation is provided between the logic circuitry and the exchange (noisy) earth. Although the exchange earth may fluctuate by ±4V, malfunction of the logic circuitry will not occur since the exchange earth is at −5V with respect to the logic supply.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



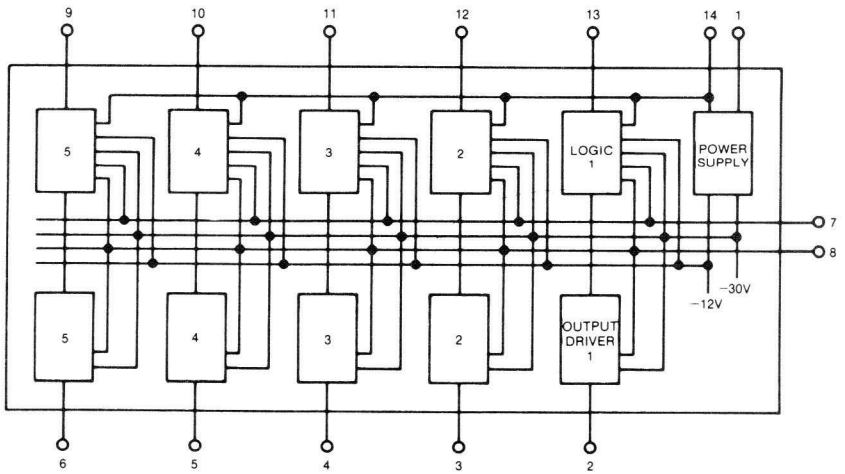
CIRCUIT FUNCTION

Input State	Output State
Logic '0'	On
Logic '1'	Off
Open Circuit	Off

CIRCUIT FUNCTION UNDER FAULT CONDITIONS

Fault Condition	Output State
V_{CC} + open circuit	Off
Electronic earth open circuit	Not defined
Noisy earth open circuit	Off

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Maximum continuous power dissipation 800mW
Maximum continuous supply voltage (V_{CC}+) ..... +7.0V
Minimum continuous supply voltage (V_{CC}+) ..... −0.3V
Maximum continuous supply voltage (V_{CC}−) Pin 8 = 0V ..... −60V
Maximum continuous positive input voltage Pin 7 = 0V ..... +7.0V
Maximum continuous negative input voltage Pin 7 = 0V ..... −12V
Maximum continuous positive output voltage Pin 8 = 0V ..... +4.0V
Maximum continuous negative output voltage (output off) ..... −65V
Maximum continuous negative output current per channel 60mA
Maximum continuous noisy earth voltage with respect to electronic earth ..... ±5.25V
Operating temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to 125°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

Positive supply (V_{CC}+) = +4.75V to +5.25V
Negative supply (V_{CC}−) = −44V to −52V
Noisy earth wrt 0V = ±4.0V
Ambient temperature = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Positive supply current (I_{CC}+)	—	0.9	4.5	mA	V_{CC}+ = 5.25V
Negative supply current (I_{CC}−)	—	—	4.5	mA	V_{CC}+ = 5.25V; V_{CC}− = −52V
Outputs Off					
Logic '1' Input voltage	2.4	—	V_{CC}+	Volts	
Logic '1' Input current	—	—	25	μA	V_{CC}+ = 5.25V; $V_{in} \geqslant$ 2.0; Pin 7 = 0V
Outputs On					
Logic '0' Input voltage	−12.0	—	0.4	Volts	
Logic '0' Input current	—	—	25	μA	V_{CC}+ = 5.25V; $V_{in} \leqslant$ 0.8V; Pin 7 = 0V
Output On Resistance (R_{ON})	—	25	40	Ω	V_{CC}+ = 4.75V; V_{CC}− = −44V; $I_{out} \leqslant$ 50mA; $V_{in} \leqslant$ 0.8V
On State Output Voltage	0.2	—	2.0	Volts	V_{CC}+ = 4.75V; I_{out} = 50mA; V_{in} = 0.8V; Pin 8 = 0V
Output Leakage Current (Off)	—	—	200	μA	V_{CC}+ = 4.75V; V_{out} = −60V; V_{in} = 2.0V; Pin 8 = 0V
Output Leakage Current (Off)	—	—	1.0	mA	V_{CC}+ = 4.75V; V_{out} = −65V; V_{in} = 2.0V; Pin 8 = 0V
Propagation Delay and Transition Time (T_{pon} + T_{on} and T_{poff} + T_{off})	—	50	300	μs	See Fig. 1

**Typical values are at +25°C and nominal voltages.

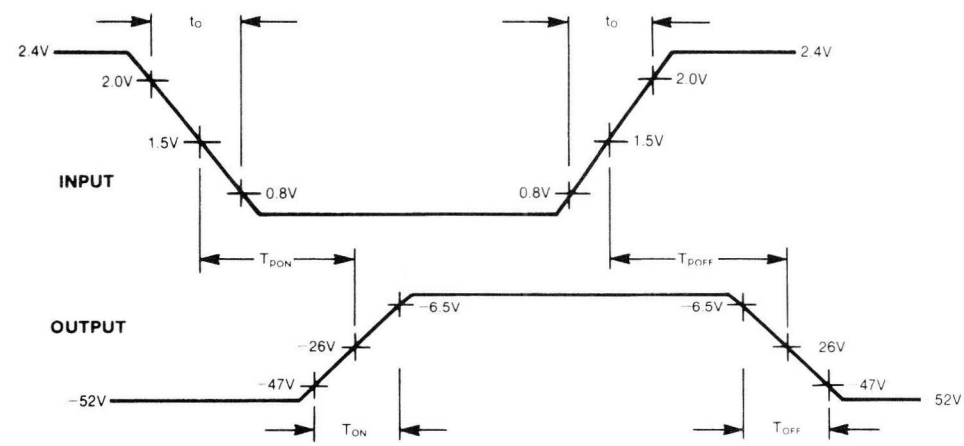


Fig.1 TRANSITION TIME

TELECOM

PRELIMINARY INFORMATION

Dual Tone Multi-Frequency Generator

FEATURES

- Low operating voltage (1.5V)
- High accuracy of the generated frequencies using 3.579545 MHz crystal
- Low output distortion
- Direct interface with keyboards or with buss oriented systems.

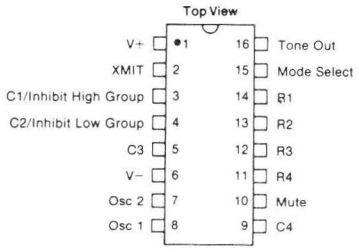
DESCRIPTION

The AY-9-9086 utilizes I^2L technology to provide a low power, low voltage, dual-tone multi-frequency generator intended for telephone applications where power is derived from the telephone lines and for microprocessor telecommunications applications using a fixed power supply.

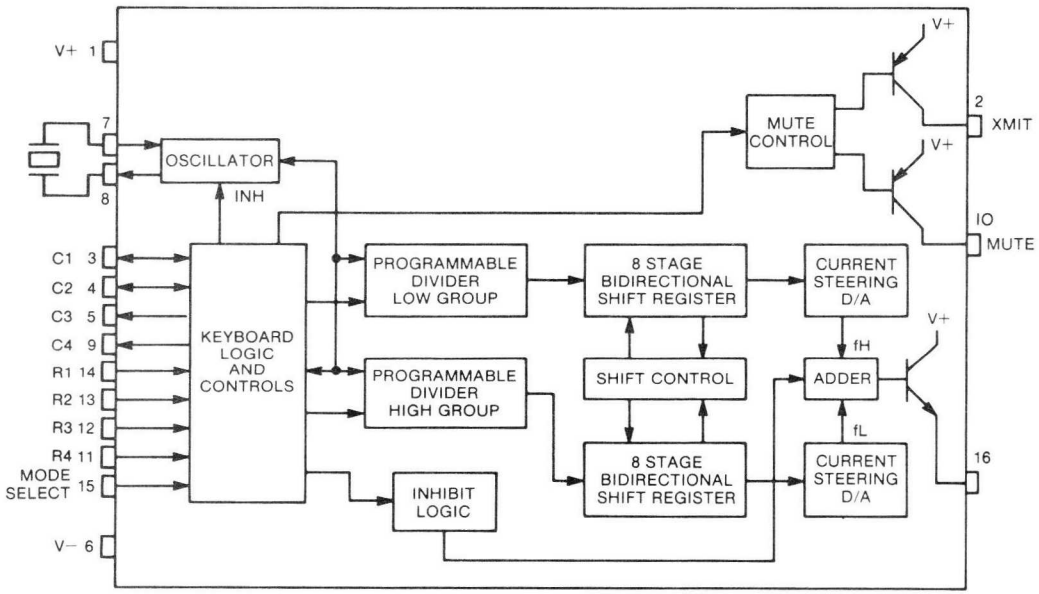
The AY-9-9086, when operating in the keyboard mode, can interface directly with a single closure 4×4 or 3×4 keyboard or with a matrix 4×4 keyboard. In the binary mode, the AY-9-9086 can operate as part of a buss-oriented system. The AY-9-9086 may also be mask-programmed to operate with a 1 of 10 or 1 of 12 keyboard—this version, however, would require a 22 pin package for the additional keyboard pins.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



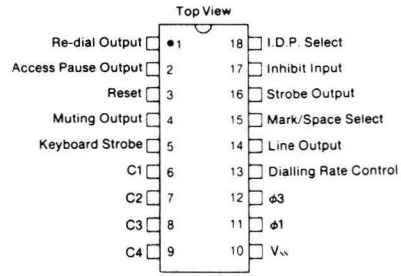
Push Button Telephone Diallers

FEATURES

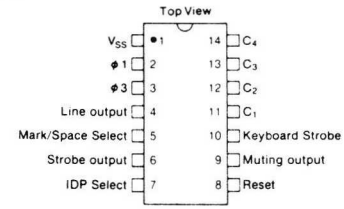
- 20 Digit Storage
- Selectable dialling rate
- Selectable mark/space ratio
- Selectable Inter-Digit Pause (except AY-5-9118)
- Dynamic circuitry — low power consumption
- Re-dial of last number (except AY-5-9118)
- Access Pause Facility (except AY-5-9118)
- Companion Repertory Dialler chip (AY-5-9200)

PIN CONFIGURATION

18 LEAD DUAL-IN-LINE
AY-5-9100/9106/9110/9120

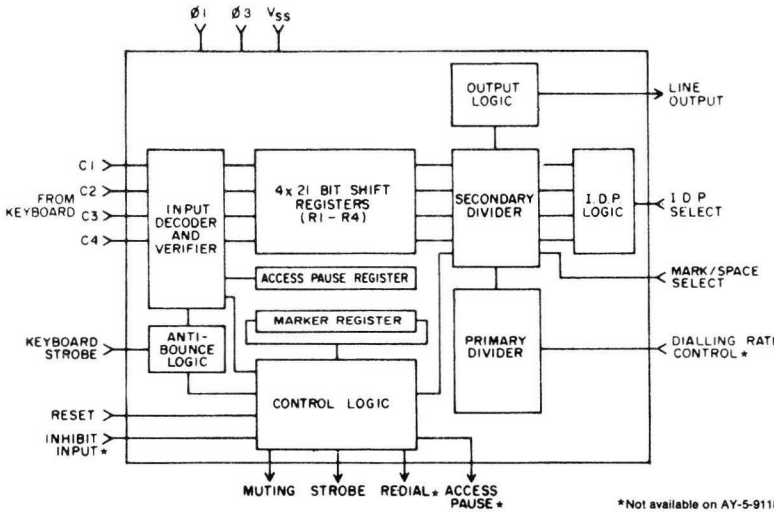


14 LEAD DUAL-IN-LINE
AY-5-9118



DESCRIPTION

The AY-5-9100 Series Push Button Dialler provides all of the logic required to convert a push button input to a series of pulses suitable for simulating a telephone dial. Pulse repetition rate, interdigital pause, and mark-space ratio are all programmable. Outputs are provided for line pulsing and muting. An "inhibit input" is provided to allow redial of one number of up to 20 digits. An "Access pause" capability is provided to allow automatic operation with a PBX or WATS line system. The low power consumption enables line-powered operation in a PBX or similar system. An AY-5-9100 Series circuit may be operated alone or in conjunction with the AY-5-9200 repertory dialler.



*Not available on AY-9118.

TELECOM

PIN FUNCTIONS

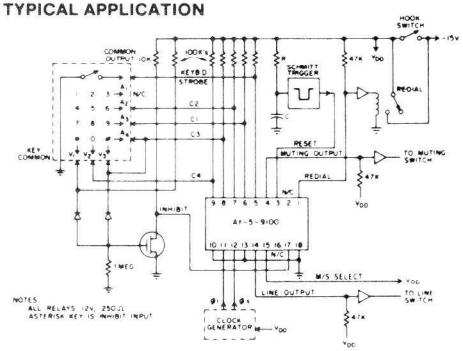
AY-5-9100 AY-5-9106 AY-5-9110 AY-5-9120 Pin No.	AY-5-9118 Pin No.	Name/Description
1	—	**Re-Dial Output** (except AY-5-9118): A logic "0" at this output indicates that redial mode has been selected.
2	—	**Access Pause Output** (except AY-5-9118): A logic "0" at this output indicates that an access pause is required.
3	8	**Reset:** A logic "0" on this input clears all shift registers and resets all counters. Reset should be applied after power on to clear the device.
4	9	**Muting Output:** The muting output goes to logic "0" whenever data is being entered or transmitted. It returns to logic "1" when the access pause output turns on and when transmission is complete.
5	10	**Keyboard Strobe:** This is the common signal from all the keys. A logic "0" on this input indicates that either the inhibit input or C1-C4 are to be read.
6-9	11-14	**C1-C4** (except no access pause on AY-5-9118): These are the keyboard data inputs. They are encoded as follows to allow simple interface with a standard push button (2-of-7) keyboard.

		AY-5-9100/9106 AY-5-9110/9118				AY-5-9120			
Digit	Impulses	C1	C2	C3	C4	C1	C2	C3	C4
1	1	1	1	1	1	1	1	1	0
2	2	1	1	1	0	1	1	0	1
3	3	1	1	0	1	1	1	0	0
4	4	1	0	1	1	1	0	1	1
5	5	1	0	1	0	1	0	1	0
6	6	1	0	0	1	1	0	0	1
7	7	0	1	1	1	1	0	0	0
8	8	0	1	1	0	0	1	1	1
9	9	0	1	0	1	0	1	1	0
0	10	1	1	0	0	0	1	0	1
Access Pause	—	0	0	1	1	0	1	0	0

10	1	**Vss**
11	2	**ϕ1**
12	3	**ϕ3**
13	—	**Dialling Rate Control** (Fixed at 10 p.p.s. on AY-5-9118) This input controls the line pulsing frequency as follows: (See Note 1):

Input	Line Pulse Rate
ϕ1	600 p.p.s.
ϕ3	20 p.p.s.
V_{SS}	10 p.p.s.

TYPICAL APPLICATION



AY-5-9100 AY-5-9106 AY-5-9110 AY-5-9120 Pin No.	AY-5-9118 Pin No.	Name/Description
14	4	**Line Output** A logic "0" on this output is a line pulse "mark" or "break."
15	5	**Mark/Space Select** The mark to space ratio is controlled by this input as follows:

Input	Mark	Space
ϕ1	70	30
ϕ3	50	50
Logic 0	66 2/3	33 1/3
Logic 1	60	40

These ratios are exact and do not depend on clock frequency.

16	6	**Strobe Output** This output goes to logic "0" to indicate that a digit is being out-pulsed.
17	—	**Inhibit Input** (except AY-5-9118) The inhibit input is used to inhibit out-pulsing and to place the device in re-dial mode. The keyboard strobe must be taken to logic "0" at any time the inhibit input is strobed, except when an Access Pause is being signalled. This input normally operates as a "toggle flip-flop". If it is taken to a logic "1" any time other than when an access pause is being signalled, the circuit will lock into the redial mode and the redial output will go to logic "0". The chip will remain in the re-dial mode until this input is taken to logic "1" again. If the chip is cleared before inhibit is toggled, digits entered are accepted, but out-pulsing does not commence until the inhibit is re-strobed. If a number is being outpulsed when the inhibit is strobed, dialling ceases until the inhibit is re-strobed. If the inhibit is strobed when a dialling sequence is completed, the redial output goes to logic "0" and the number is stored. Re-strobing the inhibit starts the dialing sequence. When an access pause is signalled, this input no longer operates as a toggle, but rather as a gate, with a logic "1" inhibiting further out-pulsing.
18	7	**I.D.P. Select** This input controls the inter-digital-pause as follows: (See Note 1):

Input	IDP: AY-5-9100/9106/9120		
	10p.p.s.	20p.p.s.	600p.p.s.
ϕ3	400ms	200ms	6.66ms
V_{SS}	800ms	400ms	13.33ms
ϕ1	1000ms	500ms	18.33

Input	IDP: AY-5-9110			IDP: AY-5-9118
	10p.p.s	20p.p.s.	600p.p.s.	10p.p.s.
ϕ3	700ms	350ms	11.66ms	700ms
V_{SS}	900ms	450ms	15ms	900ms
ϕ1	800ms	400ms	13.33ms	800ms

A pre-digital pause equal in length to the inter-digital pause precedes the first digit of any number.

NOTE 1: Line Pulse Frequency and Inter-Digital Pause are specified with an 18KHz clock frequency.

OPERATION

The 4 bit code from the keyboard arrives on inputs C1-C4 of the Push Button Dialler. A fifth input from the keyboard, the Keyboard Strobe, is also required. In its quiescent state the five inputs are at logic 1 (−volts). A logic 0 on the Keyboard Strobe input indicates to the input circuitry that it is to read the data on C1-C4, thus allowing 1111 as an allowable code from the keyboard.

When a digit key is depressed the logic detects the 1-0 transition on the Keyboard Strobe input. When this occurs a timer with a minimum count time of 4.2 msec. is started. If the common input is removed before this period has elapsed, the counter will be reset to its starting state. If the Keyboard Strobe input is stable for at least 8.7 msec. the code is fed to the code verifier and converter.

If the code is invalid, it is ignored. If valid it is converted to the proper BCD code and written into recirculating shift registers R1-R4. If an access pause is decoded, it is written into the access pause register.

Simultaneous with the data being written into R1-R4, the muting output goes to logic "0", to disconnect the transmission circuitry. When all digits that have been keyed into the circuit have been dialled out the muting output returns to logic "1".

During dialling if an access pause is required, the muting output will reconnect the transmission circuitry so that the caller can listen for the dial tone and ensure himself that the system is functioning correctly.

The digit store has a capacity of 20 digits. The numbers are read non destructively allowing redial.

Four 21 bit registers hold the number in BCD format; the number is stored in parallel. A fifth register holds a marker bit (Signified as A) showing the first number entered. This fifth register has a gated 22nd bit allowing the marker bit (A) to be 'slipped' backwards one bit with respect to the number. Gating ensures that all numbers are sequentially entered, the first aligning itself with the marker A. When the first number is to be loaded into the counter, A is decoded in its 21st position and the parallel enable signal reads the first digit into the counter. Gating is enabled to allow A to be shifted through the 22nd bit of the marker store, so aligning itself with the next number to be dialled out. When A is decoded at the 21st bit and no number is in the stored digit register, A remains aligned in this state until 'redial' is depressed and the marker store goes into its 22nd bit mode until A aligns with the first digit.

Gating ensures that only 20 digits are entered into R1-4. One empty state at least is required to indicate to the system that a number is complete.

TIMING DIAGRAMS (L = Low = Logic "1"; H = High = Logic "0")

Fig.1 Clock Waveforms

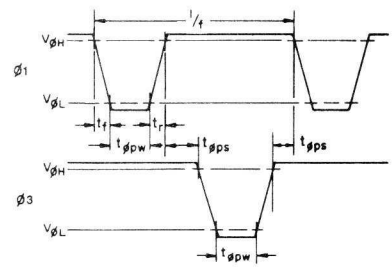


Fig.2 Reset and Keyboard Strobe Timing

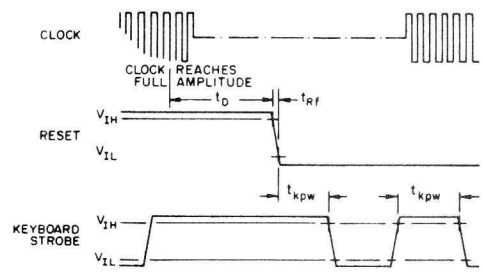


Fig.3 Line, Muting and Strobe Output Timing

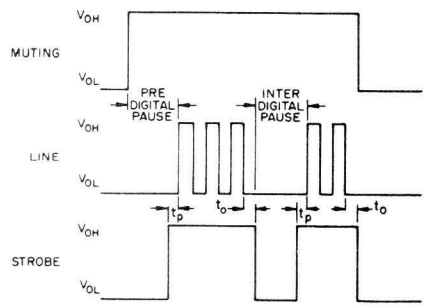
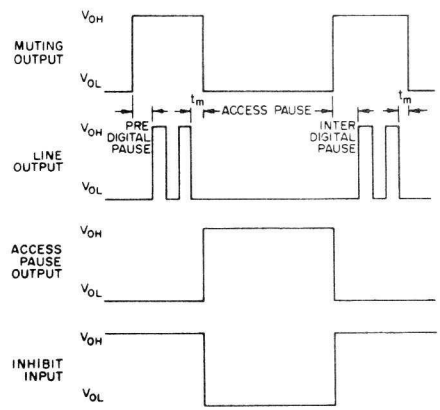


Fig.4 Line, Muting and Access Pause Output Timing



TELECOM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS}) . . . . . −20V to +0.3V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

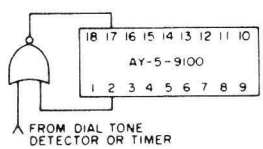
Standard Conditions (unless otherwise noted)
V_{SS} = 0V T_A = −25°C to +70°C
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	$V\phi_1$	−13.5	—	−16.5	V	
Logic '0'	$V\phi_H$	+0.3	—	−1.0	V	Match clocks within 0.5V
Frequency	f	10	18	30	kHz	See Note 2
Capacitance	$C\phi$	—	90	150	pF	Each clock input, $V\phi$ = OV, f = 1MHz
Rise Time	t_r	.1	—	8	μs	
Fall Time	t_f	.1	—	4	μs	
Leakage	$I_L\phi$	—	—	30	μA	$V\phi$ = −16.5, T_A = +80°C
Pulse Width	$t\phi_{PW}$	5	—	40	μs	
Pulse Separation	$t\phi_{PS}$	5	—	40	μs	
All Outputs (Note 3)						
On Resistance (Logic '0')	R_{ON}	—	—	1	kΩ	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LL}	—	—	10	μA	V_{OL} = −10V, T_A = 25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_p	—	—	3	ms	
Line-Strobe Delay	t_o	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay	t_m	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	V_I = −16.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	—	5	pF	V_I = OV, F = 1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width	t_{KPW}	10	—	—	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	Vin = −16.5, T_A = 25°C
Capacitance	C_I	—	—	5	pF	Vin = 0V, f = 1MHz
Fall Time	t_{Rf}	3	—	100	μs	
Delay Time	t_D	3	—	—	ms	After clocks reach full amplitude
Power	—	—	0.9	2	mW	$V\phi$ = 16.5V

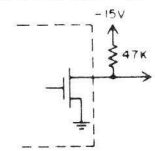
** Typical values are at +25°C and nominal voltages.

NOTES: 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18kHz.
3. Outputs require external pull-down resistors (47K typical).

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS}) . . . . . −20V to +0.3V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

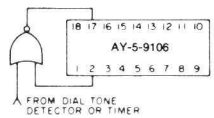
Standard Conditions (unless otherwise noted)
V_{SS} = 0V T_A = +25°C.
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	$V\phi_L$	-4.0	—	-8.5	V	
Logic '0'	$V\phi_H$	+0.3	—	-0.2	V	Match clocks within 0.05V
Frequency	f	8	9	20	kHz	See Note 2
Capacitance	$C\phi$	—	90	120	pF	Each clock input, $V\phi$ = OV, f = 1MHz
Rise Time	t_r	.1	—	8	μs	
Fall Time	t_f	.1	—	4	μs	
Leakage	$I_L\phi$	—	—	10	μA	$V\phi$ = -8.5V, T_A = +80°C
Pulse Width	$t\phi_{PW}$	5	—	40	μs	
Pulse Separation	$t\phi_{PS}$	5	—	40	μs	
All Outputs (Note 3)						
Output Current (Logic '0')	I_{OH}	0.1	—	—	mA	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LL}	—	—	10	μA	V_{OL} = -8.5V T_A = 25°C
Line Output (See Fig. 3)						
Strobe-Line Delay (Note 4)	t_p	—	—	6	ms	
Line-Strobe Delay (Note 4)	t_o	66	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay (Note 4)	t_m	66	— Ω	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IL}	-2.0	—	-8.5	V	
Logic '0'	V_{IH}	+0.3	—	-0.2	V	
Leakage	I_{LI}	—	—	1	μA	V_I = -8.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	—	5	pF	V_I = OV, F = 1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width (Note 4)	t_{KPW}	20	—	—	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IL}	-2.0	—	-8.5	V	
Logic '0'	V_{IH}	+0.3	—	-0.2	V	
Leakage	I_{LI}	—	—	1	μA	Vin = -8.5, T_A = 25°C
Capacitance	C_I	—	—	5	pF	Vin = 0V, f = 1MHz
Fall Time	t_{Rf}	—	—	100	μs	
Delay Time (Note 4)	t_D	6	—	—	ms	After clocks reach full amplitude
Power	—	—	0.12	—	mW	$V\phi$ = 8.5V, f = 9kHz
	—	—	0.24	—	mW	$V\phi$ = 8.5V, f = 18kHz

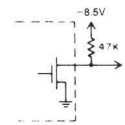
** Typical values are at +25°C and nominal voltages.

NOTES: 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 9kHz
3. Outputs require external pull-down resistors (47K typical).
4. These times will be halved for 18kHz operation.

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE



TELECOM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS}) . . . . . −20V to +0.3V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

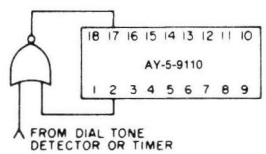
V_{SS} = 0V T_A = +25°C
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	$V\phi_L$	−13.5	−15	−16.5	V	
Logic '0'	$V\phi_H$	+0.3	—	−1.0	V	Match clocks within 0.5V
Frequency	f	10	18	30	kHz	See Note 2
Capacitance	$C\phi$	—	90	150	pF	Each clock input, $V\phi$ = OV, f = 1MHz
Rise Time	t_r	.1	—	8	μs	
Fall Time	t_f	.1	—	4	μs	
Leakage	$I_L\phi$	—	—	30	μA	$V\phi$ = −16.5, T_A = +80°C
Pulse Width	$t\phi_{PW}$	5	—	40	μs	
Pulse Separation	$t\phi_{PS}$	5	—	40	μs	
All Outputs (Note 3)						
Output Current (Logic '0')	I_{OH}	0.25	—	—	mA	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LL}	—	—	10	μA	V_{OL} = −10V. T_A = 25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_p	—	—	3	ms	
Line-Strobe Delay	t_o	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay	t_m	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	V_I = −16.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	—	5	pF	V_I = OV, F = 1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width	t_{KPW}	10	—	—	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−0.5	V	
Leakage	I_{LI}	—	—	1	μA	Vin = −16.5, T_A = 25°C
Capacitance	C_I	—	—	5	pF	Vin = 0V, f = 1MHz
Fall Time	t_{Rf}	3	—	100	μs	
Delay Time	t_D	3	—	—	ms	After clocks reach full amplitude
Power	—	—	0.7	2	mW	$V\phi$ = 16.5V

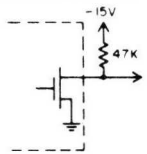
** Typical values are at +25°C and nominal voltages.

NOTES: 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18kHz.
3. Outputs require external pull-down resistors (47K typical).

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE



SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS}) . . . . . −20V to +0.3V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

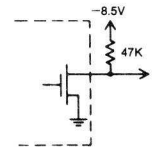
V_{SS} = 0V T_A = −25°C to +70°C
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	$V\phi_L$	-3.8	—	-8.5	V	
Logic '0'	$V\phi_H$	+0.3	—	-0.2	V	Match clocks within 0.05V
Frequency	f	15	18	21	kHz	See Note 2
Capacitance	$C\phi$	—	90	150	pF	Each clock input, $V\phi$ = OV, f = 1MHz
Rise Time	t_r	.1	—	8	μs	
Fall Time	t_f	.1	—	4	μs	
Leakage	$I_L\phi$	—	—	10	μA	$V\phi$ = -8.5, T_A = +80°C
Pulse Width	$t\phi_{PW}$	10	—	40	μs	
Pulse Separation	$t\phi_{PS}$	5	—	40	μs	
All Outputs (Note 3)						
Output Current (Logic '0')	I_{OH}	0.1	—	—	mA	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LL}	—	—	10	μA	V_{OL} = -8.5 T_A = 25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_p	—	—	3	ms	
Line-Strobe Delay	t_o	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay	t_m	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IL}	-2.0	—	-8.5	V	
Logic '0'	V_{IH}	+0.3	—	-0.2	V	
Leakage	I_{LI}	—	—	1	μA	V_I = −8.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	—	5	pF	V_I = OV, F = 1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width	t_{KPW}	10	—	—	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IL}	-2.0	—	-8.5	V	
Logic '0'	V_{IH}	+0.3	—	-0.2	V	
Leakage	I_{LI}	—	—	1	μA	Vin = -8.5V, T_A = 25°C
Capacitance	C_I	—	—	5	pF	Vin = 0V, f = 1MHz
Fall Time	t_{Rf}	3	—	100	μs	
Delay Time	t_D	3	—	—	ms	After clocks reach full amplitude
Power	—	—	0.24	—	mW	$V\phi$ = 8.5V

** Typical values are at +25°C and nominal voltages.

NOTES: 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18 kHz.
3. Outputs require external pull-down resistors (47K typical).

TYPICAL OUTPUT INTERFACE



TELECOM

PRELIMINARY INFORMATION

Push Button Telephone Diallers

FEATURES: AY-5-9151

- 2.5V to 5V and 200μA operation, plus standby mode
- Frequency of on-chip clock set by external RC network
- Selectable break: make ratio and interdigital pause
- Uses 3 × 4 matrix keyboard with no keyboard ground or common contact
- Keyboard inputs have antibounce protection
- Input pull-up or pull-down resistors on-chip
- Data entry inhibited and error signal produced if more than one key is pressed
- Redial and access pause controlled from keyboard
- 22 digit capacity including access pauses
- Dialler reset for line power breaks>200ms.

FEATURES: AY-5-9152. Same as AY-5-9151 except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

FEATURES: AY-5-9153. Same as AY-5-9151 when in 3 × 4 matrix keyboard mode plus:

- Pin selectable options of 1 of 12 keyboard, 2 of 7 keyboard with common and 4 bit binary with common
- Repertory dialler capability when used with AY-5-9200
- 8 bit output for displaying number in digit store
- Simple call-barring facility using display outputs

FEATURES: AY-5-9154. Same as AY-5-9153 except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

DESCRIPTION

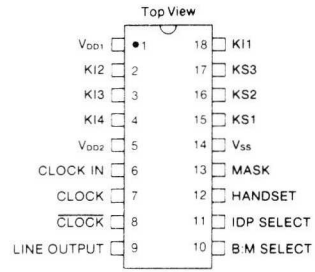
This range of CMOS Pushbutton diallers consists of four devices AY-5-9151 to AY-5-9154, all of which perform the function of converting input data (e.g. from a keyboard) into a series of pulses suitable for loop disconnect dialling. The series is based on two devices: a simple, basic dialler circuit and a more complex and versatile device which accepts a variety of data entry codes and has a display facility.

The use of CMOS technology results in low voltage and current requirements, enabling easy interfacing with a variety of telephones. The versatility of the devices and the low external component count enables the building of sophisticated, reliable telephones at low cost.

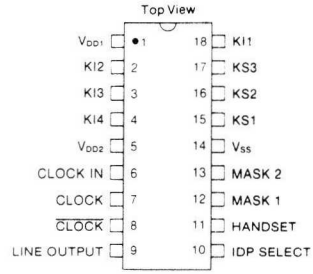
PIN CONFIGURATIONS

18 LEAD DUAL IN LINE

AY-5-9151



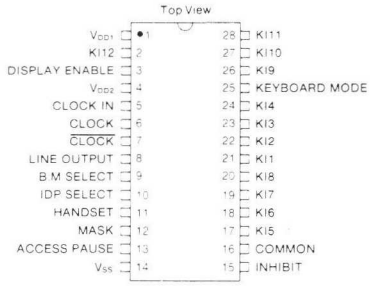
AY-5-9152



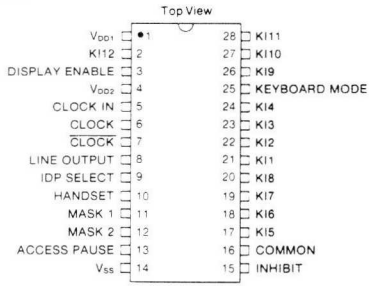
PIN CONFIGURATIONS

28 LEAD DUAL IN LINE

AY-5-9153



AY-5-9154



PIN FUNCTIONS

V_{SS} - The negative supply to the device. All voltages are referenced to this pin.

V_{DD1} - The positive supply to the digit store and write counter. Power must be maintained on this pin if the redial function is used.

V_{DD2} - The positive supply to the clock generator and control logic. V_{DD2} should rise to 2.5V withing 20 ms of switch-on.

Clock In, $\overline{\text{Clock}}$, Clock - These pins are connected to an external RC network which controls the frequency of the clock generator and hence the timing of the line and mask outputs.

Handset Input - The state of the handset is used to control this input, a logic 1 on the input indicating that the handset is on-hook and a logic 0 indicating that the handset is off-hook. This input is used to reset the control logic depending on the past history of the input.

If the input is taken from logic 1 to logic 0, and the clock is not oscillating, a reset pulse is produced when clock pulses are detected. The device is then ready for operation.

If the input is taken to logic 1 for less than 200ms and the clock generator is operating throughout this period, a reset pulse is not produced when the input is taken back to logic 0. Thus short breaks in line power will not affect the operation of the circuit.

If the input is taken to logic 1 for more than 200ms, and clock pulses are present throughout this period, a reset pulse will be generated at the end of the 200ms period.

Line Output - The loop disconnect dial pulses appear at this output. It is an open drain output with the source of the output transistor being connected to V_{SS}. A break period corresponds to this transistor being switched on and a make period or IDP corresponds to the transistor being switched off. The first digit of any outdialling sequence is preceded by a pre-digit pause equal in length to an interdigital pause.

Mask Output/Mask 1 Output - This is a push-pull output and is used to mute the telephone speech circuit. A logic 1 indicates that the speech circuit is to be muted, this occurring immediately on recognition of an input from the keypad.

Mask 2 Output - The AY-5-9152 and AY-5-9154 are fixed at 60:40 Break:Make ratio and a Mask 2 output is substituted for the Break:Make input. The mask 2 output is identical to the mask 1 but is driven in antiphase to enable a bistable mask relay to be used.

On initial application of power, a pulse is produced on Mask 1 and Mask 2 outputs to reset a bistable relay which may be connected to these outputs.

IDP Input - This pin is used to select the duration of the interdigital pause. With a clock frequency of 18kHz, interdigital pauses of 700, 800 or 900ms may be selected. A further option for test purposes enables the IDP to be fixed at 13.3ms and the impulsing rate to be fixed at 600 impulses per second.

Break:Make Ratio - A choice of four break:make ratio is available as a pin programmable option, 70:30, 66:33, 60:40 and 50:50.

Display Enable - When display data is being output from the dialler, this output goes to a logic 1.

Common Input - When a 4 bit code is used for data input a logic 1 on this input strobes the data into the device. Antibounce protection is provided for this input. A steady logic 1 of less than 5ms duration will not be recognized and a steady logic 1 of greater than 10ms duration will be recognized. This input has a pull down resistor to V_{SS}.

Inhibit Input - This is used to inhibit outdialling. If a logic 1 is placed on this input while a digit is being dialled, outdialling will cease when the digit has been completed. If the logic 1 appears during an IDP, outdialling will cease immediately. When outdialling has ceased, the Mask/Mask 1 output goes to logic 0 and Mask 2 goes to logic 1. When the input is taken to logic 0, the Mask signal reappears and dialling continues, starting with an IDP.

Access Pause Output - When an access pause is reached in the dialling sequence, this output goes to a logic 1. By connecting this to the inhibit input, further outdialling will be prevented.

Keyboard Mode - The data on this pin determines whether the device will accept data from:

a) 1 of 12 keyboard with keyboard ground
b) 2 of 7 keyboard with keyboard ground and common switch
c) 4 bit binary code with common signal
d) 4 + 3 matrix keyboard without keyboard ground and common switch

When modes b, c or d are in use with the AY-5-9153 or AY-5-9154 data in the form of two, four-bit words is available for display purposes, except when a key is pressed.

Keyboard Inputs/Keyboard Scans/Display Outputs 1 of 12 Mode - All twelve pins are used as keyboard inputs, on-chip pull-up resistors to logic 1 being incorporated. A logical AND of the twelve inputs produces an on-chip Any Key Down signal when any input is taken to logic 0. Detection of this signal initiates an anti-bounce period and at the end of this period, the data on the twelve inputs is read into the digit store, provided the Any Key Down signal is present throughout this period. Any further data is then inhibited until an antibounce period has been completed with all keys up. If, during the anti-bounce period, the Any Key Down signal disappears, the anti-bounce timer will be reset.

2 of 7 Mode - Keyboard inputs 1-4 are used for the 4-bit data, the common input strobing the data into the digit store. On-chip pull down resistors to logic 0 are incorporated on the four data inputs and the common input. When the common input is taken to logic 1, an antibounce timer is started and if the common input is at logic 1 throughout, the data is read at the end of the period. Further data is then inhibited until the common input has been at logic 0 for an antibounce period.

Binary Mode - The 4-bit word is entered into the digit store via inputs 1-4 by use of the common input, in a similar manner to the 2 of 7 mode. On-chip pull down resistors to logic 0 are incorporated. When data is not being read into the device (i.e. when the common input is at logic 0) these four inputs are used as output pins for a 4-bit word for digit display purposes as described later.

4 × 3 Matrix Mode - This function will be described for the AY-5-9151 and AY-5-9152. The mode of operation is slightly different for the AY-5-9153 and AY-5-9154, as explained later.

A pulse to logic 0 is sequentially switched around the three keyboard scan outputs, taking 5ms for a complete scan cycle. When a key is pressed the pulse appears on one of the four keyboard inputs 1-4 (provided with pull-up resistors to logic 1), and if it occurs on the same input on the next scan cycle, the data is entered into the digit store. Before a second key depression may be recognized, the first key must be released and a full scan cycle completed without a pulse on any input.

If two keys are pressed during the same scan cycle, the data will be rejected and again a full scan cycle must be completed without a pulse appearing on any of the inputs before another key depression may be recognized.

If a key is pressed during an inhibited period, or two keya are pressed simultaneously, all three scan outputs will go to logic 0 until the key or keys is/are released.

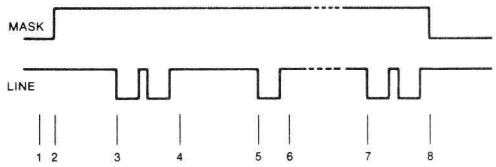
Display Scans/Display Outputs - Data for the first 16 digits and access pauses in the store is available for display.

The position of a digit within a telephone number is indicated by a 4 bit binary word from the Display Scan outputs. Display Scan 1 is the least significant bit and Display Scan 4 is the most significant bit. Binary word 0000 corresponds to the left-hand digit of the display (the first number entered) and 1111 corresponds to the right-hand (16th) digit of the display.

The digit being output is available as a 4 bit word on the display outputs (Display Out 1 = least significant bit). Binary word 0001 represents digit 1 and so on to 0000 = digit 10. Access pauses are represented by 1011.

When in the 2 of 7 mode or the Binary mode, the display data is inhibited by the appearance of the common signal. When in the 4 × 3 matrix mode, depression of a key causes display scan data to appear on the keyboard inputs. The dialler then reverts to the normal keyboard scanning mode of operation.

LINE AND MASK OUTPUT TIMING



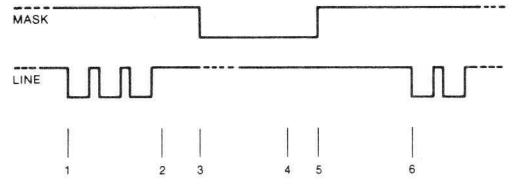
The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 18kHz. The time intervals are inversely proportional to the clock frequency.

	Event	Time Interval
1	The first key is depressed and the anti-bounce timer is started	T_{1-2} = 5-10ms after end of bounce
2	The data from the keyboard is accepted. The mask output appears and the pre-digital pause commences. This is the same duration as the inter-digital pause and is pin selectable.	T_{2-3} = 700, 800 or 900ms
3	Dialling of the first digit starts. The example shown is a digit 2.	$T_{3-4} = n \times 100$ms where n = digit dialled
4	End of 1st digit and start of inter-digital pause.	T_{4-5} = 700, 800 or 900ms
5	Dialling of 2nd digit starts. The example shown is a digit 1.	$T_{5-6} = n \times 100$ms where n = digit dialled
6	End of 2nd digit and start of inter-digital pause.	T_{6-7} = 700, 800 or 900ms

Dialling of further digits continues in a similar manner until the last digit.

7	Dialling of last digit commences, in this case a digit 2.	$T_{7-8} = n \times 100$ms where n = digit dialled
8	End of last digit and end of mask signal.	

EFFECT OF ACCESS PAUSE ON LINE AND MASK OUTPUT TIMINGS



The following time intervals are valid only for a clock frequency of 18kHz.

	Event	Time Interval
1	Dialling of the last digit before the access pause commences. A digit 3 is shown in this example.	$T_{1-2} = n \times 100$ms where n = digit dialled.
2	The end of the last digit before the access pause.	T_{2-3} = 700, 800 or 900ms
3	The mask signal is removed so that the telephone user can listen for the appearance of the second dial tone.	
4	The telephone user presses the # key to release the access pause. The antibounce timer is started.	T_{4-5} = 5-10ms
5	The data from the # key is accepted or the inhibit input is taken to logic 0 and the mask signal reappears. A pre-digital pause equal in length to an inter-digital pause starts.	T_{5-6} = 700, 800 or 900ms
6	The digit after the access pause is dialled out. Dialling then continues as normal.	

Access Pause and Redial Operation

These facilities are available on all devices, control being via the keypad or data input codes. The 1 of 12 keypad and 4 × 3 keypad use the '*' button to insert an access pause and the '#' button to release the access pause.

The '#' button may also be used to redial the number in the digit store. If the redial mode is used, power must be maintained on V_{DD1} at all times.

PIN SELECTABLE OPTIONS

a) Break:Make Ratio

Ratio	Voltage On Pin
70:30	Clock
66:33	V_{DD}
60:40	V_{SS}
50:50	$\overline{\text{Clock}}$

b) IDP (with 18kHz clock frequency)

IDP	Voltage On Pin
700ms	V_{DD}
800ms	V_{SS}
900ms	Clock
13.3ms	$\overline{\text{Clock}}$

c) Keyboard Mode

Mode	Voltage On Pin
2 of 7	V_{DD}
3 × 4	V_{SS}
1 of 12	Clock
Binary	$\overline{\text{Clock}}$

DATA INPUT CODES

KI = Keyboard Input

Binary

KI 4	KI 3	KI 2	KI 1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	Access Pause
1	1	0	0	Redial

2 of 7

KI 1	KI 2	KI 3	KI 4	Digit
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	7
1	0	0	1	8
1	0	1	0	9
0	0	1	1	10
1	1	0	0	Access Pause
1	1	0	1	Redial

4-bit codes other than those shown above are ignored.

DATA OUTPUT CODES

Display Scan (DS)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DS4	DS3	DS2	DS1	Position
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

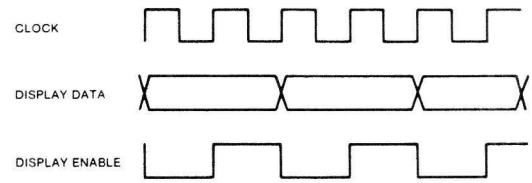
Display Outputs (DO)

DO4	DO3	DO2	DO1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	0
1	0	1	1	Access Pause

The Display Scan outputs are continuously incremented, and the Display outputs changed accordingly, to enable the display of all the digits in the digit store by the use of multiplexing.

The Display Scan code is incremented at half the clock frequency.

The relationship between Clock, Display Data out and Display enable is as follows.



TELECOM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +7.0V to −0.3V
Storage temperture range ..... −65°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
$V_{DD1} = V_{DD2}$ = 2.5 V to 5.0V ($V_{DD1} \geq V_{DD2}$)
T_A = −25°C to +80°C

Clock frequency = 18kHz The device will finction correctly from 8kHz to 50kHz but all timings (break period, IDP etc.,) willbe directly dependent on the clock period.

Characteristic	Min.	Typ.	Max.	Units	Conditions
INPUTS					
Logic '0' Level	−0.3	0	0.5	V	Note 1
Logic '1' Level	V_{DD} −0.5	V_{DD}	V_{DD} +0.3	V	
Capacitance	—	—	10	pF	$V_{IN} = V_{SS}$, f = 1MHz
CURRENT SOURCE TO V_{DD}					
Keyboard Inputs	—	20	—	μA	
CURRENT SOURCE TO V_{SS}					
Keyboard Inputs Common IDP, B:M,	—	20	—	μA	
Inhibit, Keyboard Mode	—	2	—	μA	
Clock In Leakage Current	—	—	20	nA	T_A = +25°C $V_{IN} = V_{SS}$ or V_{DD1}
Key Depression Period	10	—	—	ms	
OUTPUTS					
LINE:					
Logic '0' Output Current	2	—	—	mA	V_0 = 1.0V
Logic '1' Leakage Current	—	—	1	μA	V_0 = 5.0V
MASK:					
Logic '0' Output Current	2	—	—	mA	V_0 = 1.0V
Logic '1' Output Current	2	—	—	mA	$V_0 = V_{DD}$−1.0V
ALL OTHER OUTPUTS:					
Logic '0' Output Current	0.2	—	—	mA	V_0 = 1.0V
Logic '1' Output Current	0.2	—	—	mA	$V_0 = V_{DD}$ −1.0V
CLOCK FREQUENCY	17.28	18.00	18.72	kHz	For specified component values
SUPPLY CURRENT					
I_{DD1}	—	—	7	μA	V_{DD1} = 5.0V, V_{DD2} = 0V
I_{DD2}	—	—	200	μA	V_{DD2} = 5.0V, Note 2

NOTES:

1. The device will function correctly with a maximum logic '0' of 1.0V and a minimum logic '1' of V_{DD} −1.0V. However, use under these conditions may result in an increased supply current
2. Measured with Break: Make, IDP, inhibit and Keyboard Mode inputs at V_{SS}, and with no keys depressed.

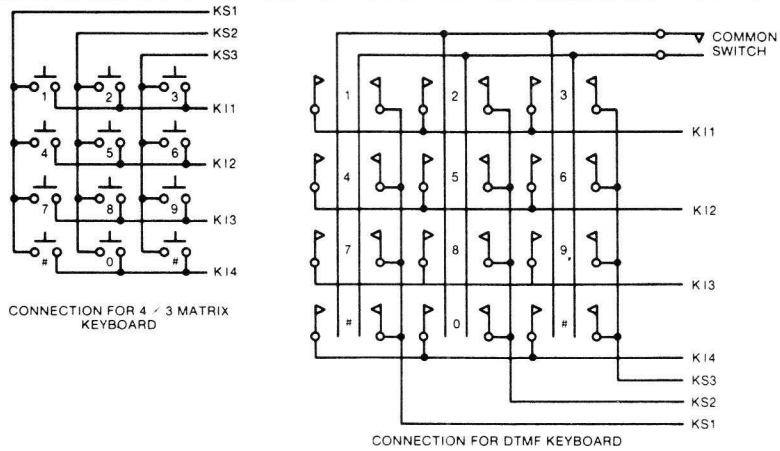


Fig.1 KEYBOARD CONNECTIONS FOR AY-5-9151 & AY-5-9152

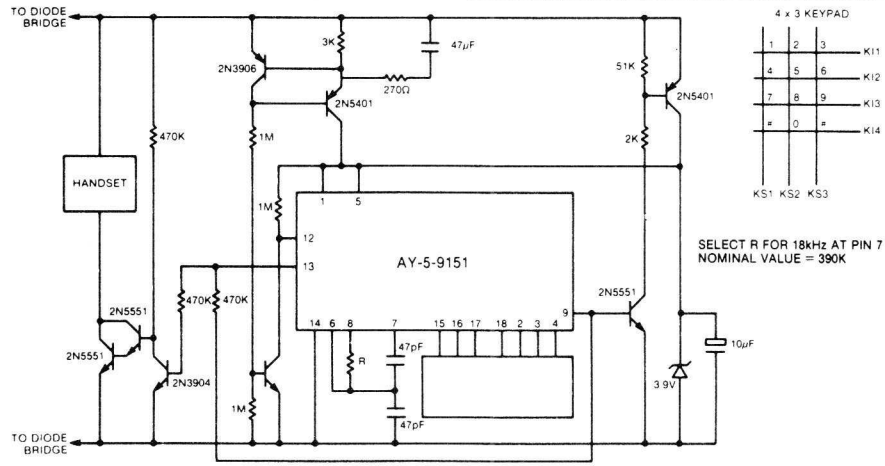


Fig. 2 PROVISIONAL PUSH-BUTTON DIALLER CIRCUIT USING AY-5-9151

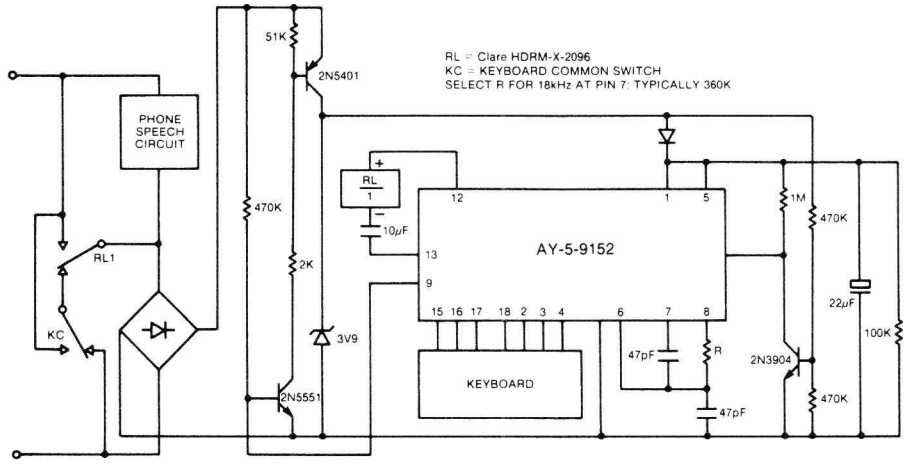


Fig. 3 PUSHBUTTON DIALLER USING MASK RELAY

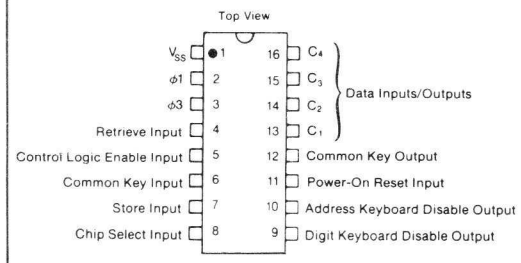
Repertory Dialler

FEATURES

- Stores 10 x 22 digit telephone numbers, including access pauses
- Devices can be 'stacked' to give a store expandable in blocks of 10 numbers
- Operates in conjunction with the AY-5-9100 Push-Button Dialler
- Single or Dual Keyboard operation
- Interfaces to standard MF Tone Dialler Keyboards
- Applications in Repertory Diallers and Security Systems
- Will operate MF Tone Diallers such as the AY-3-9400
- Low power consumption, typically 2.25mW

PIN CONFIGURATION

16 LEAD DUAL IN LINE



DESCRIPTION

The AY-5-9200 is a 10 number store designed to work in conjunction with the AY-5-9100 Push Button Telephone circuit to form a Repertory Dialler, each of the 10 numbers containing up to 22 digits or access pauses.

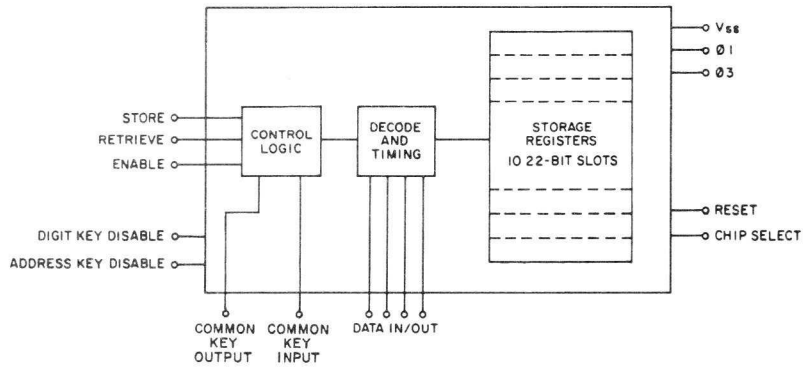
The keyboard, AY-5-9100 and as many AY-5-9200's as required are all connected to a 4 line data bus. Numbers for direct dialling are routed to the AY-5-9100, numbers to be stored go straight to the AY-5-9200. Numbers that are being retrieved are transmitted from the AY-5-9200 to the AY-5-9100 while control outputs from the AY-5-9200 determine the routing of the data.

The system may operate either with a single 12 button keyboard, which is used for both address and digit entry, or with separate address and digit keyboards. Single keyboard operation would normally be employed in a 10 number Repertory Dialling telephone. Dual keyboard operation is usual for 10 to 100 number Repertory Diallers.

The AY-5-9200 may also be used in MF tone dialling systems, the output data rate being directly compatible.

Four phase logic is used to achieve minimum power consumption, the circuits being manufactured using the MTNS P-channel nitride MOS process.

BLOCK DIAGRAM



Pin.No.	Name	Function
1	V_{SS}	This is the ground and substrate connection and is used as a reference for all the electrical parameters.
2-3	Clocks $\phi 1$, $\phi 3$	These inputs form the two supply clocks, and alternate negative-going pulses are required. These are described in the Electrical Characteristics and fig. 1. Any deviation from the nominal 18KHz will result in a proportional modification of the on-chip timings.
4	Retrieve Input	The retrieve input must be taken to a logic '1' for at least 10ms to indicate when a retrieve operation is to be performed. Anti-bounce logic is provided on this input.
5	Control Logic Enable Input	This input must be taken to a logic "1" for the duration of any store or retrieve operation. The control logic is reset when the input returns to logic '0'. Anti-bounce is provided for this input.
6	Common Key Input	This input is taken from the common contact on all keyboards. A '1' to '0' transition will indicate a key closure. Anti-bounce is provided to ensure only a single depression is read.
7	Store Input	This input must be taken to a logic '1' for the duration of any store operation. Anti-bounce logic is provided for both logic transitions.
8	Chip Select Input	When at logic '0' all inputs and outputs (except for Common Key input and output) are inhibited. It may be permanently wired to logic '1' if only one AY-5-9200 is used in the system.
9	Digit Keyboard Disable Output	The digit keyboard must be disabled while information is being transferred from the Store chip to the Push Button Dialler during a Retrieve operation. This output goes to a logic '0' during this period. In a single keyboard system this output is the one to be used.
10	Address Keyboard Disable Output	The address keyboard is to be disabled, both during a Retrieve operation when information is being transferred between chips and during the Store operation after an address has been allocated, until the Store operation is finished. This output goes to a logic '0' during these periods.
11	Power-On-Reset Input	An initial reset is required for clearing the chip when power is initially applied. This input must be held at a logic '0' initially, going to a logic '1' to activate the chips.
12	Common Key Output	This output is fed directly to the Common Key input of the associated AY-5-9100 Push Button Dialler and goes to a logic '0' to indicate a valid code signal. It controls the routing of data into the AY-5-9100. (See Function Description for further details.)
13-16	C_1 C_2 C_3 C_4	Data Input/Outputs. These four lines are connected to the system. Address and dialled digit information is input on these pins and dialling information is fed out from these pins to the Push-Button Dialler. The standard keyboard code accepted by the AY-5-9200 is shown below. When outputting information, the output is normally at a logic '1' and goes to a logic '0' for a data bit.

NOTE:
Chip Select, Retrieve, Control Logic Enable and an address can all be applied simultaneously to the Store Chip. Also Store and Control Logic Enable signals can be applied simultaneously.

KEYBOARD CODE

Digit	No. of Impulses	Code			
		C_1	C_2	C_3	C_4
1	1	1	1	1	1
2	2	1	1	1	0
3	3	1	1	0	1
4	4	1	0	1	1
5	5	1	0	1	0
6	6	1	0	0	1
7	7	0	1	1	1
8	8	0	1	1	0
9	9	0	1	0	1
0	10	1	1	0	0
Access Pause		0	0	1	1

FUNCTION DESCRIPTION

The following description applies to a Push Button Repertory Dialler using the AY-5-9100 and AY-5-9200 circuits. The system provides normal push button telephone facilities with access pause and redialling, together with a repertory dialling store expandable in blocks of 10 numbers.

The AY-5-9100 is a standard Push Button Dialler circuit with normal dialling and redialling facilities. It also has the capability of storing access pauses and waiting until a dial tone is detected by external circuitry before dialling is recommenced. This chip can operate by itself when a storage facility is not required. A detailed description of this device is contained in the AY-5-9100 data sheet.

The AY-5-9200 contains all the control logic and store facility required to store ten telephone numbers. Each number may be up to 22 characters in length, each character being either a digit or access pause; a dynamic memory technique being used for the data storage. Digits, access pauses and memory addresses are entered into the AY-5-9200 as 4-bit codes on 4 input/output pins which are also connected to the digit input pins of the AY-5-9100 as in Figs.4 and 5. While data is being transferred between the AY-5-9200 and the AY-5-9100, the keyboards are externally disabled by signals generated by the AY-5-9200, so that further key depressions have no effect until the transfer of data has been completed. Further address inputs are inhibited until the call is terminated.

The digit keyboard common key output is routed through the control logic and depending on the state of the logic, the Common Key output to the Push Button Dialler chip is enabled or disabled. This prevents digits to be stored and memory addresses from entering the Push Button Dialler.

The Common Key output from the AY-5-9200 is controlled as follows:

	C.S.	C.L.E.	
Logic Level	'0'	'0'	Common output is a direct replica of Common input and digits are dialled directly by the AY-5-9100
Logic Level	'1'	'1'	Common signals to the Push Button Dialler are generated only as a number is being retrieved (see Fig. 3). After a retrieve operation, Common signals are gated through, allowing further dialling unless externally inhibited.
Logic Level	'0'	'1'	No Common signals are generated and the output device goes off.

The control logic operates so that the first key depression at the beginning of an operation determines the subsequent sequence. Invalid key depressions at a later stage in a sequence are then ignored by the control logic.

The system is expanded by connecting further AY-5-9200 chips to the busses and using the Chip Select input to enable the required chip.

When a separate address keyboard is to be used an address keyboard strobe can be fed to the 'Retrieve' input, thus allowing a single button depression when retrieving a number from the store.

OPERATION MODES

1. STORE OPERATION

DEPRESS STORE

This sets the logic into a store mode. This signal must be present throughout the store operation. Thus, either electrical or mechanical bistable switching is required, or the 'Store' button must remain depressed during the sequence. The Control Logic Enable and Chip Select inputs should be activated at the same time. The Common Key output is inhibited and the address and digit codes are routed into the AY-5-9200 chip. The order of application of the signals is not important, they may be applied simultaneously with Address if required.

DEPRESS ADDRESS (one digit)

The address code, if valid, is latched and the memory location associated with this address is cleared to prevent corrupting the new number with old information. The Common Key output remains disabled. The Address Keyboard is also disabled for the remainder of the Store operation.

ENTER NUMBER DIGITS (and Access Pauses)

The number to be stored is then entered using the digit keyboard, and is stored in the addressed location. The maximum allowable number of digits or access pauses is 22. Chip select must be at logic '1' during digit entry.

RELEASE STORE, CONTROL LOGIC ENABLE AND CHIP SELECT

This is accomplished by re-setting the electrical or mechanical bistable or releasing the Store button. The control logic is then reset and disabled.

2. RETRIEVE OPERATION

DEPRESS RETRIEVE

For separate address keyboard systems, this signal can be generated automatically with the address. The control logic is set in a retrieve mode and the address inputs are enabled. Control Logic Enable and Chip Select must be at logic '1' for the whole of the Retrieve operation, including the data transfer period. The Retrieve input must be returned to logic '0' before the end of data transfer to prevent a repeat operation.

DEPRESS ADDRESS (Digit)

The address is decoded and latched, both keyboard disable outputs go active, disabling the keyboards. After a minimum period of 60ms, the first digit code is transmitted to the Push Button Dial chip together with a Common signal. The Common is stable for a minimum period of 60ms, the Common only being present while the code is stable. The data transmission continues at 60ms on, 60ms off until the whole number has been transferred after which the chip is reset, the keyboard disable signals are removed and the Common signal is enabled to the Push Button Dialler chip. (See Fig. 3.)

3. ERASE OPERATION

This operation is basically a Store operation with no digits being input.

DEPRESS STORE

This sets up the logic as in the Store operation.

DEPRESS ADDRESS (Digit)

This then clears the decoded address.

RELEASE STORE

This is accomplished either by releasing 'Store' input, or re-setting the mechanical or electrical 'Store' bistable.

4. RECALL AND NORMAL DIALLING

These are performed as for the Push Button Dialler on its own. See AY-5-9100 data sheet for full description.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . −20V to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . −55°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS}=0V
Vϕ=−15±1.5V (see fig. 1 for waveform)
Clock frequency=18kHz
Operating Temperature (T_A)=−55°C to +80°C
Negative logic conventions are followed for this data sheet.

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock					
Logic '0' level	+0.3	—	−1	Volts	Note 1
Logic '1' level	−13.5	—	−16.5	Volts	
Frequency	10	18	30	kHz	
Rise Time (Tr)	0.1	—	4	μs	
Fall Time (Tf)	0.1	—	8	μs	
Width (Tw)	5	—	40	μs	At logic '1' min. level
Separation (Ts)	5	—	40	μs	At logic '0' max. level
Capacitance	—	70		pF	Per phase Vϕ=0V, f=1MHz(Note 2)
Leakage	—	—	10	μA	Vϕ=16.5V, T_A=25°C
Inputs					
Logic '0' level	+0.3	—	−1	Volts	
Logic '1' level	−5	—	−16.5	Volts	
Capacitance	—	—	5	pF	V_{IN}=0V, f=1MHz
Leakage	—	—	1	μA	V_{IN}=−16.5V, T_A=25°C
Common Key Input					
Pulse Width (Tc)	10	—	—	ms	At logic '0' max level see fig. 2
Reset Input					
Pluse Width (Td)	3	—		ms	After clocks reach full amplitude
Fall Time (Te)	—	—	100	μs	Fig.2
Anti-bounce on all Inputs except Chip Select & Reset	4.2	—	—	ms	
Outputs					
All outputs including C_1 to C_4 when acting as outputs					
Logic '0' output current	0.6	—	—	mA	V_0=−1V
Logic '1' output leakage	—	—	10	μA	V_0=−10V
Digit Output Rate	—	8.35	—	Hz	
Power	—	2.25	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. Clock logic '0' levels should be within 0.5V of each other.
2. The effective dynamic clock capacitance while operating is 260pF.

TIMING DIAGRAMS

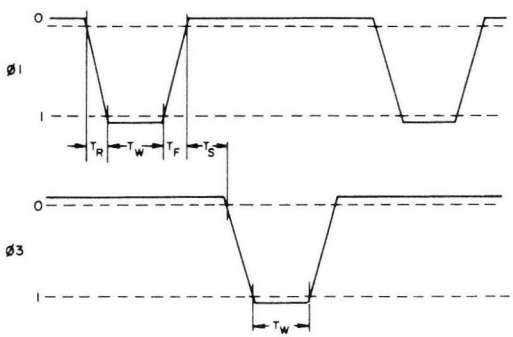


Fig.1 CLOCK WAVEFORMS

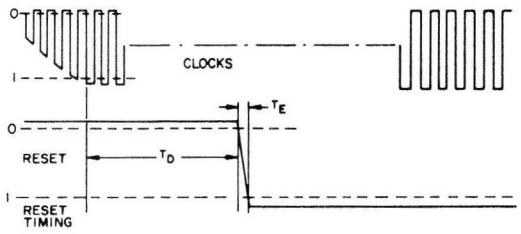


Fig.2 CLOCK WAVEFORMS WITH RESET TIMING

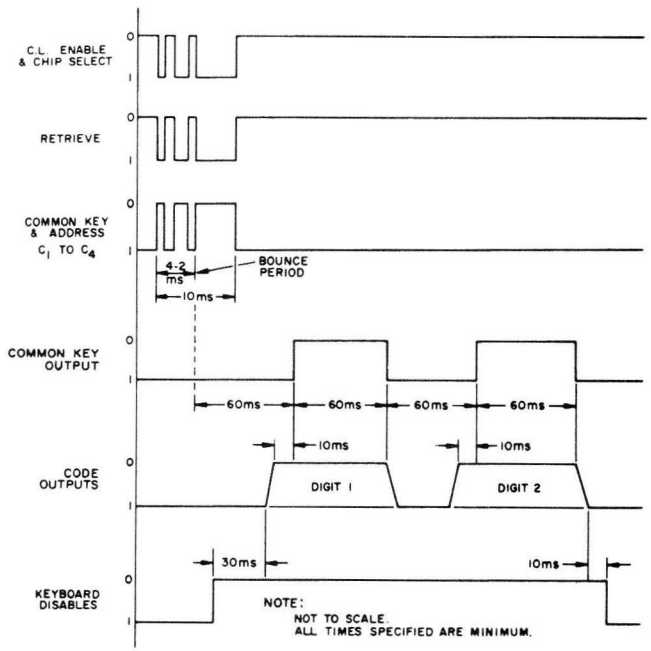


Fig.3 "RETRIEVE" WAVEFORMS

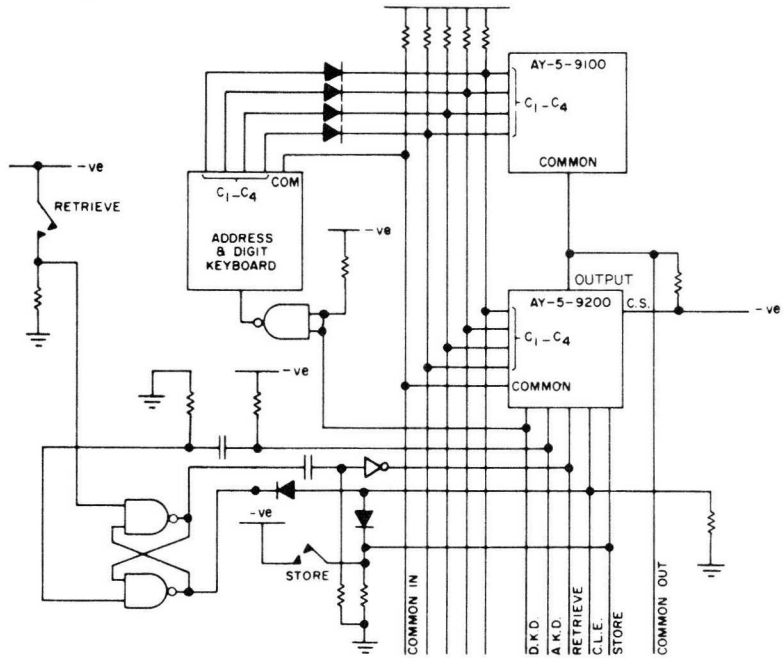


Fig.4 SINGLE KEYBOARD SYSTEM FOR REPERTORY DIALLER

Note for Figs.4 and 5
Logic: CD4011A (C-MOS)
Resistors: 100K
Capacitors: 0.1uF
Diodes: 1N914

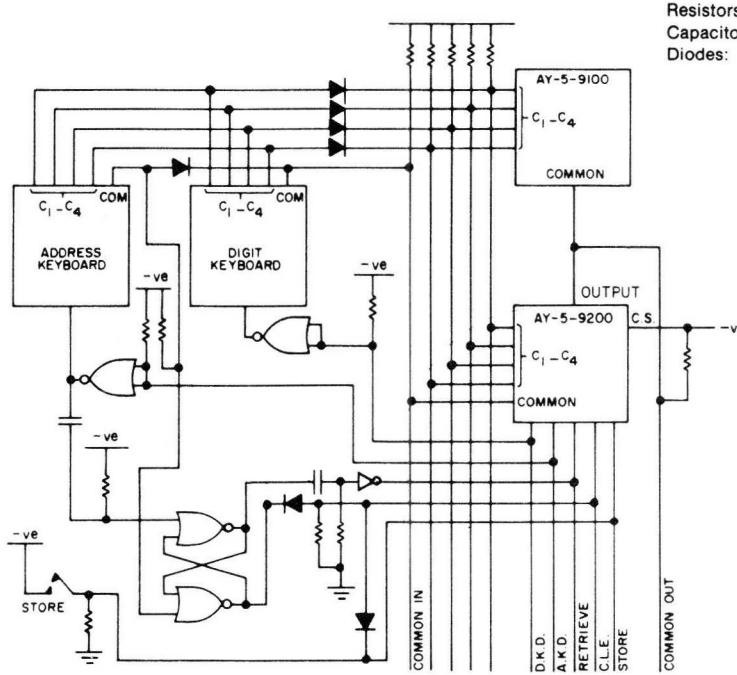


Fig.5 DUAL KEYBOARD SYSTEM FOR REPERTORY DIALLER

TELECOM

AY-3-9400
AY-3-9401 AY-3-9410

Dual Tone Multi-Frequency Generators

FEATURES

- No tuning required, inherent accuracy ± 0.25%
- Uses low cost ceramic resonator
- 12 tone pairs (16 tone pairs with AY-3-9401/9410 and choice of high group pre-emphasis with AY-3-9410)
- Total harmonic distortion less than 8% (but dependent on external filter)
- Instant generation of tone outputs
- Low voltage drop
- Low power consumption (less than 35mW)
- Good thermal and voltage stability
- Keyboard lock out inhibits output if more than one key depressed
- N-channel ion implant construction
- High group pre-emphasis fixed at 3.52dB (AY-3-9400), 2dB (AY-3-9401), 3/6dB (AY-3-9410).
- Pre-emphasis can be varied by simple component adjustment.

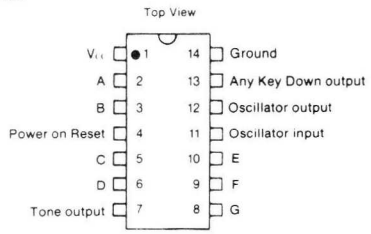
DESCRIPTION

The AY-3-9400/9401/9410 DTMF circuits generate all the tone pairs required for multifrequency tone dialing. The tones are generated from a single ceramic controlled master oscillator, ensuring high accuracy and stability of the output frequencies and eliminating the need for any adjustments. The digitally synthesized tones give precisely controlled characteristics.

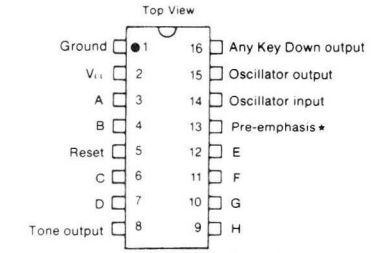
The AY-3-9400/9401/9410 is fabricated using the ion implant N-channel low voltage process, and employs novel logic techniques to minimize power consumption and voltage drops. The circuit is suitable for operation direct from telephone line power, or it can be used with main power or battery supplies.

PIN CONFIGURATION

14 LEAD DUAL IN LINE
AY-3-9400

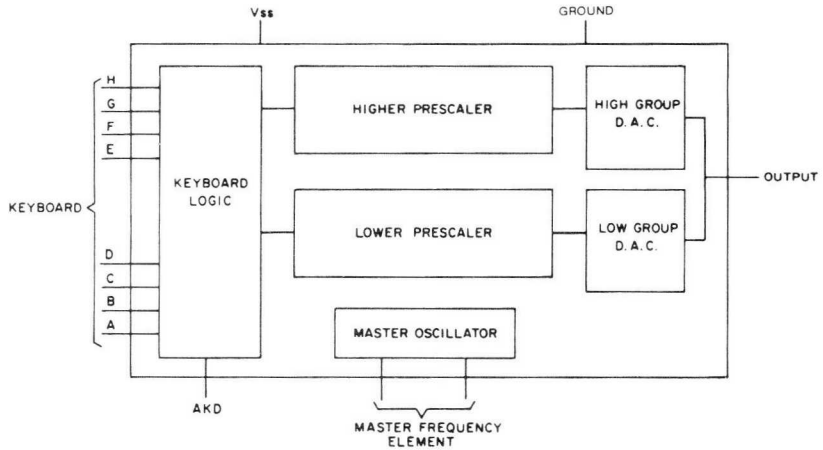


16 LEAD DUAL IN LINE
AY-3-9401/AY-3-9410



*2dB on AY-3-9401, 3/6dB on AY-3-9410.

BLOCK DIAGRAM



AY-3-9401/9410

OPERATION

When a key is pressed the chip will immediately start operating, the output tones both starting from zero on the first negative half cycle. The first cycle will be of full amplitude assuming the power supply is at the correct level. If power is applied at the same time as a key is pressed, the power on reset circuit will operate, preventing spurious outputs.

When two or more keys are pressed together, one or both tones will be switched off. The tones will start from zero as soon as the extra keys have been released. When all keys are released, the tone outputs will immediately cease.

If only one key contact is made, a single tone corresponding to the closed contact will be output. The "Any Key Down" output, which requires a pull-up resistor (typ. 47K), goes to logic '0' as soon as a key depression is recongnized.

The tones are output on a single pin, as a mixture of pulse width modulated, constant amplitude square waves. This output signal is constructed into resultant sine waves in the external low pass filter. The approximation chosen yields a total harmonic distortion of less than 8%.

The amplitude of the output signal is directly proportional to the V_{CC} supply voltage.

A low pass filter buffer amplifier is used to remove switching noise and interface the tones to the line. There is an option of either a low impedance or a high impedance output for interfacing to telephone lines. The low impedance circuit is shown in Fig. 1.

NOTES:

1. Pre-emphasis selection for the AY-3-9401: Connect pin 13 to ground for 2dB pre-emphasis. Pre-emphasis selection for the AY-3-9410: Connect pin 13 to V_{CC} for 3dB high group pre-emphasis, or to ground for 6dB pre-emphasis. The circuits are otherwise identical in operation to the AY-3-9400.
2. See MFO2 specification for the resonator.

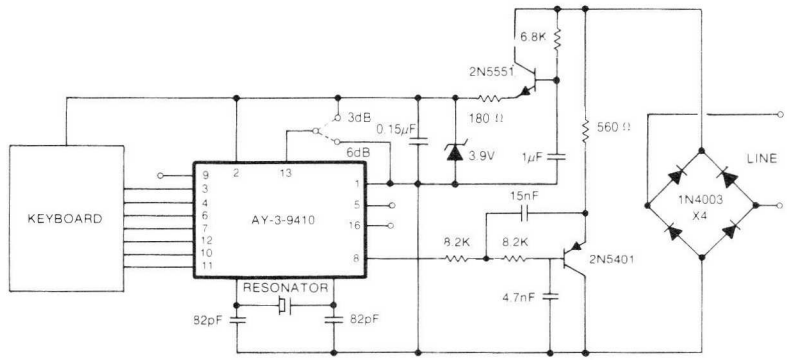


Fig. 1 LOW IMPEDANCE INTERFACE CIRCUIT

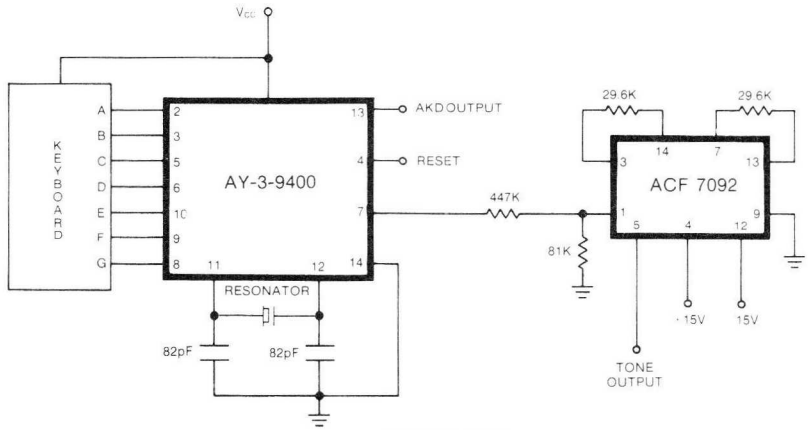


Fig. 2 AY-3-9400 TEST CIRCUIT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin . . . . +10V to —0.3V
Storage temperature range . . . . . —65°C to +150°C
Ambient operating temperature range. . . . . -25°C to -70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{cc} = +3.5 to +8V
F Clock=559.7kHz
Operating Temperature (T_A) -25°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic '1'	+3.3	—	+8	Volts	Logic '1' activates tone
Input Logic '0'	—0.3	—	+0.4	Volts	
Input pull down resistance	20	—	100	kΩ	Resistor to ground
Input capacitance	—	—	10	pF	
Tone output Low Group	—	0.312	—	V_{peak}	V_{cc} = 4V, Note 1, Note 4
Tone output High Group	—	0.486	—	V_{peak}	V_{cc} = 4V, Note 1, Note 4
High group pre-emphasis	—	3.52	—	dB	1.6dB typ. for AY-3-9401.
Output impedance	—	—	500	Ω	Note 2, Note 3
Any Key Down output					
On resistance	—	—	1	kΩ	Vout = +1V
Off Leakage	—	—	10	μA	Vout = +8V
Total Distortion	—	—	—23	dB	Note 4
Harmonic component	—	—	—30	dB	Note 4
Supply current	—	—	8	mA	V_{cc} = +3.5V
	—	—	10	mA	V_{cc} = +8V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. The amplitudes of the output signals are directly related to the V_{cc} supply voltage.
2. The chip output is intended to drive a low pass filter having an input impedance of greater than 8K.
3. The output would be buffered to drive the line, the buffer can be arranged to have either a high impedance current output or a low impedance voltage output (See Fig. 1).
4. Output parameters determined by Test Circuit (See Fig. 2).

FREQUENCY OUTPUTS

All output frequencies are derived from a 559.7kHz master oscillator.
The output frequencies are as follows:

	Nominal frequency Hz	Actual Frequency Hz	Error %	Key
Low Group	697	695.28	—0.25	A
	770	768.82	—0.15	B
	852	850.61	—0.16	C
	941	940.68	—0.03	D
High Group	1209	1211.48	+0.21	E
	1336	1332.62	-0.25	F
	1477	1480.69	+0.25	G
	1633	1631.78	—0.07	H

TYPICAL CHARACTERISTIC CURVES

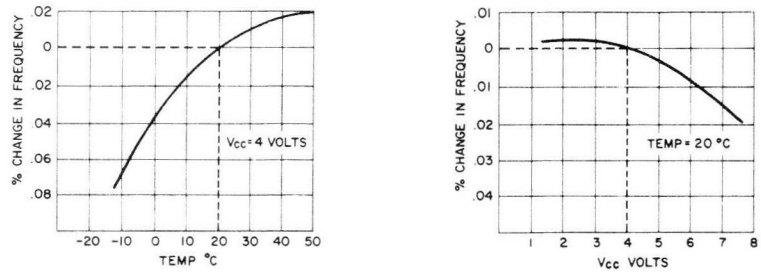


Fig.3 OSCILLATOR CHARACTERISTICS

C-MOS Clock Generator

FEATURES

- Generates 2 phase clock from single power supply
- Operates with AY-5-9100 Push Button Dialler and AY-5-9200 Repertory Dialler
- Very Low power consumption, allowing use of line powered telephones
- Minimizes external components in Push Button Telephones
- Stable generation of clock frequencies

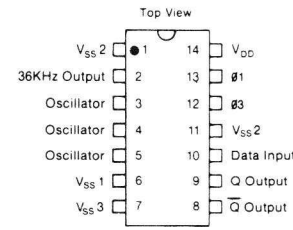
DESCRIPTION

The AY-5-9500 is a C-MOS circuit designed to generate the 2 phase clock required by the AY-5-9100 series of Push Button Telephone Diallers and the AY-5-9200 Repertory Dialler circuit.

It consists of an RC oscillator, a level shifter, a 2 phase clock generator and driver, and a clocked D-type bistable. The RC oscillator is set by external components to run at 36kHz and is normally operated from a −4 Volt supply to minimize power consumption. The oscillator output is shifted and used to drive the 2 phase clock generator. The D-type bistable is either used as a Reset generator for the AY-5-9100 or AY-5-9200 or it is used to drive a Cockroft-Walton voltage multiplier to generate the nominal 15 Volt supply for the AY-5-9100 and AY-5-9200.

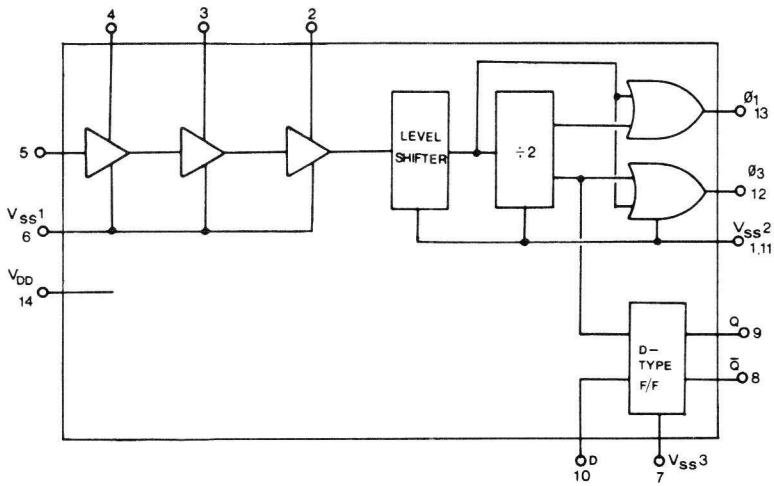
PIN CONFIGURATION

14 LEAD DUAL IN LINE



TELECOM

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{DD} pin .....−15V to +0.3V
Storage temperature range ..... −65°C to +150°C
Ambient operating temperature range .....−25°C to +70°C
Output Current .....7mA per output

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

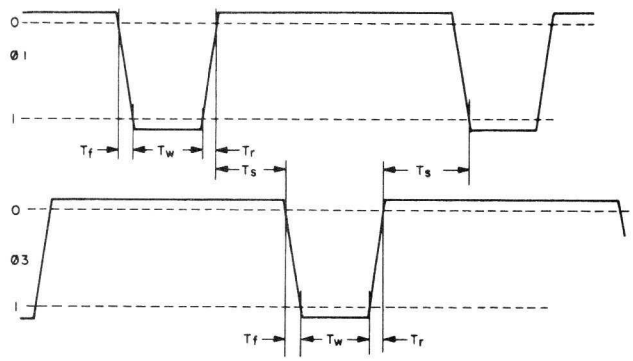
V_{DD} = 0V
$V_{SS}1$ = −3.8V to −8.5V
$V_{SS}2$ = −3.8V to −15.0V
$V_{SS}3$ = −3.8V to −15.0V
F Clock = 36kHz ± 10%
Operating Temperature (T_A) = +25°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock Outputs					
Frequency at pin 12	15.8	18.0	20.2	kHz	V_{SS} = 4.0V, T_A = +25°C, Note 1, Fig 1.
Frequency stability	−5		+8	%	V_{SS} 1 = −4.0V, T_A = +25°C, Fig. 2.
Rise Time (T_R)	—	—	700	ns	V_{SS} 2 = −3.8V }
	—	120	250	ns	V_{SS} 2 = −15V } At 360 pF
Fall Time (T_F)	—	—	600	ns	V_{SS} 2 = −3.8V } load/phase
	—	90	200	ns	V_{SS} 2 = −15V }
Width (T_W)	10	—	—	μs	} Fig. 1
Separation (T_S)	10	—	—	μs	
Input Leakage	—	—	20	nA	T_A = +25°C, Fig. 3
Output Current-Logic "0" (High)					
Pin 2	0.5	—	—	mA	}
ϕ 1, ϕ 3	0.5	—	—	mA	} V_{OUT} = −0.5V
Q, $\overline{Q}$	0.8	—	—	mA	}
Output Current-Logic "1" (Low)					
Pin 2	0.5	—	—	mA	}
ϕ 1, ϕ 3	0.5	—	—	mA	} V_{OUT} = +0.5V
Q, $\overline{Q}$	0.8	—	—	mA	}
Power Supply Current					
I_{SS1}	—	200	250	μA	V_{SS}1 = −4.0V
I_{SS2}	—	—	50	μA	V_{SS2} = −4.0V
	—	200	250	μA	V_{SS2} = −15V
I_{SS3}	—	—	15	μA	V_{SS}3 = −4.0V
	—	50	60	μA	V_{SS} 3 = −15V

** Typical values are at +25°C and nominal voltages.

NOTES: 1. In practice, it is recommended that the capacitor at pin 3, or the resistor at pin 4, be adjusted to set the frequency to 18 kHz with a nominal supply voltage at an ambient temperature of +25°C.

TIMING DIAGRAM



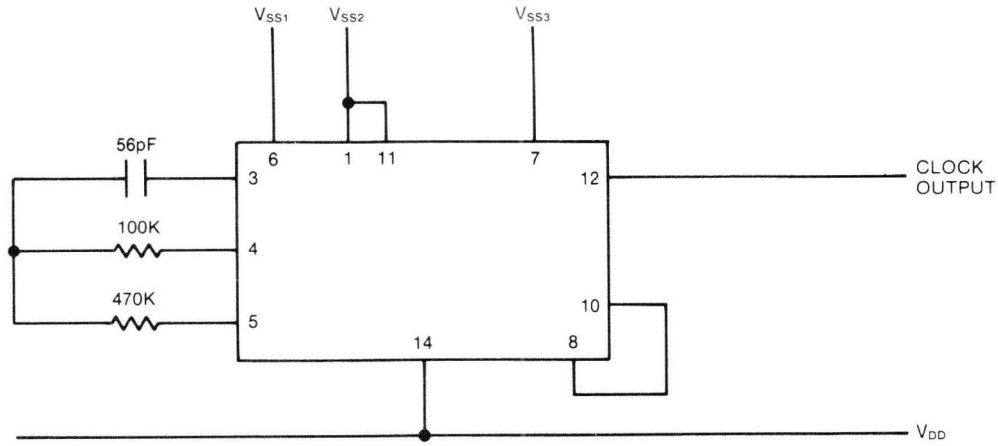


Fig. 1

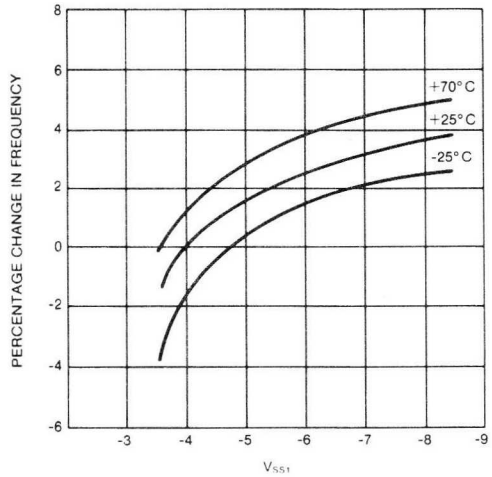


Fig. 2 TYPICAL FREQUENCY STABILITY

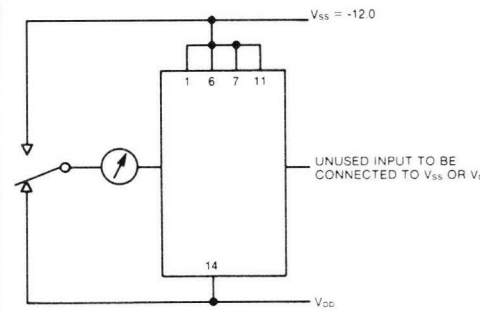


Fig.3 INPUT LEAKAGE CURRENT TEST

TELECOM

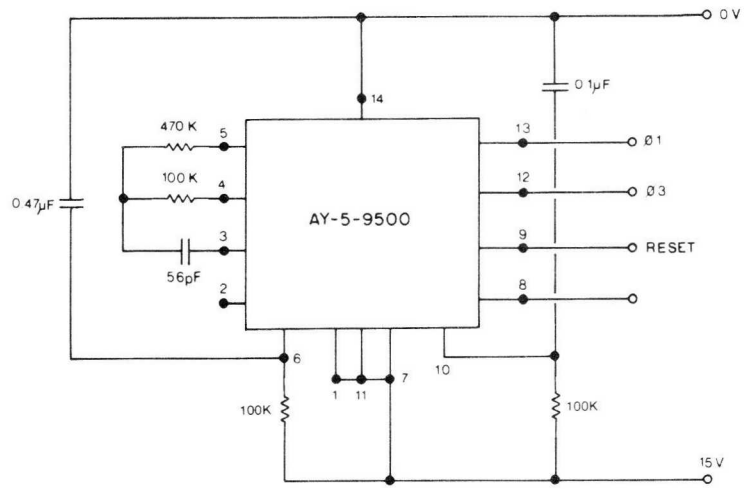


Fig.4 SINGLE SUPPLY OPERATION

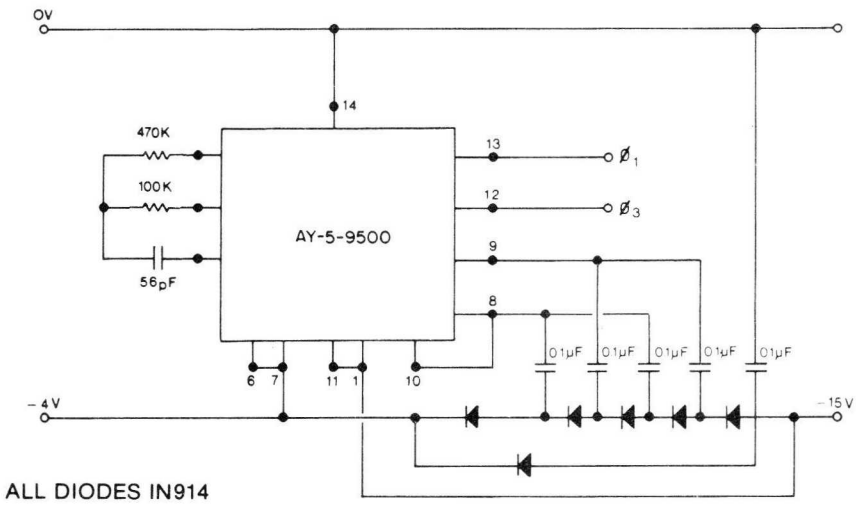


Fig.5 DC-DC CONVERTOR CONNECTION

I^2L Push Button Telephone Dialler

FEATURES

- Low operating power and voltage (1mW and 1.5V)
- Direct line switching
- Very few external components required.

DESCRIPTION

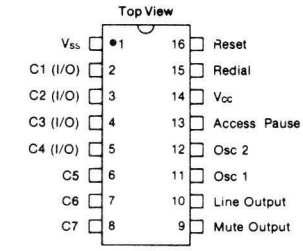
The AY-9-9600 utilizes I^2L technology to provide a low power, low voltage, single number push button dialler intended for applications where power is derived from the telephone lines.

The AY-9-9600 provides all of the logic required to convert a push button input to a series of pulses suitable for simulating a rotary telephone dial. Dialing rate is controlled by the oscillator frequency. Inter-digital pause (IDP) and mark/space ratio are mask programmable. Internal clock generation, power-on reset, pull-up/down resistors are provided to minimize the external component count. The input code configuration is also mask programmable.

The AY-9-9600 has been designed to interface with standard MF tone dialer (2 of 7) keyboards, 3×4 cross point arrays, 1 of 10 and 1 of 12 keyboards as well as direct BCD input. Seven input lines (C1 - C7) are used for 2 of 7, 3×4 and BCD. 10 or 12 inputs are used when the circuit is configured for 1 of 10 or 10 of 12 coding (requiring a 22 lead dual in line package).

PIN CONFIGURATION

16 LEAD DUAL IN LINE



TELECOM

Dual Tone Multi-Frequency Receivers

FEATURES

- No tuning required; inherent discrimination better than ±0.1%
- Digitally defined bandwidths with no inherent voltage or temperature drift
- Acquisition time typically 25 ms. (tone inputs to common output)
- Frequency correlation provides good S/N performance
- Inter-tone separation checked for correct IDP period
- Many programmable features provide wide applications
- High reliability and low cost using P-channel process
- On-chip analog amplifiers for analog preprocessing
- Interfaces directly with the AY-5-9100 for M.F.—Strowger converters. (AY-5-9801/9805)
- Handshaking facility to interface directly with CP1600 microprocessor
- Three-State code outputs

AY-5-9800 SERIES

Part Number*	Output Code	On-Chip OP Amps	Pins
AY-5-9801/9821	4-Bit	Yes	28
AY-5-9802/9822	1 of 16	Yes	40
AY-5-9803/9823	2 of 8	Yes	40
AY-5-9804/9824	Binary	Yes	28
AY-5-9805/9825	4-Bit	No	24
AY-5-9806/9826	1 of 16	No	40
AY-5-9807/9827	2 of 8	No	24
AY-5-9808/9828	Binary	No	24

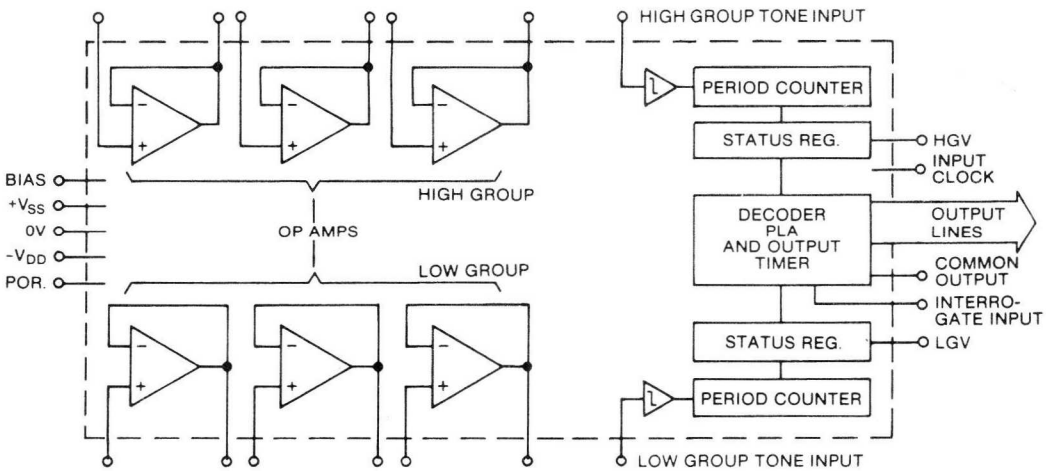
*Part numbers AY-5-9801 through 9808 are supplied in ceramic packages. Part numbers AY-5-9821 through 9828 are supplied in plastic packages.

PROGRAMMABLE OPTIONS

These options can all be provided by a single layer mask change.

- Programmable center frequencies
- Programmable accuracies
- Variable "Acquire" criteria (1 out of 5 to 5 out of 5)
  Variable "Release" criteria (1 out of 5 to 5 out of 5)
- Normally arranged for 2 of 8 detection, but can be reprogrammed for single tone (1 of 8) detection
- Common output can be delayed by 1-32 ms after tones are detected valid
  Note: IDP period = common delay + common width
- Common output pulse can be programmed from 1-31 mS.
- Output code can be any 4 bit code in 24/28 lead DIP or any 16-bit code in 40 lead DIP (e.g. 2 of 7, 1 of 12 etc.)

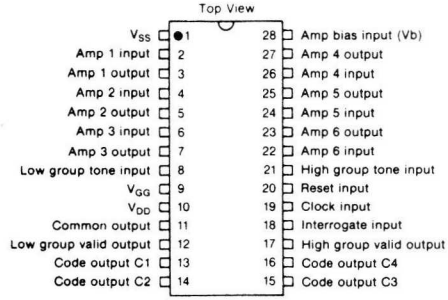
BLOCK DIAGRAM



PIN CONFIGURATIONS

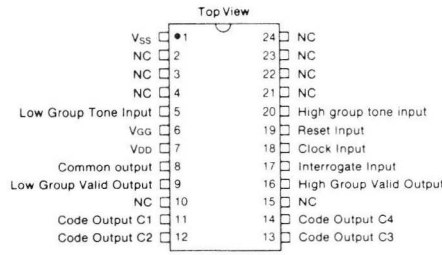
28 LEAD DUAL IN LINE
AY-5-9801/9821
AY-5-9804/9824

Top View



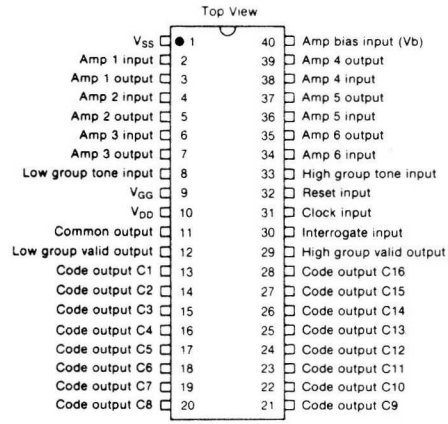
24 LEAD DUAL IN LINE
AY-5-9805/9825
AY-5-9808/9828

Top View



40 LEAD DUAL IN LINE
AY-5-9802/9822

Top View

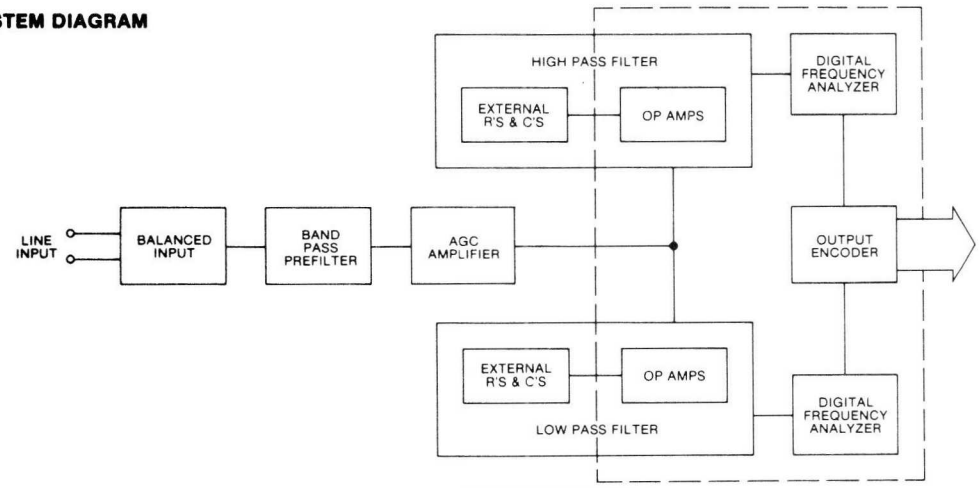


40 LEAD DUAL IN LINE
AY-5-9803/9823
Not yet defined

40 LEAD DUAL IN LINE
AY-5-9806/9826
Not yet defined

24 LEAD IN DUAL LINE
AY-5-9807/9827
Not yet defined

SYSTEM DIAGRAM



TELECOM

DESCRIPTION

The AY-5-9800 series circuits are fabricated in P channel MTNS process thus minimizing cost and providing high reliability. The basic chip block diagram is shown on the previous page. For analog preprocessing six amplifiers and two source followers are included on-chip, external components being used to determine the filter characteristics. The major functions are mask programmable thus giving a flexible system at a low cost.

The tone pair is separated into two individual tones using the analog circuitry, the separated tones being applied to the Schmidt triggers to square incoming signals which are then processed by the digital circuitry. The high and low group logic is similar; only the decode values for frequency recognition are different. The incoming signal is divided by two or three to eliminate the effects of changing mark/space ratio and its period counted by a timer which is clocked by the accurate 1MHz clock. If the period value is within encoded limits, the result is stored. Five cycles of incoming signal are stored and a decision is made with this information as to whether the tone is valid. A programmable logic array scans the five cycle store for both an "Acquire" criteria and "Release" criteria. If the "Acquire" criteria is exceeded (e.g. 4 out of 5), and the "Release" criteria is not reached (e.g. less than 2 out of 5), the frequency is deemed to be valid. If both high and low frequencies are detected, a time-out timer is started. This timer is mask programmable and will normally require 25ms of valid tone pair signal. Once this period has elapsed the Common Output pulses high, again for a preprogrammed period. After this pulse, the system will not respond again until an IDP of a preprogrammed duration occurs, after which a new input tone pair can be applied.

The Code Outputs and Common Output can be configured for a wide variety of systems. A typical device, AY-5-9801/9821, provides four Three-State Code outputs suitable for microprocessor controlled systems and direct interfacing to the AY-5-9100 for DTMF-Strowger converters. A handshaking interface is provided using the Interrogate input thus allowing very simple microprocessor interfacing. The outputs will directly drive low power TTL, CMOS or MOS and, being Three-State, can be bussed in large systems.

Input Clock — The recommended clock frequency is 1MHz which will then give a frequency detect range of 620—3400Hz with a discrimination of ± 1μs. The discrimination of 1633Hz using a 1MHz clock will be better than ± 0.1%. Any deviation of the 1MHz clock will result in a proportional deviation of the tone recognition bands.

Power-On-Reset—An external power-on reset is required which is used to reset all counters, etc. An on-chip resistor pulls this input to V_{DD}; a 0.1μF capacitor connected from the P.O.R. input to V_{SS} will provide automatic power-on-reset. This input can be used as a chip select putting all Three-State outputs into their high impedance state when held high.

Input Amplifiers—Input amplifiers are suitable for use in band-pass and general buffer amplifiers. They have an open loop gain of approximately 250 and are trimmed by a single 'Bias Input'.

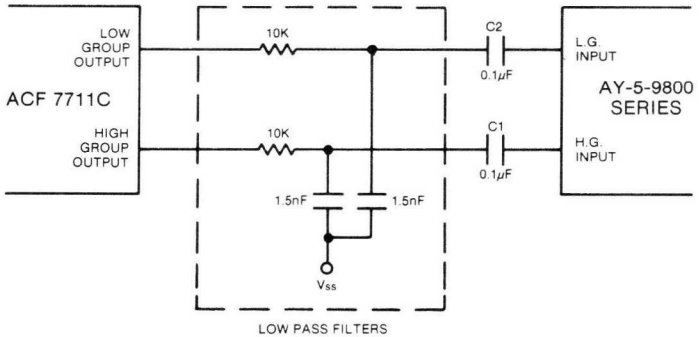
Period Counters—The input frequency, which must be A.C. coupled, is interrogated by the period counter. Each counter has eight values decoded, these representing F1 low limit, F1 high limit etc. Once a positive going edge is detected, the period counter is started and if the next positive going edge occurs during a time slot decode, the circuit deems the tone to be valid and a bistable indicating the tone decoded is set. Special logic is incorporated to prevent the counter from being continuously triggered in the presence of noise.

Status Word Register—The Status Word Register is a five bit register which is filled with 1's for an in-band signal but filled with 0's for out-of-band signals. With the data in this register a decision is performed which sets a bistable (Acquires the signal) or resets a bistable (Releases the signal). Thus by changing the preprogrammed acceptance standard, a direct trade-off between S/N ratio and stimulation rate can be obtained for different systems.

Output Logic—Two outputs, HGV and LGV, indicate the current state of the correlator for each group. A valid high group frequency, if present for longer than the correlation time, will cause the HGV (high group valid) output to go high. Similarly with the LGV (low group valid) output. Once both high and low group tones have been detected valid, a preprogrammed timer is started. If the tone pair is still valid after the timer has counted out, the Common Output goes high for a preprogrammed period and the Code Outputs present the programmed outputs corresponding to the tone pair input.

If the interrogate input is used for handshaking, the Code Outputs are only presented after the interrogate input goes low, the interrogate input going high removes both the Codes and the Common Output.

AY-5-9800 SERIES SYSTEM IMPROVEMENT NOTE



Leakage of the 1MHz Clock signal onto the High or Low Group inputs can cause intermittent High or Low Group Valid outputs, and reduction of the system sensitivity.

To remedy this, the low pass filters shown below are inserted between the ACF 7711 Band Separation Filter and the input decoupling capacitors (C1 and C2) of the AY-5-9800 series Multi-Frequency Receivers. This restores proper operation of the MFR while attenuating stray clock signals more than 39 db.

OUTPUT CODE CHART

Input Tone Pair		Normal Digit Representation	AY-5-9801/9821 AY-5-9805/9825 Output Code*				AY-5-9802/9822 AY-5-9806/9826 Output Code	AY-5-9803/9823 AY-5-9807/9827 Output Code	AY-5-9804/9824 AY-5-9808/9828 Output Code**			
Low Group (Hz)	High Group (Hz)	C1	C1	C2	C3	C4	1 of 16	2 of 8	C1	C2	C3	C4
697	1209	1	1	1	1	1	C1	C1,C5	1	1	1	0
697	1336	2	1	1	1	0	C2	C1,C6	1	1	0	1
697	1477	3	1	1	0	1	C3	C1,C7	1	1	0	0
697	1633	—	0	0	0	1	C4	C1,C8	0	0	0	1
770	1209	4	1	0	1	1	C5	C2,C5	1	0	1	1
770	1336	5	1	0	1	0	C6	C2,C6	1	0	1	0
770	1477	6	1	0	0	1	C7	C2,C7	1	0	0	1
770	1633	—	0	0	1	0	C8	C2,C8	0	0	1	0
852	1209	7	0	1	1	1	C9	C3,C5	1	0	0	0
852	1336	8	0	1	1	0	C10	C3,C6	0	1	1	1
852	1477	9	0	1	0	1	C11	C3,C7	0	1	1	0
852	1633	—	0	1	0	0	C12	C3,C8	0	0	1	1
941	1209	*	0	0	1	1	C13	C4,C5	0	1	0	0
941	1336	0	1	1	0	0	C14	C4,C6	0	1	0	1
941	1477	#	0	0	0	0	C15	C4,C7	0	0	0	0
941	1633	—	1	0	0	0	C16	C4,C8	1	1	1	1

*Compatible with AY-5-9100 **Compatible with AY-5-9120.

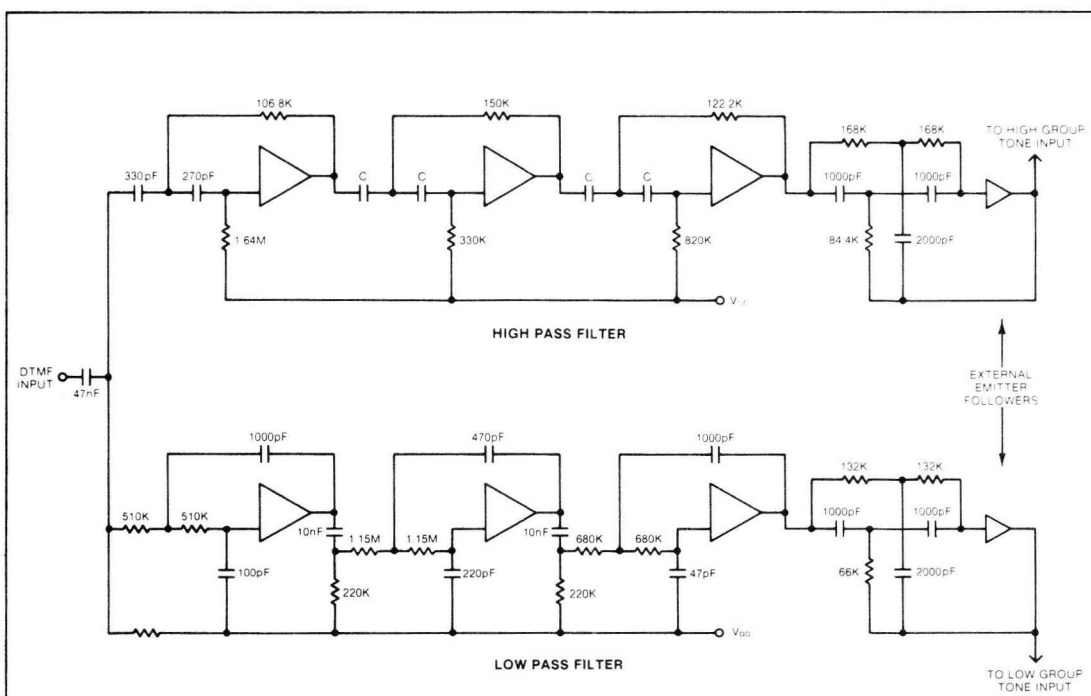


Fig. 3 FILTER CONNECTIONS (Active elements on chip)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage Temperature Range ..... -65°C to +150°C
Ambient operating temperature ..... -25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -8.5 ±0.5V
V_{GG} = -17V ±1V
Clock frequency = 1 MHz
Operating Temperature (T_A) = +25°C

Characteristics	Min	Typ	Max	Units	Conditions
Clock					
Logic '0' level	+0.3	—	-1.0	V	
Logic '1' level	-6.5	-8.5	-18	V	
Frequency (see NOTE below)	0.01	1.0	1.1	MHz	
Rise Time	10	—	50	ns	
Fall Time	10	—	50	ns	
Width	450	500	550	ns	
Capacitance	—	—	20	pF	
Leakage	—	—	10	µA	
Logic Inputs					
Logic '0' level	+0.3	—	-1.0	V	
Logic '1' level	-3.7	-5	-18	V	
Capacitance	—	—	10	pF	
Leakage	—	—	10	µA	
Logic Outputs					
(i) Code outputs					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	460	—	—	µA	V_O = -5V
(ii) Common output					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	620	—	—	µA	V_O = -5V
Pulse delay	1	—	31	ms	
Pulse width	1	32	32	ms	
(iii) Group valid outputs (HGV & LGV)					
Logic '0' output current	500	—	—	µA	V_O = -1V (External pull-down resistors to V_{DD} required).
Signal Input	.5	—	2	V	Peak to peak sine wave
"Handshake" Routine					
(See Fig. 1 for timing diagram). T1, T2	—	—	2.5	µs	
Pull-down resistor (to V_{DD})	50	150	500	kΩ	
Power-on Reset					
Pull-down resistor (to V_{DD})	50	150	500	kΩ	
Pulse Width	10	—	—	µs	
Amplifiers					
Open loop gain	—	500	—	—	F_{in} = 1kHz
Open loop bandwidth	—	1	—	MHz	
Output Impedance	—	—	6	kΩ	F_{in} = 1kHz
Power Dissipation	—	—	350	mW	V_{DD} = -9V V_{GG} = -18V

NOTE: Any deviation from the nominal 1MHz clock frequency will result in a corresponding deviation of the frequency detection bands. Other frequencies than 1MHz clock can be preprogrammed in, but circuit characteristics will be modified.

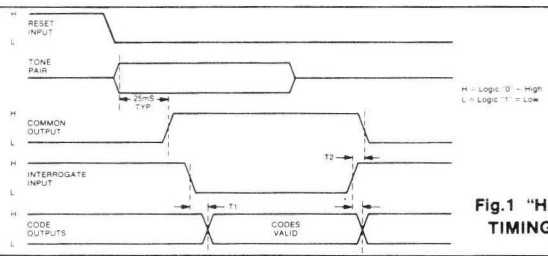


Fig.1 "HANDSHAKING" TIMING DIAGRAM

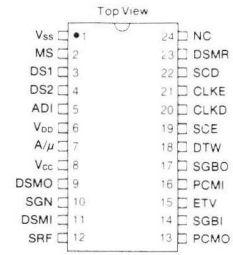
PCM Code Converter (CODEC)

FEATURES

- Converts a delta-sigma modulated pulse stream at 2048 kbit/sec into 8 ksample/sec companded PCM.
- Converts 8 ksample/sec companded PCM into a delta-sigma modulated pulse stream at 2048 kbit/sec.
- Enables the realization of a single channel PCM Codec using a minimum of external components.
- Serial PCM input/output interface can operate in a single channel mode at 64 kbit/sec, or at up to 2048 kbit/sec for a multi-channel burst format.
- All digital technique uses no on-chip precision components.
- Pin-selectable A-law/μ-law companding characteristic.
- Optional alternate digit inversion provided.
- Direct interface with standard TTL or CMOS.
- Encoder and Decoder can be clocked asynchronously (useful for PCM multiplex applications)

PIN CONFIGURATION

24 LEAD DUAL IN LINE



DESCRIPTION

The AY-3-9900 provides all the logic necessary to realize a high performance, low cost, single channel PCM Codec using a minimum of external components. The AY-3-9900 has been designed with a pin-selectable choice of companding characteristic: either the standard 8 bit A-law characteristic or the standard 8 bit μ-law characteristic.

The AY-3-9900, together with the external delta-sigma modulator and demodulator required to build up a single channel codec, has been designed to meet CCITT requirements G711/G712 (1972).

The AY-3-9900 is subject to a License agreement with the British Post Office and Patents Pending.

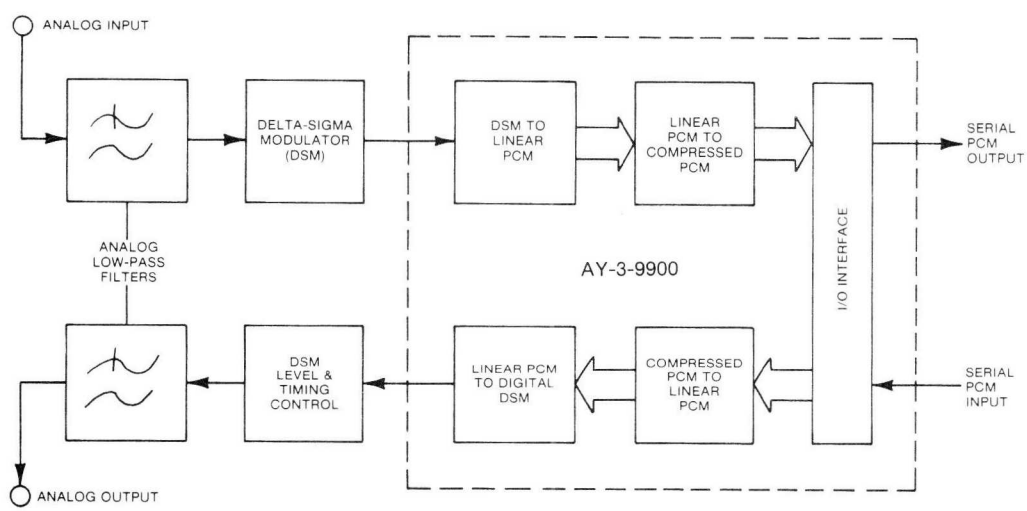


Fig.1 BLOCK DIAGRAM OF A COMPLETE CODEC.

TELECOM

CIRCUIT DESCRIPTION

The AY-3-9900 consists of two autonomous logic systems, designated in this specification as encoder and decoder. The encoder provides the necessary logic for the digital conversion of a delta-sigma encoded pulse density signal at 2048 kbit/sec into standard 8 ksample/sec 8 bit compressed PCM codewords. The decoder provides the necessary logic for the digital conversion of standard 8 bit compressed PCM characters at 8ksample/sec into a delta-sigma encoded pulse density signal at 2048 kbit/sec. Serial PCM input/output interfaces are also provided with facilities for a data rate of 64 to 2048 kbit/sec to enable its use in either a single channel system or a standard 30 channel TDM environment. For the necessary timing information to clarify this section reference should be made to the waveform diagrams, Figs. 5a, 5b, and 5e.

The encoder logic, operating continuously on the delta-sigma input pulse train, will generate a corresponding compressed PCM codeword every 125μs; with alternate digit inversion being provided if required by appropriate use of the ADI control input. A timing vector pulse (ETV) of nominal width equal to one encoder clock period, will define the required frame start time and should be repeated every 125μs to ensure correct synchronization.

If the mode select (MS) input is connected high then the 8 bit PCM codeword will be transmitted serially at a rate of 64 kbit/sec at which speed each codeword will occupy the full 125μs frame period for transmission, with the leading edge of the first bi occurring at a time defined by the ETV pulse.

Alternatively, if the MS input is left open circuit or connected low, the serial PCM transmission will be under the control of an externally generated shift clock (SCE) which can vary in frequency from 64kHz to 2048kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGBI input.

With the MS input connected high, an input PCM bit stream at 64 kbit/sec will be accepted by the decoder logic under the control of internal clocks generated from the CLKD signal. Because of delays through the transmission network, normally under the control of transmission switches, the input pulse stream may be delayed in time by number of digit periods from the original pulse stream as transmitted. To allow for this, a discrete delay of 0 to 3 digit periods can be selected by the control inputs DS1 and DS2 which results in a controlled shift of decoder timing in order to re-align bit 1 in its correct position in the input register. Alternatively, if the MS input is left open circuit or connected low the decoder input interface will be under the control of externally generated waveforms in which case it requires an input shift clock (SCD) and timing waveform (DTW) to define the time when bit 1 of the input codeword occupies its correct position in the input register. In this mode, the device will accept an input PCM stream at up to 2048 kbit/sec, with any signalling bits present in this signal being extracted via the SGBO output.

Upon receipt of a compressed PCM codeword, the decoder logic will first remove alternate digit inversions if necessary (under the control of the ADI input) after which the codeword will be linearized. A digital delta-sigma modulator will then generate a delta-sigma bit stream at 2048 kbit/sec for external decoding to produce the required analog signal.

All inputs and outputs of the AY-3-9900 are directly compatible with standard TTL (driving capacitive loads) or CMOS.

INPUT/OUTPUT FUNCTIONS

Supplies:

V_{SS}	GND
V_{CC}	+5V
V_{DD}	+9V

DC Control Signals:

MS — Mode Select — Selects between internal and external PCM I/O interface timing
Logic 0 = external
Logic 1 = internal
A resistor is connected internally between this input and V_{SS}.

ADI — Alternate-digit-inversion control – Selects ADI or no ADI
Logic 0 = no ADI
Logic 1 = ADI
A resistor is connected internally between this input and V_{SS}.

DS1, DS2 — Decoder delay select — A two bit binary word to select the required digit delay between encoder and decoder.

DS1	DS2	Digit Delay
0	0	0
0	1	1
1	0	2
1	1	3

A resistor is connected internally between each input and V_{SS}.

A/μ — Companding characteristic select-selects either A law or μ law
Logic 0 = A law
Logic 1 = μ law
A resistor is connected internally between this unput and V_{SS}.

CLOCKS & AC CONTROL SIGNALS

CLKE — Encoder main clock — 2.048 MHz clock signal

CLKD — Decoder main clock — 2.048 MHz clock signal

SCE — Encoder shift clock — Used to control the output of serial PCM data from the encoder (when MS=0)

SCD — Decoder shift clock — Used to control the input of serial PCM data to the decoder (when MS=0)

ETV — Encoder timing vector — A pulse defining the beginning of each frame, used to maintain encoder timing.

DTW — Decoder timing waveform — A pulse used to indicate to the decoder when the input PCM stream is in the input register (only required when external shift clocks are used).

DSMR — Delta-sigma reset — a pulse used to reset the digital delta-sigma modulator during testing only. Should be tied to ground during normal operation.

ENCODER OPERATIONAL INPUTS & OUTPUTS

DSMI — Delta-Sigma modulated input signal — Input to the encoder from the delta-sigma modulator.

SRF — Spectral redistribution function — 8kHz Output signal used to operate on the delta-sigma modulator to reduce low frequency quantization noise.

SGN — Sign bit output — Sign bit from the encoder, used to operate on the delta-sigma modulator for DC alignment.

SGBI — Signalling bit input — facility for adding signalling bit(s) to the output PCM stream. (MS = 0).

PCMO — PCM output — Serial PCM output under the control of the encoder shift clock (MS = 0) or the encoder main clock (MS=1).

DECODER OPERATIONAL INPUTS AND OUTPUTS

PCMI — PCM input — Serial PCM input under the control of the decoder shift clock (MS = 0) or the decoder main clock (MS=1).

SGBO — Signalling bit output — Serial output for extracting signalling bit(s) from the incoming PCM stream.

DSMO — Delta-sigma modulated output signal — Output pulse stream from the decoder.

A SINGLE CHANNEL PCM CODEC

The block schematic of a single channel Codec using the AY-3-9900 is shown in Fig. 1. It consists of a band limiting low pass filter followed by a delta-sigma modulator which, by sampling at a rate of 2048kHz provides a highly over-sampled, waveform-tracking A/D conversion. The bit stream produced by this modulator at 2048 kbits, is then converted into 8 bit compressed PCM code words at the standard rate of 8 ksample/sec; which, after conversion into serial format is transmitted serially at a bit rate of 64 kbit/sec. By the application of external timing signals, the PCM output transmission rate can be increased to allow for multiplexing in a burst format, with a maximum bit rate of 2048 kbit/sec.

The PCM input interface will accept either a 64 kbit/sec bit stream or, by the application of external timing signals, a bit rate of up to 2048 kbit/sec in a burst format. This input PCM stream will be converted into a delta-sigma modulated pulse stream at 2048 kbit/sec, from which the original analog signal can be recovered by the use of a low pass filter,cutting off just above the highest signal frequency to be recovered (3.4kHz).

The transition times and voltage levels of the delta-sigma modulated pulse streams are critical to the performance of the system. The delta-sigma modulator should therefore be constructed using TTL D-Types; with the delta-sigma modulated output pulse stream from the AY-3-9900 being clocked through a similar D-type before the analog signal is recovered.

Fig. 2 shows a more detailed diagram of the necessary external components (including component tolerances) required to realize a complete PCM Codec using the AY-3-9900. The response of such a Codec is shown graphically in Figs. 3 and 4.

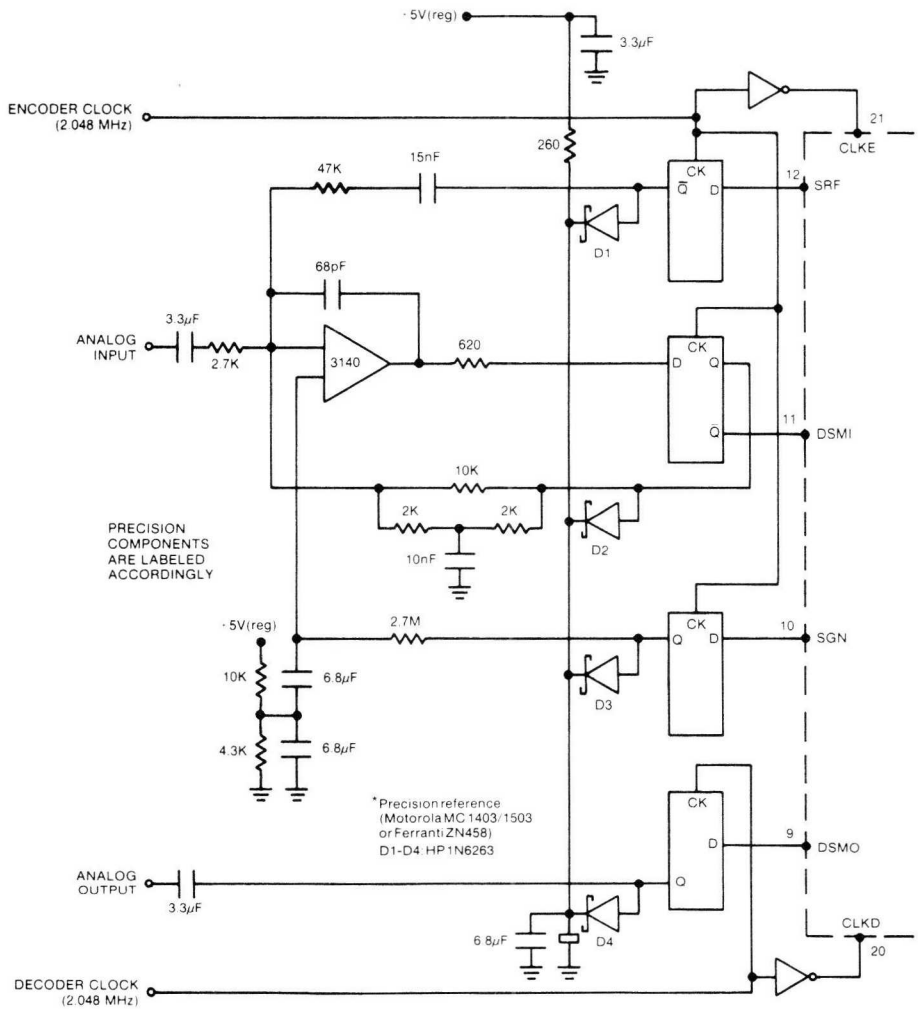


Fig.2 DETAILS OF DELTA-SIGMA MODULATOR, WITH DEMODULATOR LEVEL GENERATOR.

TYPICAL PERFORMANCE MEASUREMENTS: A-LAW

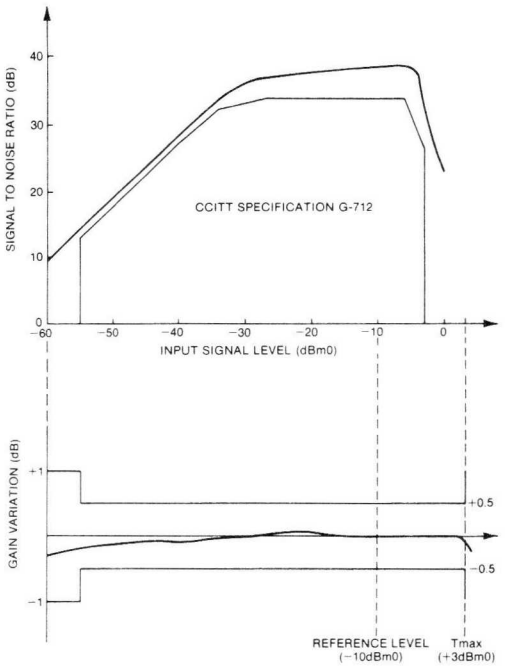


Fig. 3a SIGNAL TO NOISE RATIO (450-550Hz noise test signal)

Fig. 3b GAIN vs LEVEL LINEARITY (450-550 Hz noise test signal for level < -10dBm0; 850 Hz sine wave test signal for level > -10dBm0)

TYPICAL PERFORMANCE MEASUREMENTS: μ—LAW

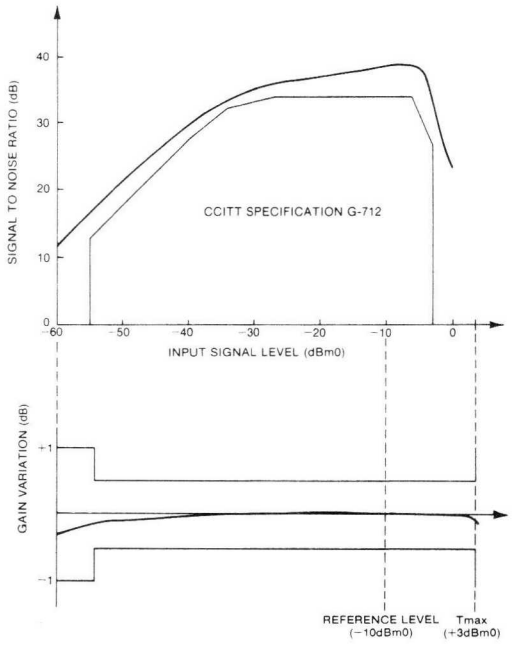


Fig. 3c SIGNAL TO NOISE RATIO (450-550 Hz noise test signal)

Fig. 3d GAIN vs LEVEL LINEARITY (450-550 Hz noise test signal for level < -10dBm0; 850Hz sine wave test signal for level > -10dBm0)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3V to +15V
Storage temperature range ..... −55°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (substrate voltage)
V_{CC} = +5V ± 5%
V_{DD} = +8.5V to +12.5V
Operating temperature (T_A) = −25°C to +75°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
DC Control Inputs					
Logic 1	4.75	5	10	V	Connect to V_{CC} or V_{DD}
Logic 0	0	–	0.4	V	Connect to V_{SS}
Pull down resistor	20	–	100	kΩ	Resistor to V_{SS}
CLOCKS (CLKD & CLKE)					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall Times	5	–	40	ns	0.4V-3V transition
Frequency	–	2.048	–	MHz	
Pulse Width	200	–	–	ns	Between 1.5V levels (Fig. 4c)
Input Capacitance	–	–	10	pF	
Other A.C. Control Signals					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall times	5	–	40	ns	0.4-3V transition
SCE/SCD pulse width	200	–	–	ns	between 1.5V levels
ETV width (tvw)	–	488	–	ns	See Fig. 4c.
edge variation (tvv)	–	–	100	ns	
DTW width	10	15.6	–	μs	One digit period (see Fig. 4c)
Input Capacitance	–	–	10	pF	
Operational Inputs					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall Times	5	–	40	ns	0.4-3V transition
Pulse Width	200	–	–	ns	between 1.5V levels
Input capacitance	–	–	10	pF	
Operational Outputs					
Logic 1	4	5	5.25	V	
Logic 0	0	–	0.4		
Logic 1 source current	100	–	–	μA	at V_O = 3V
Logic 0 sink current	1.6	–	–	mA	at V_O = 0.4V
Rise & Fall times	–	–	40	ns	0.4-3V transition (driving 15pF)
PCMO delay (from SCE edge)	40	100	140	ns	between 1.5V levels
Power Consumption	–	–	450	mW	at V_{CC}=5V, V_{DD}=9V

**Typical values are at +25°C and nominal voltages.

TELECOM

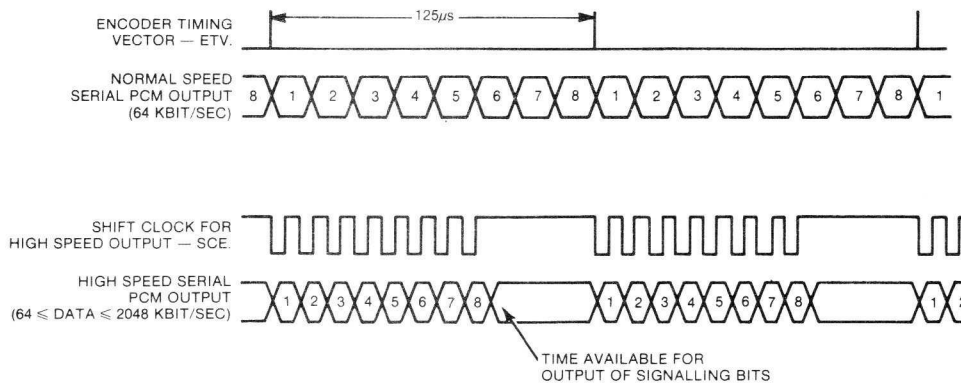


Fig.5a PCM OUTPUT TIMING

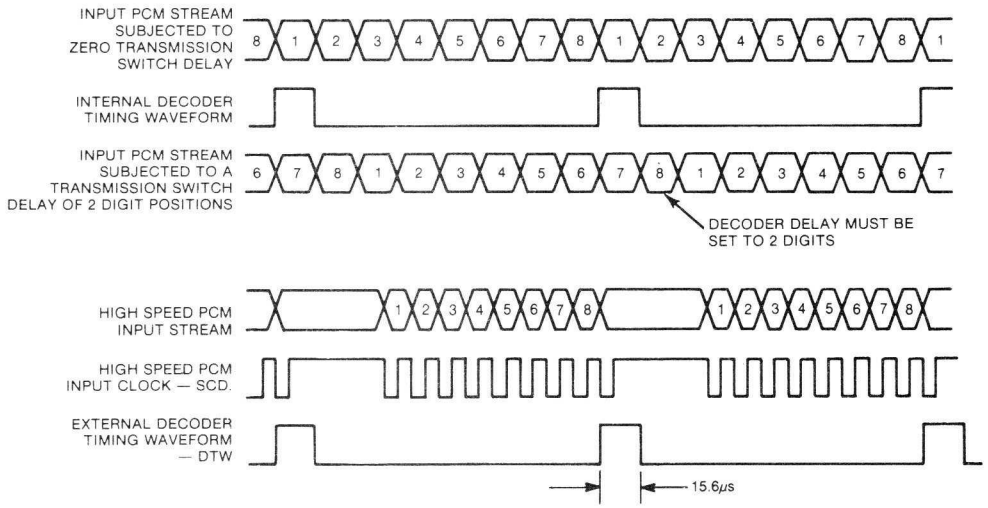


Fig.5b PCM INPUT TIMING

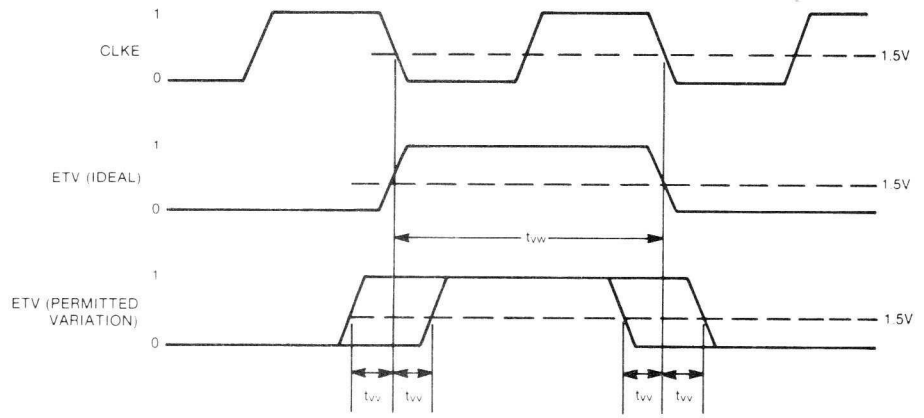


Fig.5c ENCODER TIMING VECTOR (ETV)

PRODUCT SUMMARY

Microcomputer Dialler

FEATURES

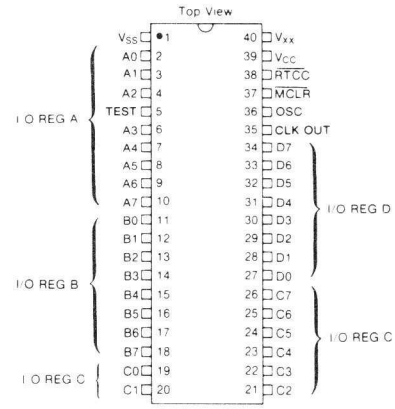
- Pushbutton Pulse Dialling (10 pps).
- Single button redial of last number.
- 12 Digit LED display.
- Access pause with manual release.
- Blinking digit indicating access pause.
- 16/32 number repertory dial with single button recall.
- Word "STORE" is displayed when storing numbers in repertory.
- Real time clock—hrs, mins, secs.
- Elapsed time/stopwatch.
- Optional interface with C593 five function calculator.

DESCRIPTION

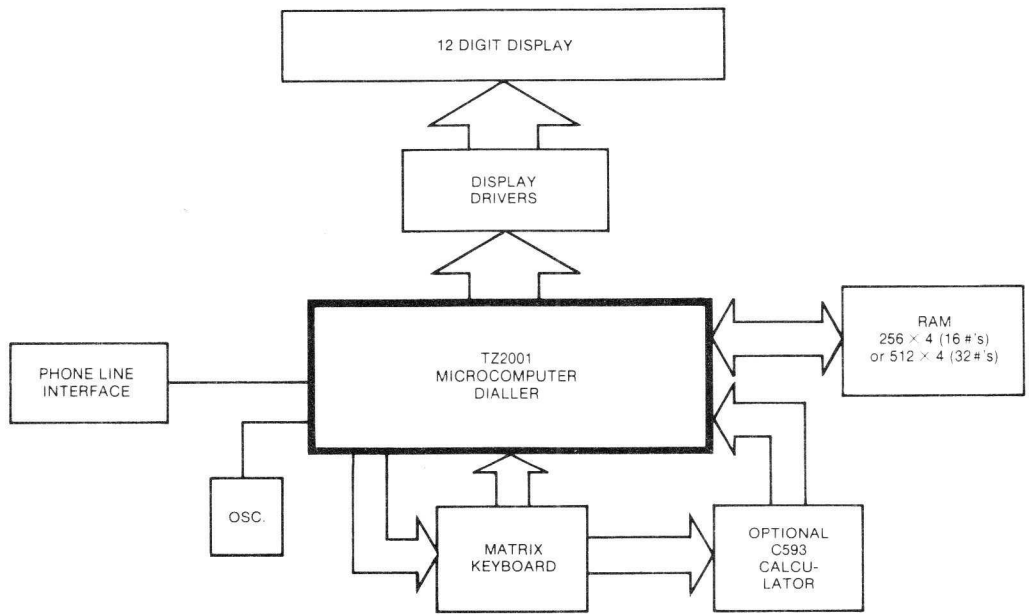
The TZ2001 is a single chip microcomputer with onboard ROM and RAM. All the software has been written, debugged and programmed into the chip. The customer has only to assemble the TZ2001 with the required external components in order to make a complete multifunction telephone controller.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



SYSTEM BLOCK DIAGRAM



TELECOM

MICRO ELECTRONICS

TELECOM HYBRIDS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
UNIVERSAL ACTIVE FILTERS	Generate any filter response by means of external connections	ACF 7032C	5-48
		ACF 7092C	5-48
LOW PASS FILTERS	PCM transmit filters.	ACF 7270C	5-52
		ACF 7272C	5-56
	PCM receive filters	ACF 7271C	5-54
		ACF 7273C	5-57
BAND PASS FILTERS	Full wave detector and a factory tunable four pole fixed bandwidth band pass filter.	ACF 7300C	5-58
		ACF 7301C	5-60
		ACF 7302C	5-62
	Detects and passes the 2600Hz signalling frequency	ACF 7310C	5-64
	DTMF/tone detection band pass filters.	ACF 7323C	5-66
		ACF 7363C	5-66
		ACF 7383C	5-66
BAND REJECTION FILTERS	Dial tone suppression, rejects frequencies of 350 and 440Hz.	ACF 7401C	5-68
	Rejects the 2600Hz signalling frequency.	ACF 7410C	5-69
BAND SEP FILTER	Isolates low and high groups of LTMF frequencies.	ACF 7711C	5-70

Universal Active Filters

FEATURES

- Low Pass, High Pass, Band Pass, and Band Reject responses from the same unit
- Independent control of Frequency, Q and Amplifier Gain
- External resistors need not temperature track internal NPO capacitors
- 10Hz. to 10kHz. operating frequency range
- 0.5 to 50 adjustable Q range

DESCRIPTION

The schematic diagram for the ACF 7032C/7092C is shown in Figure 1. The filter is composed of 4 operational amplifiers. The first three form the basic state variable configuration (triad) and the fourth can be utilized for increased gain or in the biquadratic configuration with the addition of external components. Two filter inputs are provided; a non-inverting input and an inverting input.

In the Triad configuration, amplifier A_1 is a summing amplifier providing the high pass output, amplifiers A_2 and A_3 are integrators providing band pass and low pass outputs. The external resistors establish the operating parameters for each filter mode. R_1 and R_2 determine the resonant frequency (Fn). R_7 and R_3 or R_7 and R_8 determine the values for gain and Q.

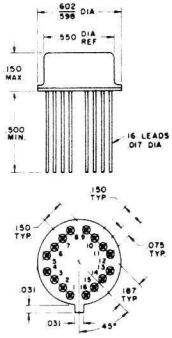
APPLICATIONS

General Instrument Hybrid universal active filters are low cost units that can be used to generate any filter response. Some common applications for these filters are found in sonar systems, telephone and paging systems, navigation systems, modems, transducers, biomedical measuring systems, process control equipment, data acquisition systems, radar systems, audio signal processing equipment and seismology.

PIN CONFIGURATIONS

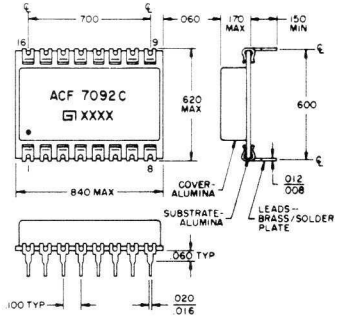
16 LEAD TO -8
ACF 7032C

PIN	FUNCTION
1	A4 (+IN)
2	VO
3	VLP
4	NC
5	A3 (—IN)
6	NC
7	GND
8	A2 (—IN)
9	VBP
10	V+
11	NC
12	A1 (+IN)
13	VHP
14	A1 (—IN)
15	V—
16	A4(—IN)



16 LEAD DUAL IN LINE
ACF 7092C

PIN	FUNCTION
1	A1(+IN)
2	A1 (—IN)
3	VHP
4	V+
5	VLP
6	A4 (+IN)
7	A3 (—IN)
8	NC
9	GND
10	A4 (—IN)
11	VO
12	V—
13	VBP
14	A2 (—IN)
15	NC
16	NC



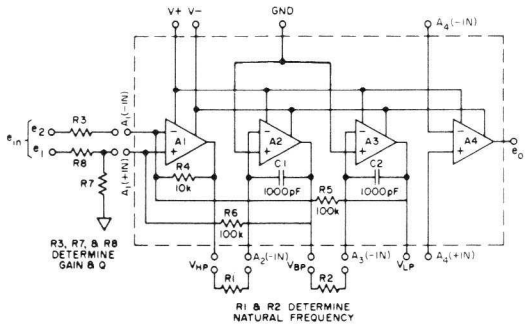


Fig. 1 SCHEMATIC

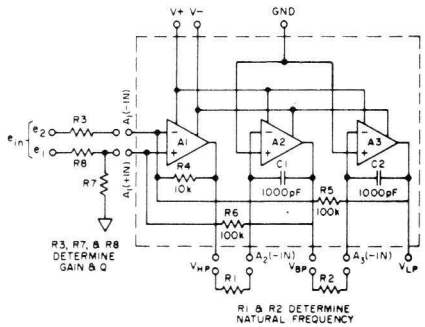


Fig. 2 TRIAD CONFIGURATION

ACTIVE FILTER DESIGN WITH UNIVERSAL FILTERS

TRIAD TRANSFER FUNCTIONS

The Triad configuration illustrated in Figure 2 gives transfer functions at the various points, HP, BP, and LP as shown in Table 1 for infinite gain band width operational amplifiers.

Table 1 TRANSFER FUNCTIONS

$$G_{HP}(s) = \frac{V_{HP}}{e_{IN}} = \frac{G_\infty S^2}{S^2 + \frac{Wn}{Q}S + Wn^2}$$ HIGH PASS

$$G_{BP}(s) = \frac{V_{BP}}{e_{IN}} = \frac{G_o \frac{Wn}{Q} S}{S^2 + \frac{Wn}{Q}S + Wn^2}$$ BAND PASS

$$G_{LP} = \frac{V_{LP}}{e_{IN}} = \frac{G(O)Wn^2}{S^2 + \frac{Wn}{Q}S + Wn^2}$$ LOW PASS

Fn = $Wn/2\pi$ = Natural or corner frequency for low or high pass outputs. Center frequency for band pass output.

S = Transform variable

G_∞ = Gain at infinite frequency (high pass)

G_o = Gain at center frequency (band pass)

$G_{(O)}$ = Gain at zero frequency (low pass)

$$Q = \frac{\text{Center frequency}}{\text{Bandwidth}}$$ BAND PASS

$$Q = \frac{\text{Gain at Natural Frequency}}{\text{Gain at infinite Frequency}}$$ HIGH PASS

$$Q = \frac{\text{Gain at Natural Frequency}}{\text{Gain at DC}}$$ LOW PASS

DESIGN EQUATIONS

The design equations for the transfer functions listed in Table 1 are:

$$Wn = \sqrt{a_3 W_1 W_2} \qquad W_1 = \frac{1}{R_1 C_1} \quad W_2 = \frac{1}{R_2 C_2}$$

$$Q = \left[\frac{1}{a_2 (1 + a_4 + a_3)}\right]\sqrt{\frac{a_3 W_2}{W_1}} \qquad a_1 = \frac{1}{1 + \frac{R_8}{R_6} + \frac{R_8}{R_7}}$$

$$a_2 = \frac{1}{1 + \frac{R_6}{R_7} + \frac{R_6}{R_8}} \quad a_3 = \frac{R_4}{R_5} \quad a_4 = \frac{R_4}{R_3}$$

	Non-Inverting Figure 3	Inverting Figure 4
G_∞	$a_1 (1 + a_3 + a_4)$	$-a_4$
G_o	$-a_1/a_2$	$\frac{a_4}{a_2 (1 + a_4 + a_3)}$
G(O)	$\frac{a_1 (1 + a_3 + a_4)}{a_3}$	$-a_4/a_3$

Note:
Since operational amplifiers have finite gain-bandwidths, the Q will be greater than calculated. A correction factor will be required and will operate on the desired Fn Q product. See Step #1 of Triad tuning procedure.

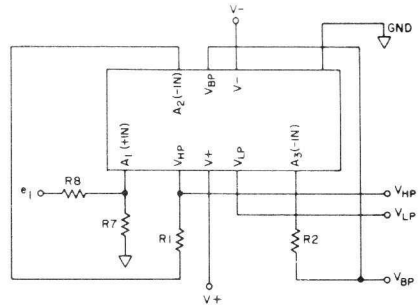


Fig. 3 NON-INVERTING CONFIGURATION

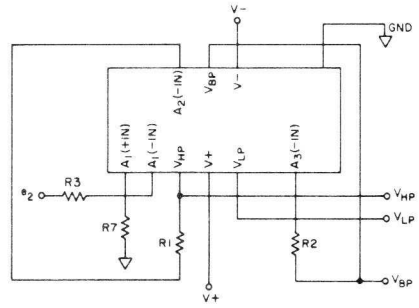


Fig. 4 INVERTING CONFIGURATION

TRIAD TUNING PROCEDURE

The following four step tuning procedure allows the selection of the external resistors R_1, R_2, R_7 and R_3 or R_8. The procedure is based on first selecting an output function (low-pass, band-pass or high-pass) and the inverting or non-inverting configuration. If other gains are desired the uncommitted operational amplifier can be used.

Step #1: Determine Design Q

Calculate the product of the desired Fn and Q. If this product exceeds 10,000 refer to Figure 5 to obtain the corresponding design FnQ. Divide the design FnQ product by Fn to determine the design Q for all subsequent calculations. The design Q now includes the effects of operational amplifier finite gain bandwidths.

If the desired FnQ product is less than 10,000, use the desired Q as the design Q for all subsequent calculations. The operational amplifier's finite gain-bandwidth in this lower FnQ region has a second order effect on the Q and can be ignored.

Step #2: Calculate R_3 or R_8 as a Function of Design Q

R_3 or R_8 can be calculated from the equations listed in Table II.

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Table II R_8 OR R_3 CALCULATION

Configuration	Non-Inverting Figure 3	Inverting Figure 4
Low-Pass	$R_8 = \frac{316k\Omega}{Q\ design}$	$R_3 = 100k\Omega$
Band-Pass	$R_8 = \frac{Q\ desired\ (100k)}{Q\ design}$	$R_3 = Q\ design\ (31.6k\Omega)$
High-Pass	$R_8 = \frac{31.6k\Omega}{Q\ design}$	$R_3 = 10k\Omega$

Step #3: Calculate R_1 and R_2 as a Function of Fn

For basic unity gain configuration, $R_1 = R_2$.

$$R_1 = R_2 = \frac{5.04 \times 10^7}{Fn}$$

LOW FREQUENCY OPERATION

For very low frequencies (fn $\leq$ 50Hz) additional capacitance can be used to shunt the internal integrating capacitors from pins 5 to 7 and 13 to 14. R_1 and R_2 are then calculated as follows:

$$R_1 = R_2 = \frac{1}{2\pi Fn} \sqrt{\frac{R_4}{R_5 C_1 C_2}}$$

Step #4: Calculate R_7 as a Function of Design Q

R_7 can be calculated from the equations listed in Table III

Table III R_7 CALCULATIONS

Configuration	Non-Inverting Figure 3	Inverting Figure 4
Low-Pass	$R_7 = \frac{100k\Omega}{3.16\ (Q\ design) - 1}$	$R_7 = \frac{100k\Omega}{3.8\ (Q\ design) - 1}$
Band-Pass	$R_7 = \frac{100k\Omega}{3.48\ (Q\ design) - 2}$	$R_7 = \frac{100k\Omega}{3.48\ (Q\ design)}$
High-Pass	$R_7 = \frac{100k\Omega}{0.32\ (Q\ design) - 1}$	$R_7 = \frac{100k\Omega}{6.64\ (Q\ design) - 1}$

BIQUAD TRANSFER FUNCTION

The BIQUAD configuration for generating Cauer or Band Reject responses is shown in Figure 6.

The transfer function is:

$$\frac{e_o}{e_{IN}} = A \left[\frac{S^2 + aWnS + bWn^2}{S^2 + \frac{Wn}{Q} S + Wn^2} \right]$$

The parameters for the Transmission Zeros (numerator) are given by:

$$a = \frac{R_{13}}{R_{14}} \sqrt{\frac{R_5}{R_4}} \qquad A = -\left(\frac{R_{14}}{R_{13}}\right) \times \left(\frac{R_4}{R_5}\right) \times G(O)$$

$$b = \frac{R_{13}}{R_{11}} \times \frac{R_5}{R_4}$$

provided that $R_{12} R_{14} = R_{15} \left(\frac{R_{11} R_{13}}{R_{11} + R_{13}} \right)$

The tuning procedure for Wn and Q is the same as in the TRIAD configuration.

A Band Reject filter can be obtained by making Constant (b) = 1 and R_{12} infinite which makes the Constant (a) = zero. The transfer function then becomes:

$$\frac{e_o}{e_{IN}} = \frac{S^2 + Wn^2}{S^2 + \frac{WnS}{Q} + Wn^2}$$

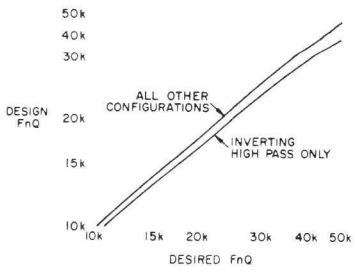


Fig. 5 FnQ CORRECTION

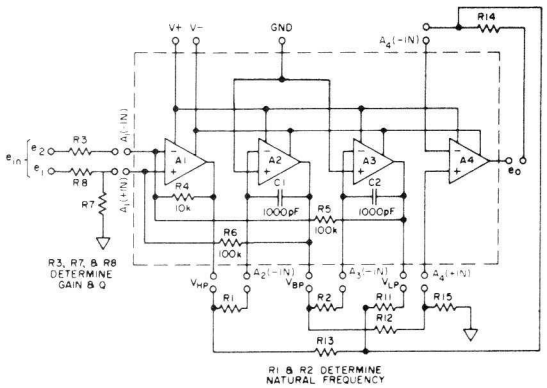


Fig. 6 BIQUAD CONFIGURATION

PERFORMANCE SPECIFICATIONS

MAXIMUM RATINGS

Supply Voltages ..... + 18 V
Supply Current (± 15 Volt Supplies) ..... ± 12mA
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +125°C

ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, these parameters apply over a temperature range of 0°C to +70°C with ± 15 VDC supplies

Characteristic	Min	Typ	Max.	Units	Conditions
FnQ Product	5	—	50,000	—	
Fn Range	10	—	10,000	Hz	Self Resonant Frequency
Fn Accuracy	—	± 1.5	±2.5	%	Note 1, T_A = 25°C
Fn Temp. Coeff.	—	± 40	±75	ppm/°C	Note 2
Q Range	0.5	—	50	—	
Q Accuracy	—	± 7	—	%	
Q Temp. Stability	—	± FnQ×10^{-6}	—	%	0°C ≤ T_A ≤ 70°C
Pass band gain	1	—	10	—	Note 3
Input offset voltage	—	2	10	mV	T_A =25°C
	—	—	15	mV	0°C ≤ T_A ≤ 70°C
Input offset current	—	5	200	nA	T_A = 25°C
	—	—	300	nA	0°C ≤ T_A ≤ 70°C
Input bias current	—	40	500	nA	T_A = 25°C
	—	—	800	nA	0°C ≤ T_A ≤ 70°C
Input voltage range	± 12	± 14	—	V	
Input Resistance	0.3	5	—	MΩ	
Large Signal Voltage Gain	20,000	300,000	—	—	RL ≥ 2K, Vo = ± 10V, T_A = 25°C
	15,000	—	—	—	RL ≥ 2K, Vo = ± 10V, 0°C < T_A < 70°C
Supply Voltage Rejection Ratio	—	30	300	μV/V	
Output Resistance	—	—	100	Ω	
Load Resistance	1,000	—	—	Ω	
Output Voltage Swing	—	—	20	V P-P	
	—	—	8	V P-P	Fn = 10Hz to 1kHz, Band pass
	—	—	2	V P-P	Fn = 10Hz to 1kHz, High pass
	—	—	8	V P-P	Fn = 10kHz, Low pass
	—	—	3	V P-P	Fn = 10kHz, Band pass
	—	—	0.8	V P-P	Fn = 10kHz, High pass
Common mode rejection ratio	70	90	—	dB	

Note 1: The 25°C Fn accuracy is determined by the internal capacitor tolerance (± 1%), and the R_4/R_5 tolerance (± 2%) and does not include the tolerance of the external resistors R1 and R2.

Note 2: The internal capacitors have a temperature coefficient of ±30ppm/°C. The remaining portion of the temperature coefficient is due to the change of the operational gain band width products over temperature.

Note 3: Gain greater than 1 can be provided with the uncommitted amplifier.

PCM Transmit Low Pass Filter

FEATURES

- Pass band ripple: ±0.125 dB, from 300 to 3kHz, 0° to 70°C.
- Stop band attenuation: 32 dB, 4.2kHz to 100kHz.
- Insertion Loss: 0 dB
- Wide power supply range: ±12VDC to ±15VDC

DESCRIPTION

The ACF 7270C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ±.125 dB ripple to 3kHz and be 32 dB down at 4.2kHz with equal rejection out to 100kHz. The filter is designed to be used in PCM transmit applications.

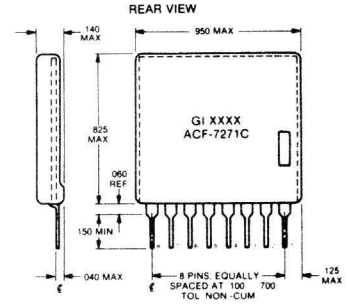
MAXIMUM RATINGS

V_{CC} ..... ±18VDC
Input Voltage ..... ±15VDC
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
$V_{CC} = +12$ to $+15$VDC
$-V_{CC} = -12$ to -15VDC

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Input	5	N.C.
2	N.C.	6	V_{CC}
3	GND	7	$-V_{CC}$
4	N.C.	8	Output

Characteristic	Min	Typ	Max	Units	Conditions
Gain	−.125	0	+.125	dB	f = 1kHz
Passband ripple	−.125	0	+.125	dB	f = 300-3kHz, ref 1kHz
Passband response	−.5	0	+.2	dB	f = 3kHz-3.4kHz, ref 1kHz
Transition atten.	15	18	—	dB	f = 4kHz, ref 1kHz
Stop band atten.	32	35	—	dB	f = 4.2kHz
Low freq 3dB pt	20	40	50	Hz	ref. 1kHz
Differential delay	—	78	90	μs	1kHz, 2.6kHz
Output noise	—	0	6	dBrnc0	input grounded
Distortion	—	0.1	0.25	%	1kHz
Output swing	10	12	—	Vp-p	RL = 2K, $V_{CC} = +15$VDC, $-V_{CC} = -15$VDC
Input impedance	100k	1meg	—	Ω	DC to 10kHz
Output impedance	—	1	5	Ω	DC to 10kHz
Supply current	—	10	15	mA	

NOTES:

1. Specifications apply with an input of 0dBM Ref 600Ω.
2. To obtain the full signal range, the filter should be driven from a source with a nominal DC voltage of 0V.
3. The source must provide a DC path to ground of not more than 10K.

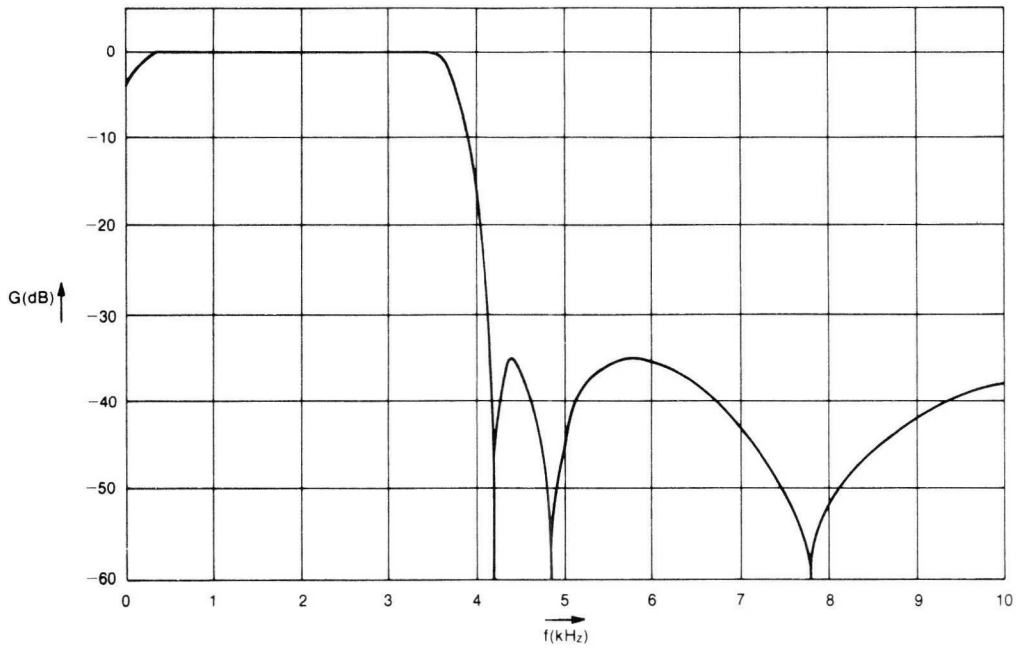


Fig.1 TYPICAL FREQUENCY RESPONSE

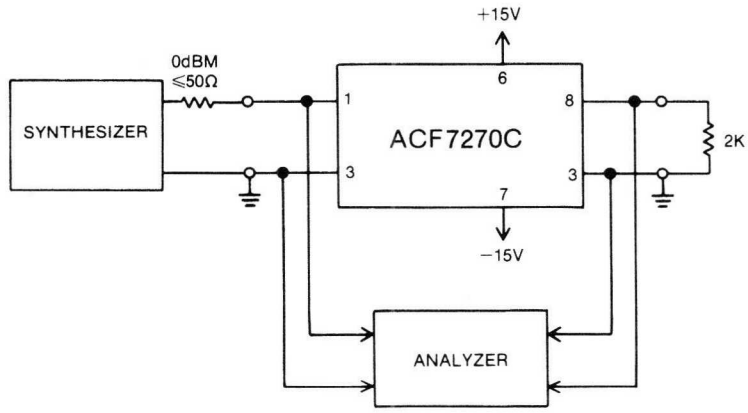


Fig. 2 TEST CIRCUIT

PCM Receive Low Pass Filter

FEATURES

- Pass band ripple: ±0.125 dB, from 300 to 3kHz, 0° to 70°C.
- Stop band attenuation: 32 dB, 4.2kHz to 100kHz.
- Insertion Loss: 0 dB
- Wide power supply range: ±12VDC to ±15VDC

DESCRIPTION

The ACF 7271C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ± .125 dB ripple to 3kHz and be 32 dB down at 4.2kHz with equal rejection out to 100kHz. The filter is designed to be used in PCM receive applications.

MAXIMUM RATINGS

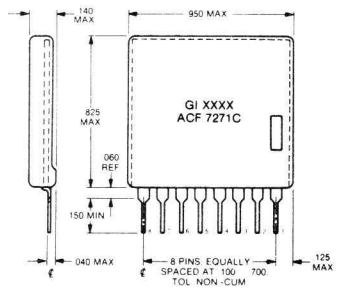
V_{CC} ..... ±18VDC
Input Voltage ..... ±15VDC
Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
$V_{CC} = +12$ to $+15$VDC
$-V_{CC} = -12$ to -15VDC

PACKAGE INFORMATION
PIN CONFIGURATION

REAR VIEW



PIN	FUNCTION	PIN	FUNCTION
1	Internal Connection	5	V_{CC}
2	Input	6	N.C.
3	GND	7	$-V_{CC}$
4	N.C.	8	Output

Characteristic	Min	Typ	Max	Units	Conditions
Gain	−.125	0	+.125	dB	f = 1kHz
Passband ripple	−.125	0	+.125	dB	f = 300-3kHz, ref 1kHz
Passband response	−.5	0	+.2	dB	f = 3kHz-3.4kHz, ref 1kHz
Transition atten.	15	18	—	dB	f = 4kHz, ref 1kHz
Stop band atten.	32	35	—	dB	f = 4.2kHz
Differential delay	—	85	95	μs	1kHz, 2.6kHz
Output noise	—	0	6	dBrnc0	input grounded
Distortion	—	0.1	0.25	%	1kHz
Output swing	10	12	—	Vp-p	RL = 2K, $V_{CC} = +15$VDC, $-V_{CC} = -15$VDC
Input impedance	130	140	—	kΩ	DC to 10kHz
Output impedance	—	1	5	Ω	DC to 10kHz
Supply current	—	10	15	mA	

NOTES:

1. Specifications apply with an input of 0dBM Ref 600Ω.
2. To obtain the full signal range, the filter should be driven from a source with a nominal DC voltage of 0V.
3. The source must provide a DC path to ground of not more than 10K.
4. Frequency response data is multiplied by sin x/x response.

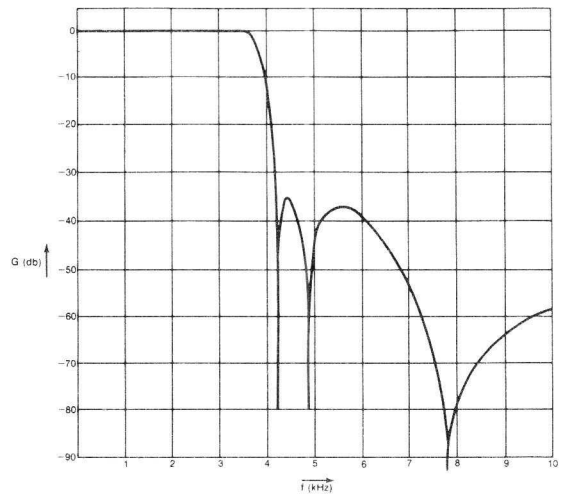


Fig. 1 TYPICAL FREQUENCY RESPONSE MULTIPLIED BY SIN X/X

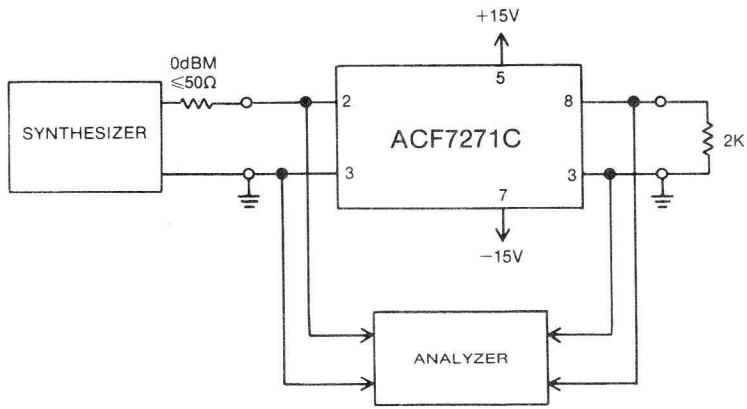


Fig.2 TEST CIRCUIT

PCM Transmit Low Pass Filter

FEATURES

- 0.53 inch high SIP configuration allows close board spacing.
- Insertion loss: 0dB nominal, adjustable with one external resistor.
- Pass band ripple: ±0.125 dB, from 300 to 3kHz, 0° to 70°C.
- Stop band attenuation: 32 dB, 4.2kHz to 100kHz.
- 60Hz Attenuation: 25dB
- Wide power supply range: ±12VDC to ±15VDC

DESCRIPTION

The ACF 7272C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ±.125 dB ripple to 3kHz and be 32 dB down at 4.2kHz with equal rejection out to 100kHz. The filter is designed to be used in PCM transmit applications.

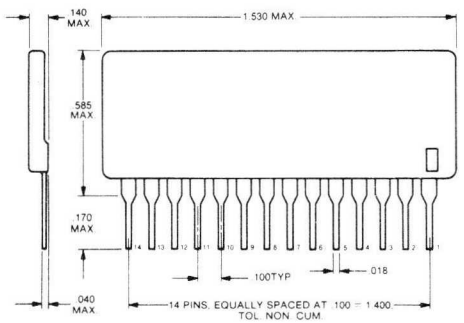
MAXIMUM RATINGS

V_{CC} ..... ±18VDC
Input Voltage ..... ±15VDC
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
$V_{CC} = +12$ to $+15$VDC
$-V_{CC} = -12$ to -15VDC

PACKAGE INFORMATION
PIN CONFIGURATION



PIN FUNCTION	PIN FUNCTION
1.	8.
2.	9.
3.	10.
4.	11.
5.	12.
6.	13.
7.	14.

Not yet defined.

Characteristic	Min	Typ	Max	Units	Conditions
Gain	−.125	0	+.125	dB	f = 1kHz
Passband ripple	−.125	0	+.125	dB	f = 300-3kHz, ref 1kHz
Passband response	−.5	0	+.2	dB	f = 3kHz-3.4kHz, ref 1kHz
Transition atten.	15	18	—	dB	f = 4kHz, ref 1kHz
Stop band atten.	32	35	—	dB	f = 4.2kHz
60Hz rejection	—	25	—	dB	ref. 1kHz
Differential delay	—	—	—	μs	1kHz, 2.6kHz
Output noise	—	0	6	dBrnc0	input grounded
Distortion	—	0.1	0.25	%	1kHz
Output swing	10	12	—	Vp-p	RL = 2K, $V_{CC} = +15$VDC, $-V_{CC} = -15$VDC
Input impedance	100k	1meg	—	Ω	DC to 10kHz
Output impedance	—	1	5	Ω	DC to 10kHz
Supply current	—	10	15	mA	

NOTES:

1. Specifications apply with an input of 0dBM Ref 600Ω.
2. To obtain the full signal range, the filter should be driven from a source with a nominal DC voltage of 0V.
3. The source must provide a DC path to ground of not more than 10K.

PCM Receive Low Pass Filter

FEATURES

- Pass band ripple: ± 0.125 dB, from 300 to 3kHz, 0° to 70°C.
- Stop band attenuation: 32 dB, 4.2kHz to 100kHz.
- Insertion Loss: 0 dB
- Wide power supply range: ±12VDC to ±15VDC

DESCRIPTION

The ACF 7273C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ± .125 dB ripple to 3kHz and be 32 dB down at 4.2kHz with equal rejection out to 100kHz. The filter is designed to be used in PCM receive applications.

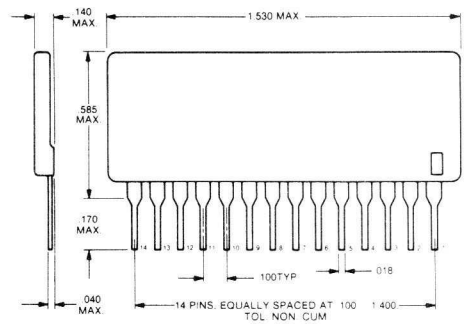
MAXIMUM RATINGS

V_{CC} ..... ±18VDC
Input Voltage ..... ±15VDC
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
$V_{CC} = +12$ to $+15$VDC
$-V_{CC} = -12$ to -15VDC

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Input	8	Output
2	Internal Connection	9	$-V_{CC}$
3	N.C.	10	N.C.
4	N.C.	11	Gain Adjust
5	N.C.	12	V_{CC}
6	N.C.	13	Output
7	N.C.	14	GND

Characteristic	Min	Typ	Max	Units	Conditions
Gain	−.125	0	+.125	dB	f = 1kHz
Passband ripple	−.125	0	+.125	dB	f = 300-3kHz, ref 1kHz
Passband response	−.5	0	+.2	dB	f = 3kHz-3.4kHz, ref 1kHz
Transition atten.	15	18	—	dB	f = 4kHz, ref 1kHz
Stop band atten.	32	35	—	dB	f = 4.2kHz
Differential delay	—	85	95	μs	1kHz, 2.6kHz
Output noise	—	0	6	dBrnc0	input grounded
Distortion	—	0.1	0.25	%	1kHz
Output swing	10	12	—	Vp-p	RL = 2K, $V_{CC} = +15$VDC, $-V_{CC} = -15$VDC
Input impedance	130	140	—	kΩ	DC to 10kHz
Output impedance	—	1	5	Ω	DC to 10kHz
Supply current	—	10	15	mA	

NOTES:

1. Specifications apply with an input of 0dBM Ref 600Ω.
2. To obtain the full signal range, the filter should be driven from a source with a nominal DC voltage of 0V.
3. The source must provide a DC path to ground of not more than 10K.
4. Frequency response data is multipled by sin x/x response.

TELECOM

ACF 7300C

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 20 dB minimum attenuation at stop band frequencies
- 0 dB Insertion loss in pass band
- Fixed band width filter
- Internal full wave detector

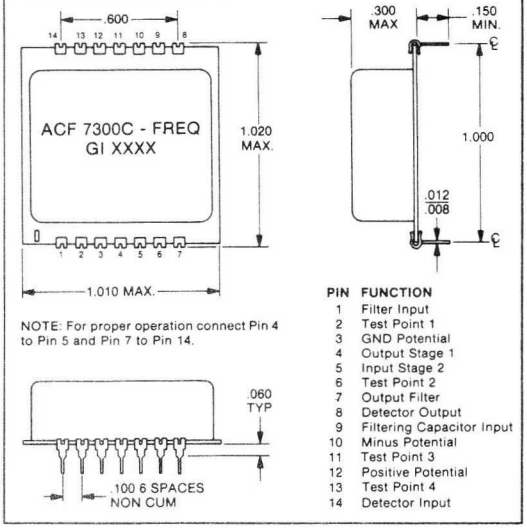
DESCRIPTION

The ACF 7300C consists of a four (4) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 540Hz to 1980Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14.

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	Test Point 3
12	Positive Potential
13	Test Point 4
14	Detector Input

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Filter Load Resistance = 5kΩ
Detector Load Resistance = 5kΩ
Source Impedance, Filter or Detector = 50Ω

Characteristic	Min.	Typ.	Max.	Units	Conditions
Filter					
Input Impedance	—	2	—	kΩ	
Voltage Gain					See Figure 1.
	—	0	0.5	±dB	Ideal Center Frequency (F_O)
	—	0	1.5	±dB	Pass Band (±10Hz from F_O)
	-20	—	—	dB	Stop Band (±110Hz from F_O)
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	Ω	
Detector					
Input Impedance	25	—	—	kΩ	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2.
Output Impedance	—	—	25	Ω	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	1.5	3.0	mA	

Standard factory tuned filters available with the following ideal center frequencies:
540Hz, 660Hz, 780Hz, 900Hz, 1020Hz, 1140Hz, 1380Hz, 1500Hz, 1620Hz, 1740Hz, 1860Hz, and 1980Hz. To order one of the above tuned filters, specify the device as follows; ACF 7300C - Frequency. e.g. ACF 7300C - 0540
Other factory tuned frequencies are available upon request and nominal set up charge.

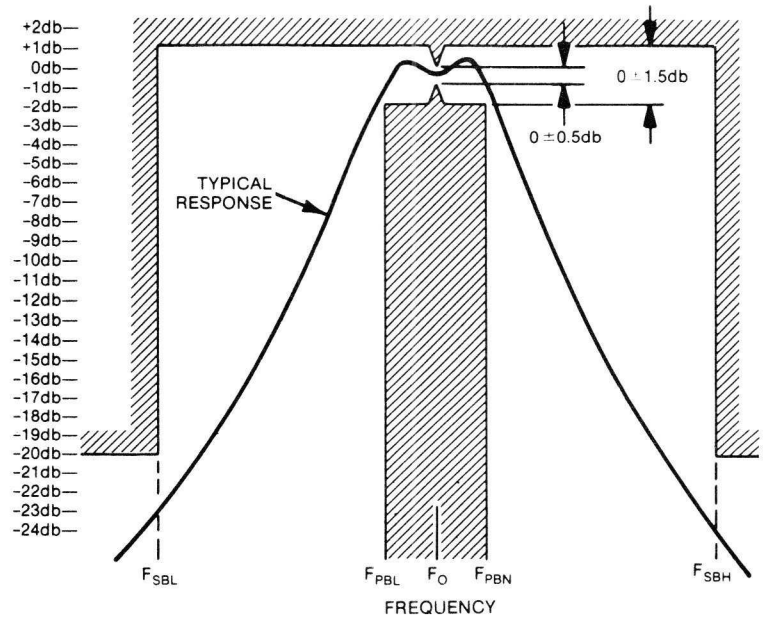


Fig.1 FREQUENCY RESPONSE

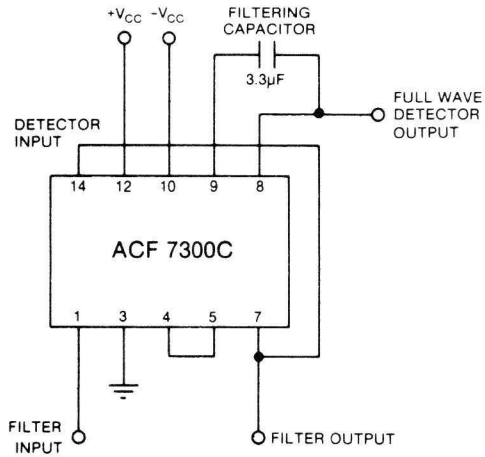


Fig.2 TYPICAL APPLICATION

Table I

Center Frequency (FO)(Hz)	Low Stop Band Frequency (FSBL)(Hz)	Low Pass Band Frequency (FPBL)(Hz)	High Pass Band Frequency (FPBH)(Hz)	High Stop Band Frequency (FSBH)(Hz)
540	430	530	550	650
660	550	650	670	770
780	670	770	790	890
900	790	890	910	1010
1020	910	1010	1030	1130
1140	1030	1130	1150	1250
1380	1270	1370	1390	1490
1500	1390	1490	1510	1610
1620	1510	1610	1630	1730
1740	1630	1730	1750	1850
1860	1750	1850	1870	1970
1980	1870	1970	1990	2090

ACF 7301C

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 0db Insertion loss in pass band
- 20db minimum attenuation at stop band frequencies
- Fixed band width filter
- Internal full wave detector

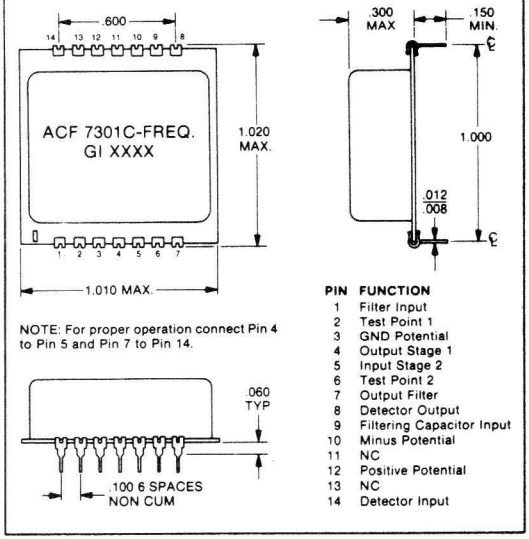
DESCRIPTION

The ACF 7301C consists of a four (4) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_o) range of 700Hz to 1700Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70° C

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14.

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	NC
12	Positive Potential
13	NC
14	Detector Input

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Load Resistance, Filter Output or Detector Output = 5k ohms
Source Impedance, Filter Input or Detector Input = 50Ω

Characteristic	Min	Typ	Max	Units	Conditions
Filter					
Input Impedance	—	2	—	kΩ	
Voltage Gain					See Figure 1
	—	0	0.5	±dB	Ideal Center Frequency (F_O)
	—	0	1.5	±dB	Pass Band (±15Hz from F_O)
	-20	—	—	dB	Stop Band (±185Hz from F_O)
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	Ω	
Detector					
Input Impedance	25	—	—	kΩ	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2.
Output Impedance	—	—	25	Ω	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	1.5	3.0	mA	

Standard factory tuned filters available with the following ideal center frequencies: 700Hz, 900Hz, 1100Hz, 1300Hz, 1500Hz, and 1700Hz. To order one of the above tuned filters, specify the device as follows; ACF 7301 C - Frequency. e.g. ACF 7301 C - 0700. Other factory tuned frequencies are available upon request and a nominal set up charge.

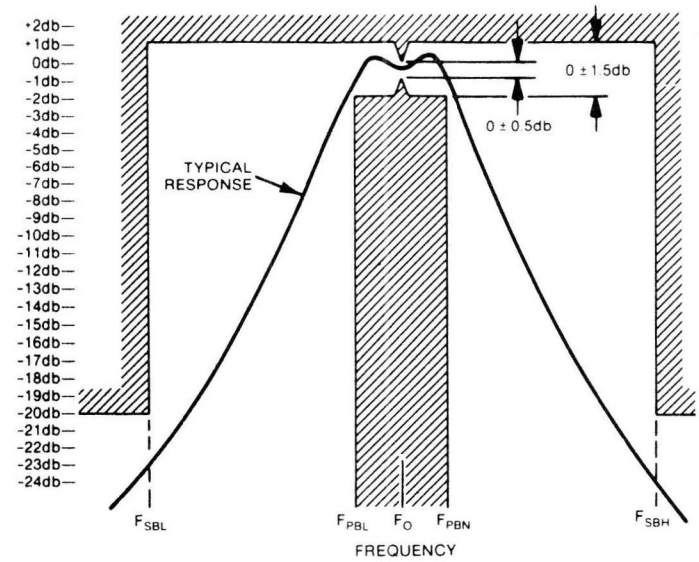


Fig.1 FREQUENCY RESPONSE

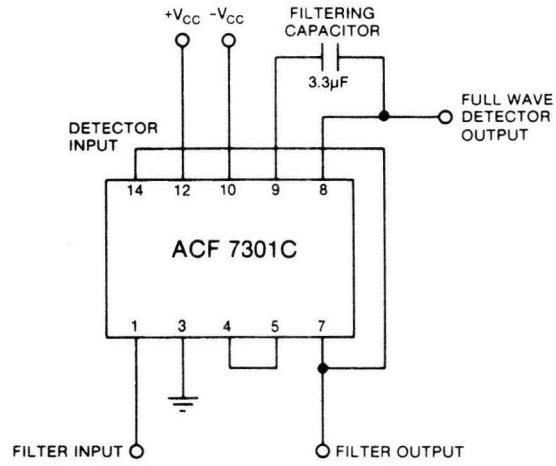


Fig.2 TYPICAL APPLICATION

TELECOM

TABLE 1

Center Frequency (FO) (Hz)	Low Stop Band Frequency (FSBL) (Hz)	Low Pass Band Frequency (FPBL) (Hz)	High Pass Band Frequency (FPBH) (Hz)	High Stop Band Frequency (FBBH) (Hz)
700	505	685	715	885
900	715	885	915	1085
1100	915	1085	1115	1285
1300	1115	1285	1315	1485
1500	1315	1485	1515	1685
1700	1515	1685	1715	1895

ACF 7302C

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 22dB minimum attentuation at stop band frequencies
- 0dB Insertion loss in pass band
- Fixed band width filter
- Internal full wave detector

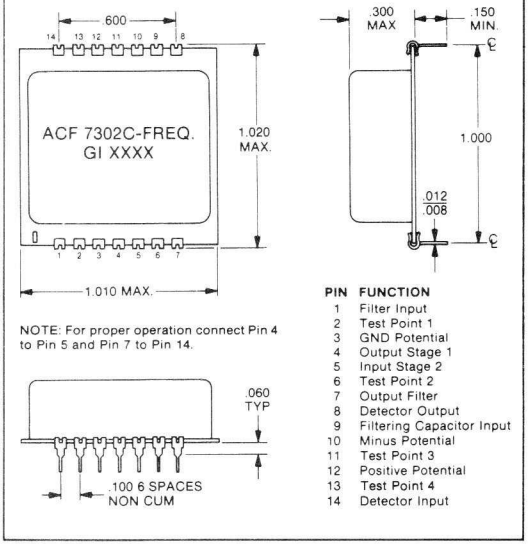
DESCRIPTION

The ACF 7302C consists of six (6) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 2280Hz to 3825Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70C

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14.

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	Test Point 3
12	Positive Potential
13	Test Point 4
14	Detector Input

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = 12 Volts
0°C to +70°C
Filter and Detector Load Resistance = 5k ohms
Filter and Detector Source Impedance = 50Ω

Characteristic	Min	Typ	Max	Units	Conditions
Filter					
Input Impedance	—	2	—	kΩ	
Voltage Gain					See Figure 1.
	—	0	0.5	±dB	Ideal Center Frequency (F_O)
	—	0	1.5	±dB	Pass Band (±15Hz from F_O)
	-22	—	—	dB	Stop Band (±120Hz from F_O)
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	Ω	
Detector					
Input Impedance	25	—	—	kΩ	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2.
Output Impedance	—	—	25	Ω	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	3.0	5.0	mA	

Standard factory tuned filters available with the following ideal center frequencies: 2280Hz, 2400Hz, 2600Hz. To order one of the above tuned filters, specify the device as follows: ACF 7320 C - Frequency. e.g. ACF 7302 C - 2280. Other factory tuned frequencies are available upon request and a nominal set up charge.

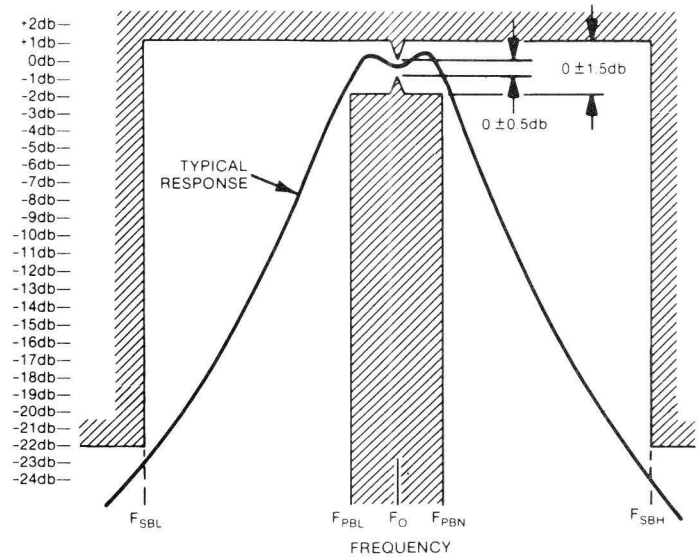


Fig.1 FREQUENCY RESPONSE

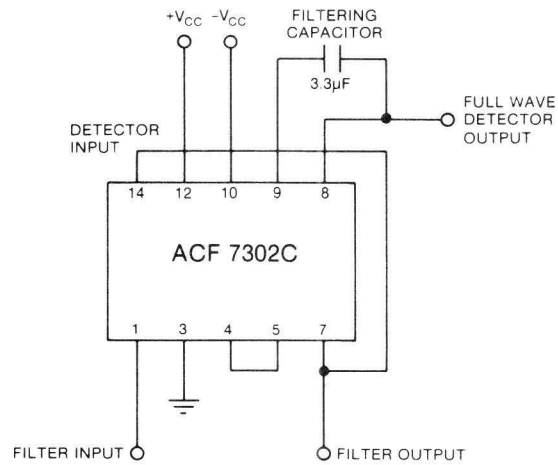


Fig.2 TYPICAL APPLICATION

TELECOM

Table I

Center Frequency (FO) (Hz)	Low Stop Band Frequency (FSBL) (Hz)	Low Pass Band Frequency (FPBL) (Hz)	High Pass Band Frequency (FPBH) (Hz)	High Stop Band Frequency (FBBH) (Hz)
2280	2160	2265	2295	2400
2400	2280	2385	2415	2520
2600	2480	2585	2615	2720
3825	3705	3810	3840	3945

2600Hz Band Pass Filter

FEATURES

- 0 Insertion Loss
- Low Power Dissipation
- Narrow Band Width
- High Out of Band Attenuation
- Can be operated with single-ended power system

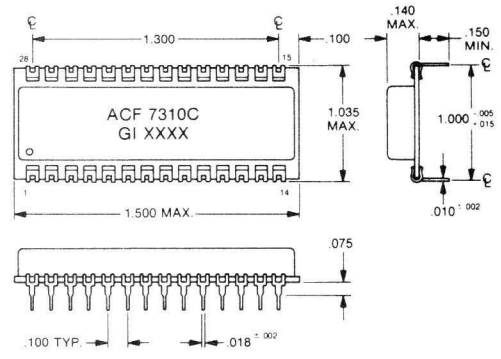
DESCRIPTION

The ACF 7310C is a linear hybrid band pass RC active filter. The ACF 7310C is a sharply tuned filter designed to detect and pass the 2600Hz signaling frequency. This filter provides for a minimum attenuation of 30 dB, plus and minus 200Hz from the ideal center frequency. The filter is self contained and requires no external components for proper operation. This filter is packaged in a dual in line configuration.

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	Input	10.	Stage 2 Input	20.	NC
2.	NC	11.	NC	21.	NC
3.	NC	12.	Stage 2 Output	22.	-12 VDC
4.	NC	13.	NC	23.	NC
5.	NC	14.	Output	24.	+12 VDC
6.	GND	15.	Stage 3 Input	25.	NC
7.	NC	16.	NC	26.	Stage 1 Output
8.	NC	17.	NC	27.	NC
9.	NC	18.	NC	28.	NC
		19.	NC		

NOTE: For proper operation connect Pin 26 to Pin 10, Pin 12 to Pin 15.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

V_{CC} = ±12 Volts
T_A = 25°C
R_S = 50
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-0.5	0	+0.5	dB	Ideal Center Frequency (F_O), 2600Hz
Frequency Response					Referenced from F_O Gain
	-70	—	—	dB	DC to 1600Hz
	-50	—	—	dB	2100Hz
	-30	—	—	dB	2400Hz
	-3	—	—	dB	2540Hz
	—	—	-3	dB	2560Hz
	—	—	-3	dB	2640Hz
	-3	—	—	dB	2660Hz
	-30	—	—	dB	2800Hz
	-50	—	—	dB	3100Hz
	-70	—	—	dB	3600Hz to 50kHz
Ripple	—	—	+0.5	dB	2541Hz to 2659Hz (Reference Fig. 1)
Input Impedance	25	—	—	kΩ	
Output Offset Voltage	—	—	20	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	1.0	%	V_{OUT} = 10 V_{PP}, Freq. = 2600Hz
Current Drain	—	—	10	mA	

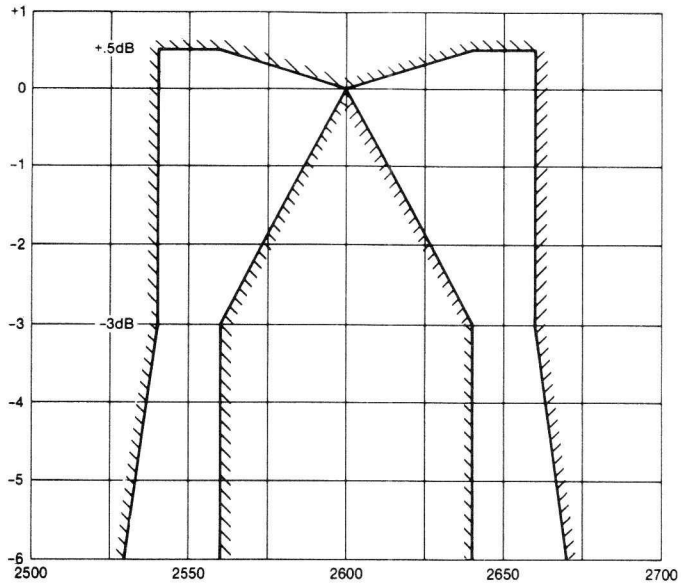


Fig.1 ACF 7310C PASS BAND ATTENUATION LIMITS EXPANDED

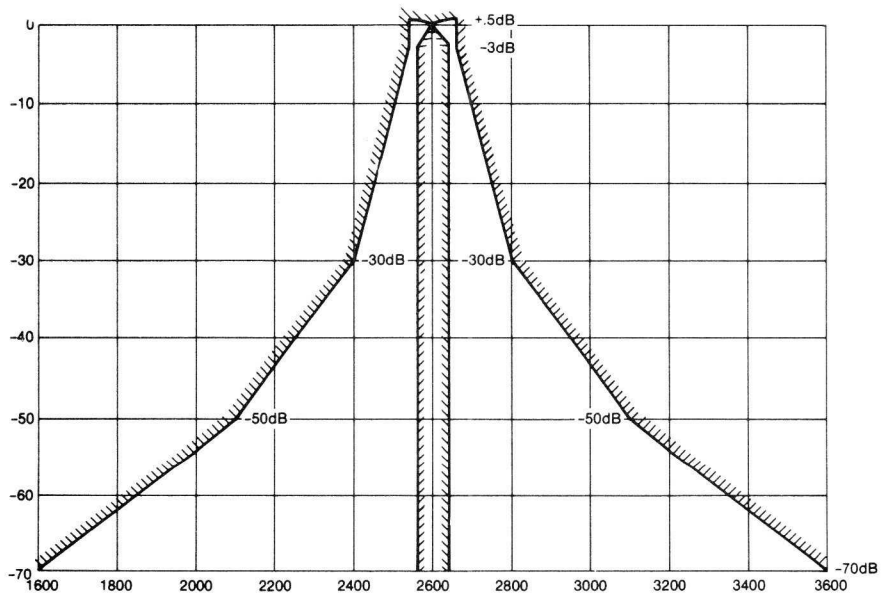


Fig.2 ACF 7310C PASS BAND ATTENUATION LIMITS

ACF7323C ACF7363C
ACF7383C

DTMF Tone Detection Band Pass Filters

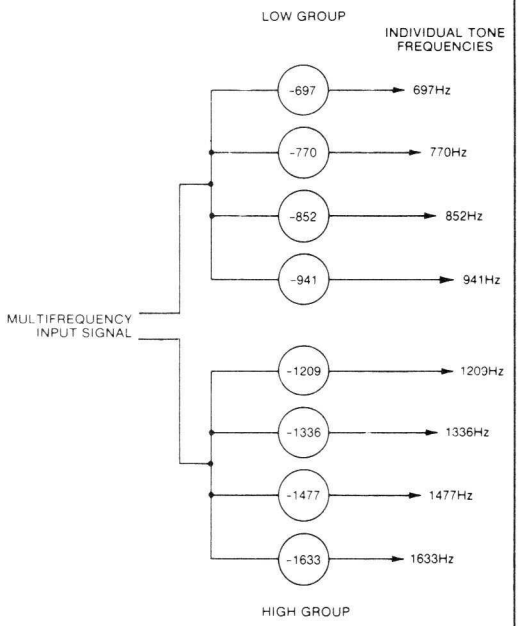
FEATURES

- Standard model tone frequency settings of 697, 770, 852, 941, 1209, 1336, 1477 and 1633 and MF frequencies of 700, 900, 1100, 1300, 1500, 1700.
- ± 0.3% F_O tolerance
- ± 0.0075%/°C F_O temperature coefficient
- ± 0.1%/°C Q temperature coefficient
- Preset Q, 22 ±10% (4.5% B.W.)
- Filter design factory turnable over F_O range of 500 to 3kHz and Q range of 10 to 30
- Low power consumption 72mW max at±12VDC
- Can be operated with single-ended power supplies

DESCRIPTION

The General Instrument ACF 7323C/ACF 7363C/ACF 7383C Band Pass Active Filters are pre-tuned active filters designed specifically for tone receiver applications. These filters are available in hermetically sealed 12-lead TO-8, D.D.I.L., and S.I.L. packages.

TYPICAL APPLICATION
8-SECTION TONE FILTER



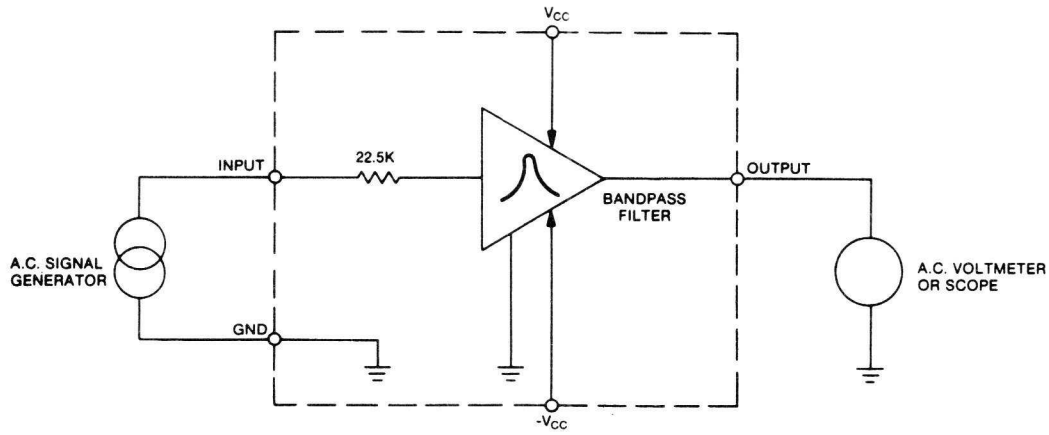
ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

$+V_{CC}$ = +12V,
$-V_{CC}$ = -12V

Characteristic	Min	Typ	Max.	Units	Conditions
Frequency Range	500	—	3000	Hz.	Note 1
Q Range	10	—	30	—	Note 1
F_O Accuracy	—	±0.2	±0.3	%	
F_O Temp Coef	—	± 35	± 75	ppm/°C	(0°C to 70°C)
Q Accuracy	—	—	±10	%	
Q Temp Coef	—	±500	±1000	ppm/°C	(0°C to 70°C)
Voltage Gain	-1	0	+1	dB	@F_O (0°C to 70°C)
Input Impedance	22.5	30	—	kΩ	
Output voltage	—	7	—	V_{RMS}	
Output Impedance	—	—	1	Ω	10 to 10kHz
Output Noise	—	0.25	0.75	mV_{RMS}	10 to 10kHz
Output Offset Voltage	—	±40	±60	mV	
Positive Supply Voltage	+5	+12	+18	V	
Negative Supply Voltage	-5	-12	-18	V	
Power Supply Current @±15V	—	1.5	3.0	mA	
Operating Temp Range	0	—	70	°C	
Storage Temp Range	-55	—	150	°C	

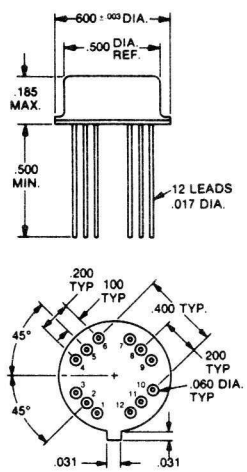
NOTE 1:
For the eight standard models, Q is preset to 22 and F_o is preset at the tone frequencies: 697, 770, 852, 941, 1209, 1336, 1477 and 1633. The model number designation is ACF 73XXC — F_o (e.g., ACF 7323C—0697). Other values of Q are indicated by a dash number (e.g., ACF 7323C—0697—18).

TEST CIRCUIT



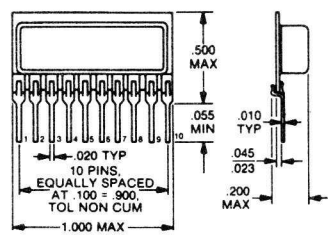
PACKAGE INFORMATION
PIN CONFIGURATION

ACF 7323C



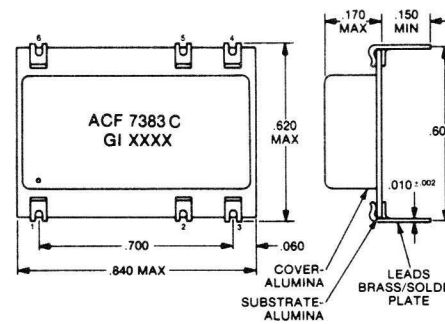
PIN FUNCTION
1. NC
2. NC
3. GND
4. Input Test Point
5. Input
6. NC
7. NC
8. NC
9. NC
10. Output
11. $-V_{CC}$
12. $+V_{CC}$

ACF 7363C



PIN FUNCTION
1. NC
2. Input
3. Test Point
4. NC
5. NC
6. $-V_{CC}$
7. GND
8. $+V_{CC}$
9. Output
10. NC

ACF 7383C



PIN FUNCTION
1. GND
2. Input Test Point
3. $+V_{CC}$
4. $-V_{CC}$
5. Output
6. Input

TELECOM

Dial Tone Band Suppression Filter

FEATURES

- 60dB Minimum attenuation at 350Hz and 440Hz
- 30dB Minimum attenuation at 60Hz
- 0dB Insertion loss in passband
- Can be operated from a single-ended power system

DESCRIPTION

The ACF 7401C is a dual tuned band suppression RC active filter which has been designed to reject frequencies of 350Hz and 440Hz, which are present on a telephone line. The unit is totally self contained and requires no external components for proper operation. The filter provides for 0dB insertion loss in the pass band of 697Hz through 1633Hz, the normal DTMF Tone Frequencies. The filter also provides for 60Hz attenuation for low noise operation. This filter is packaged in a dual in line package.

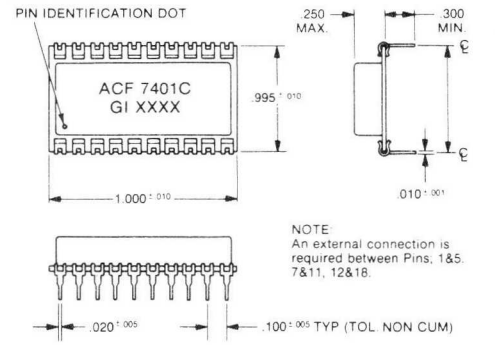
MAXIMUM RATINGS

V_{CC} ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to 150°C
Operating Temperature Range ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts R_S = 50Ω
R_L = 5kΩ 0°C to 70°C

PACKAGE INFORMATION
PIN CONFIGURATION

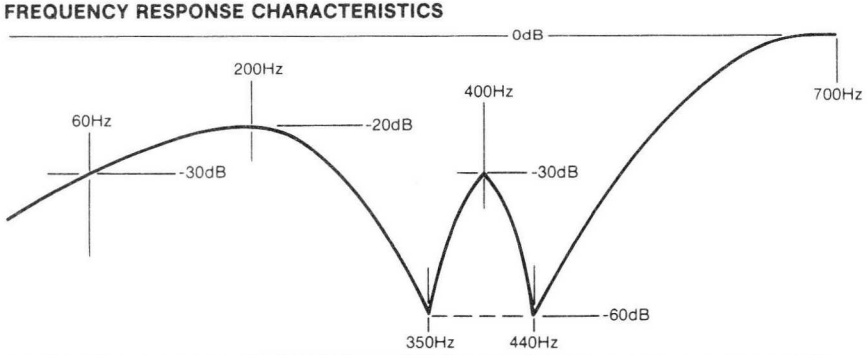


PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	Test Point	8.	Minus V_{CC}	15.	NC
2.	NC	9.	Plus V_{CC}	16.	NC
3.	Input	10.	GND	17.	NC
4.	NC	11.	Test Point	18.	Test Point
5.	Test Point	12.	Test Point	19.	NC
6.	NC	13.	NC	20.	Output
7.	Test Point	14.	NC		

Characteristics	Min	Typ	Max	Units	Conditions
Input Impedance	30	—	—	kΩ	
Input Voltage Range	—	—	V_{CC}	Volts	
Frequency Response					Referenced to 941Hz Gain
60Hz	-30	—	—	dB	
350Hz	-60	—	—	dB	
440Hz	-60	—	—	dB	
680 to 1750Hz	-0.5	0	0.5	dB	
1750 to 3000Hz	-0.8	0	+0.8	dB	
10000Hz	—	-3.5	—	dB	
Output Impedance	—	—	25	Ω	
Output Voltage Range	5.	—	—	Volts p-p	
Power Supply Current	—	—	10	mA	

NOTE: 1. Or equivalent single-ended power supplies.

TYPICAL FREQUENCY RESPONSE CHARACTERISTICS



2600Hz Band Suppression Filter

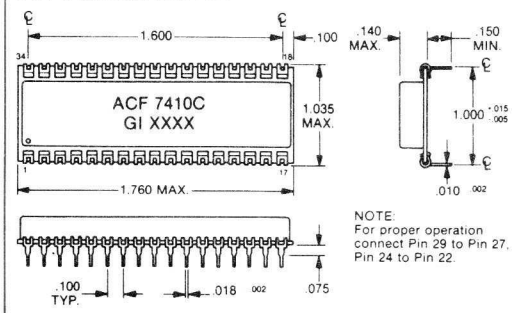
FEATURES

- 60 dB attenuation from 2585Hz to 2615Hz.
- Low Power Dissipation
- Narrow Band Rejection
- Low Ripple
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7410C is a linear hybrid band suppression RC Active Filter. The ACF 7410C is a sharply tuned filter designed to reject the 2600Hz signaling frequency. This filter provides for a 9 dB attenuation to match the characteristics of a passive filter system. In addition, the filter provides a minimum attenuation of 60 dB, plus and minus 15Hz from the ideal center frequency of 2600Hz. This filter is packaged in a dual in line configuration.

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE:
For proper operation connect Pin 29 to Pin 27, Pin 24 to Pin 22.

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	T.P.	9.	+12VCD	18.	-12VDC	26.	NC
2.	NC	10.	NC	19.	Output	27.	Stage 2 Input
3.	NC	11.	NC	20.	T.P.	28.	NC
4.	NC	12.	T.P.	21.	NC	29.	Stage 1 Output
5.	NC	13.	NC	22.	Stage 3 Input	30.	NC
6.	NC	14.	NC	23.	NC	31.	T.P.
7.	T.P.	15.	NC	24.	Stage 2 Output	32.	Input
8.	NC	16.	NC	25.	T.P.	33.	NC
		17.	GND			34.	NC

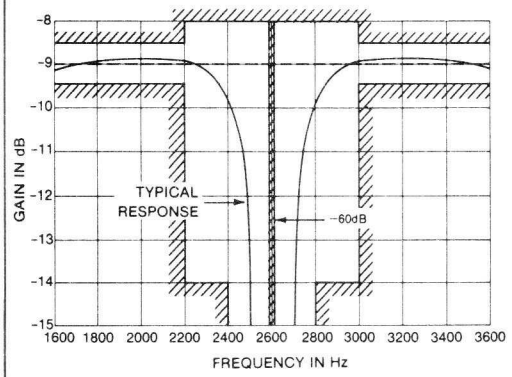


Fig. 1 FREQUENCY RESPONSE LIMITS ACF 7410C

MAXIMUM RATINGS

V_{CC} (Max) ..... ± 18 Volts
V_{CC} (Min) ..... ± 8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

at V_{CC} = ±12 Volts,
T_A = 25°C,
R_S = 50 Ω,
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-9.5	-9.0	-8.5	dB	1000Hz
Frequency Response					Referenced from the 1000Hz Gain as 0 dB
	-0.5	0	+0.5	dB	250Hz to 220Hz
	+1.0	—	-5.0	dB	2200Hz to 2400Hz
	-60	—	—	dB	2585Hz to 2615Hz
	+1.0	—	-5.0	dB	2800Hz to 3000Hz
	-0.5	0	+0.5	dB	3000Hz to 3400Hz
Input Impedance	25	—	—	kΩ	
Output Offset Voltage	—	—	100	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	0.5	%	V_{OUT} = 4.0 V_{PP}, Freq. = 1.0kHz
Current Drain	—	—	6.0	mA	

TELECOM

DTMF Band Separation Filter

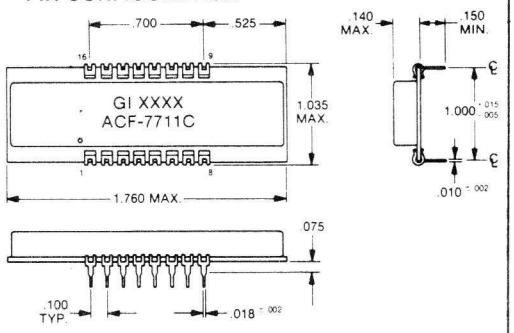
FEATURES

- Dual Filter in one package
- 24dB minimum out of band attenuation
- Low in band ripple
- 0 dB insertion loss
- 30 dB minimum out of band attenuation at 941Hz and 1209Hz respective
- Low power dissipation
- Can be operated from a single-ended power system

DESCRIPTION

The ACF 7711C is a dual RC active filter which has been designed to provide channel isolation between the low frequency group of the Tone (DTMF) frequencies of 697Hz through 941Hz, and the high frequency group of the Tone (DTMF) frequencies of 1209Hz through 1633Hz. This dual filter is packaged in a dual in line package.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Low Group Output	9.	Interstage Input #4
2	Plus V_{CC}	10.	Test Point #3
3	Test Point #2	11.	High Group Output
4	Low Group Input	12.	High Group Input
5	Interstage Output #3	13.	Test Point #1
6	GND #1	14.	Minus V_{CC}
7	GND #2	15.	Interstage Output #2
8	Test Point #4	16.	Interstage Input #1

NOTE: An external connection is required between Pins: 3&13, 5&9, 6&7, 8&10, 15&16.

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage (at V_{CC} max) ..... ±15 Volts
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

V_{CC} = ± 12V (Note 1)
R_L = 5kΩ
R_S = 50 Ω
0°C to 70°C

Characteristic	Min	Typ	Max.	Units	Conditions
Low Group Filter Section					
Input Impedance	30	—	—	kΩ	
Input Voltage Range	—	—	±12	Volts	
Gain	—	0	±0.25	dB	941Hz
Frequency Response					Reference to 941Hz Gain
650Hz to 941Hz	-.75	0	+.75	dB	
1209Hz	-30	—	—	dB	
1209Hz to 1700Hz	-24	—	—	dB	
Output Voltage Range	±3.2	—	—	Volts	No Clipping
Output Impedance	—	—	10	Ω	
High Group Filter Section					
Input Impedance	60	—	—	kΩ	
Input Voltage Range	—	—	±12	Volts	
Gain	—	0	±0.25	dB	1209Hz
Frequency Response					Reference to 1209Hz Gain
1209Hz to 1700Hz	-.75	0	+1.5	dB	
941Hz	-30	—	—	dB	
941Hz to 650Hz	-24	—	—	dB	
Output Voltage Range	±3.2	—	—	Volts	No Clipping
Output Impedance	—	—	10	Ω	
Power Supply Current	—	4.0	5.0	mA	

NOTE:
1. Or equivalent single - ended power supplies.

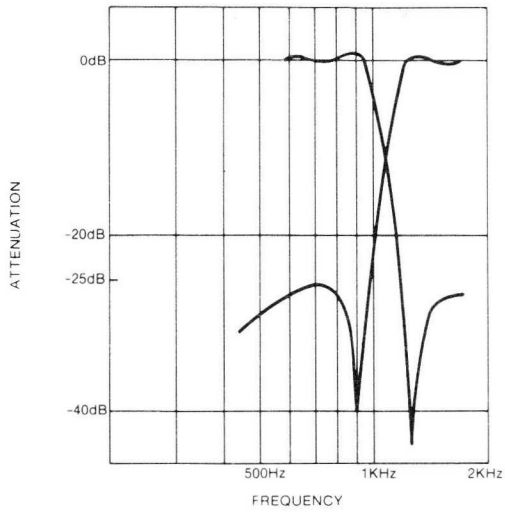


Fig.1 TYPICAL FREQ RESPONSE

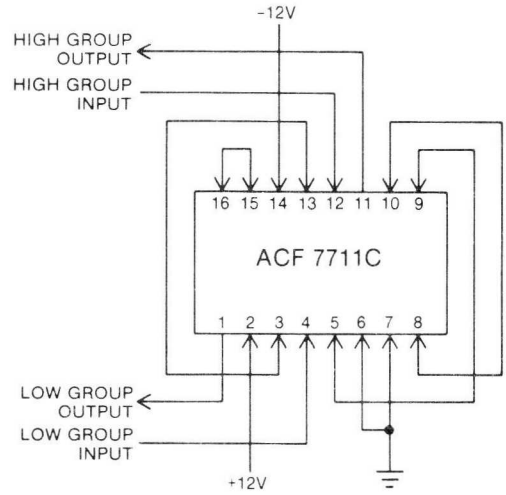


Fig.2 TONE SEPARATION FILTER TERMINATION

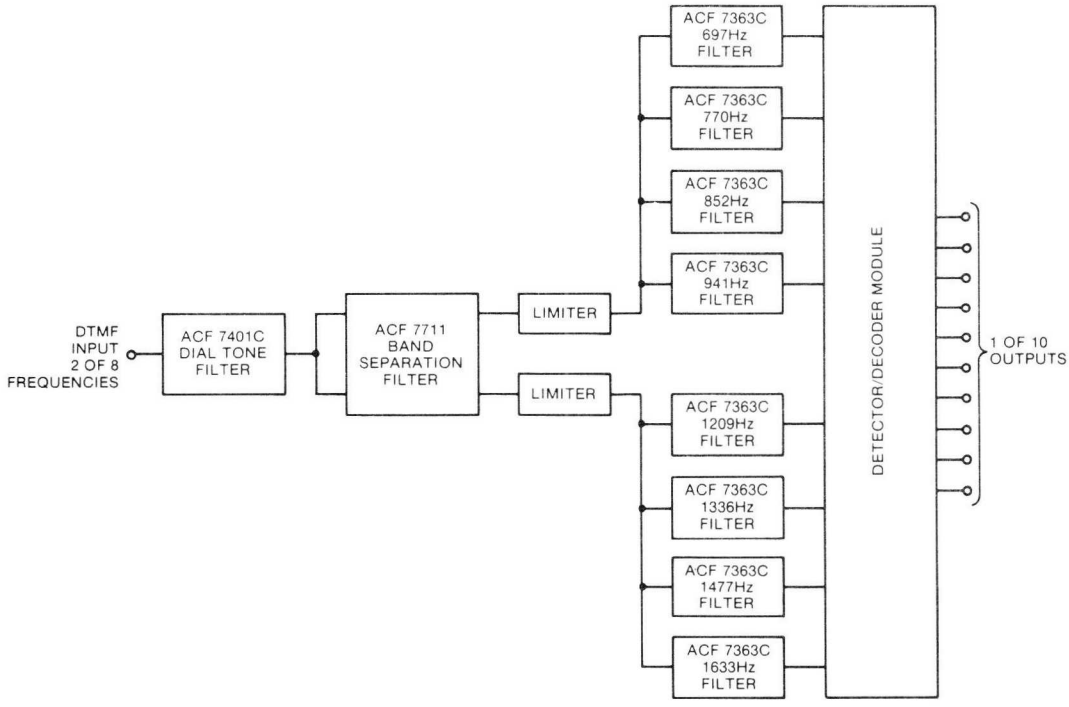


Fig.3 TYPICAL DTMF RECEIVER APPLICATION

TELECOM

DATA COMMUNICATIONS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
UAR/T	Complete 5-8 bit receiver/transmitter interface.	AY-5-1013A	5-74
		AY-6-1013	5-74
		AY-3-1014A	5-74
		AY-3-1015D	5-74
P/SAR	Programmable receiver interface.	AY-8-1472B	5-87
P/SAT	Programmable transmitter interface.	AY-8-1482B	5-94
16 CHANNEL MULTIPLEXER	Multiplexes 16 analog channels with on-chip logic control.	AY-5-1016	5-102
		AY-6-4016	5-102

UAR/T: Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TTL compatible—no interfacing circuits required—drives one TTL load
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation—can handle multiple bauds (receiving-transmitting) simultaneously
- Start Bit Verification—decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs—bus structure capability
- Low Power-minimum power requirements
- Input Protected—eliminates handling problems

AY-5-1013A
- GIANT P-channel nitride process
- 0 to 40kbaud
- Pull up resistors to V_{CC} on all inputs

AY-6-1013
- GIANT P-channel nitride process
- 0 to 22.5kbaud
- Extended Operating Temperature Range:
  -40° C to +85° C (plastic package)
  -55° C to +125° C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs

AY-3-1014A/1015D
- Single Supply Operation:
  +4.75V to +14V (AY-3-1014A)
  -4.75V to -5.25V (AY-3-1015D)
- CMOS compatible (AY-3-1014A)
- 1½ stop bit mode
- External reset of all registers except control bits register.
- GIANT II N-channel Ion Implant Process
- 0 to 30k baud
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015D)

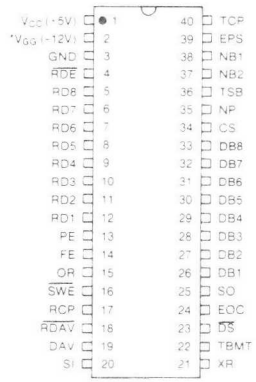
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability with the AY-3-1014A/1015D), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

PIN CONFIGURATION

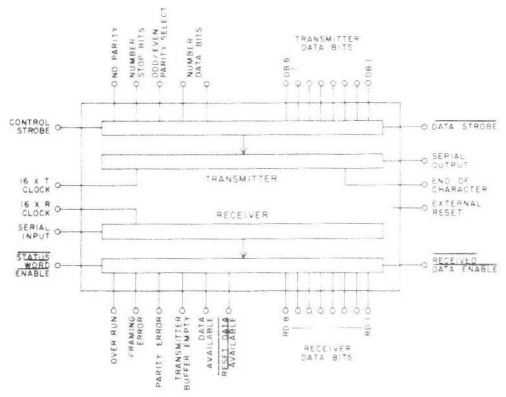
40 LEAD DUAL IN LINE

Top View



* Pin 2: AY-3-1014A/1015D — No Connection.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	V_{GG} Power Supply (V_{GG})	-12V Supply (Not connected for AY-3-1014A/1015)
3	Ground (V_{SS})	Ground
4	Received Data Enable ($\overline{RDE}$)	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{RDE}$ is "0" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable ($\overline{SWE}$)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available ($\overline{RDAV}$)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset. Must be tied to logic '1' when not in use on the AY-3-1014A.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig.12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig.11,12,33,34.
21	External Reset (XR)	Resets all registers except the control bits register (the received data register is not reset in the AY-5-1013A and AY-6-1013). Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig.18,20,40,42.
23	Data Strobe ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig.17,19,39,41.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig.16.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TRANSMITTER OPERATION

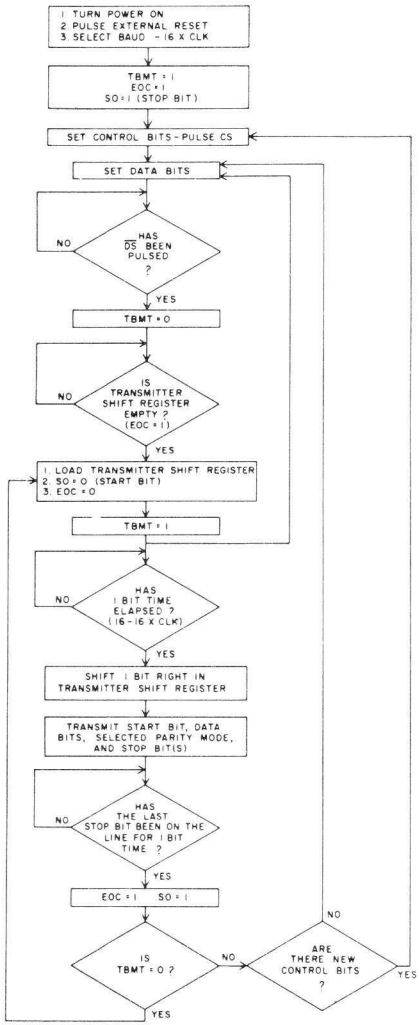


Fig.1

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

RECEIVER OPERATION

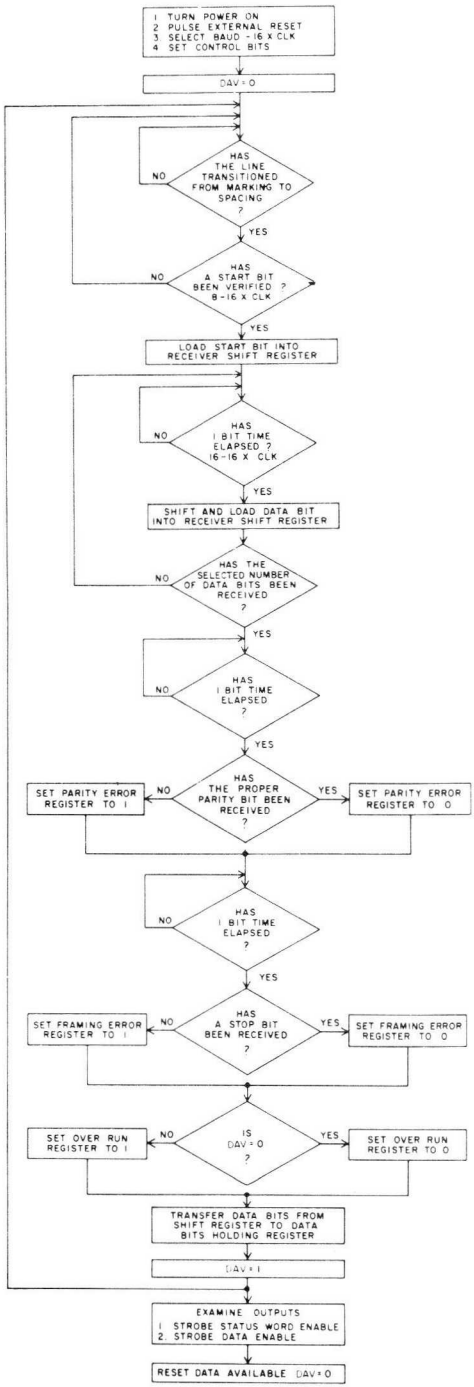


Fig.2

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "1".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

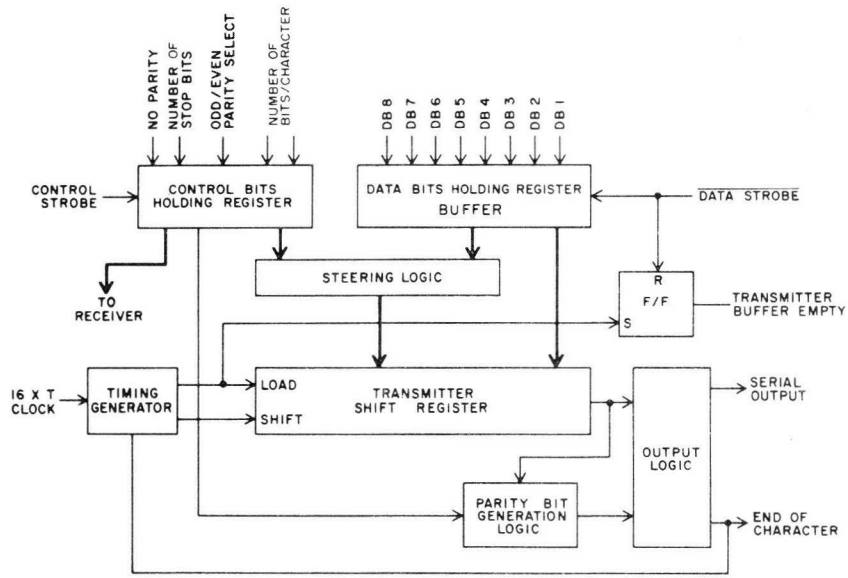


Fig.3 TRANSMITTER BLOCK DIAGRAM

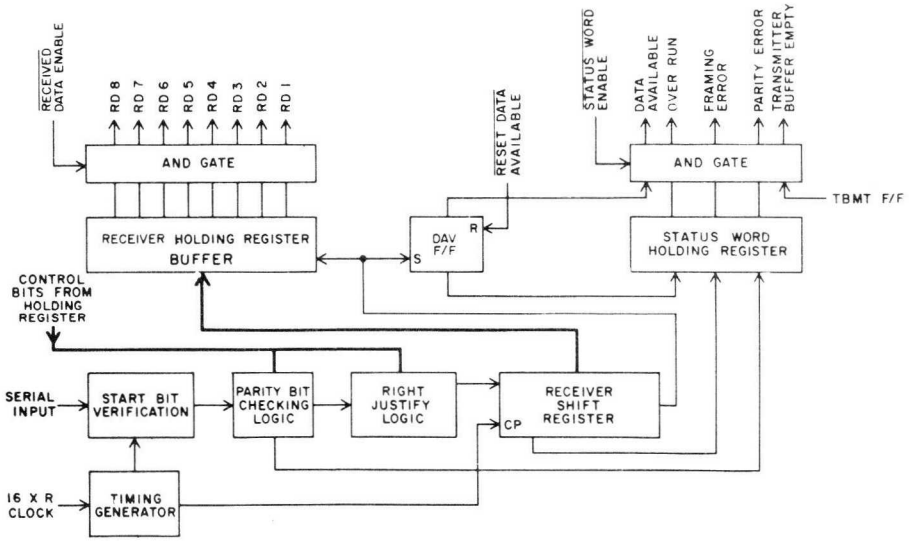


Fig.4 RECEIVER BLOCK DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} (with respect to V_{CC}) . . . . . −20 to +0.3V
Clock and logic input voltages (with respect to V_{CC}) . . . . . −20 to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = −12V ±5%
V_{CC} = +5V ±5%
Temperature (T_A) = 0°C to +70°C (AY-5-1013A)
−40 C to +85°C (AY-6-1013 Plastic Package)
−55C to +125°C (AY-6-1013 Ceramic Package)

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels					
Logic 0	0	—	0.8	Volts	(I_{IL} = −1.6mA max.)
Logic 1	V_{CC}-1.5	—	V_{CC}+0.3	Volts	Unit has internal pullup resistors
Input Capacitance					
All Inputs	—	—	20	pF	0 volts bias, f= 1MHz
Leakage Currents					
Three State Outputs	—	—	1.0	µA	0 volts
Data Output Levels					
Logic 0	—	—	+0.4	Volts	I_{OL}= 1.6mA (sink)
Logic 1	V_{CC}-1.0	—	—	Volts	I_{OH}= .3mA (source)
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig. 23
Power Supply Current					
I_{GG} } 25°C,all inputs +5V	—	14	16	mA	AY-5-1013A - See Fig.25
I_{GG} } 25°C,all inputs +5V	—	17	19	mA	AY-6-1013 - See Fig.25
I_{CC} } 25°C,all inputs +5V	—	18	20	mA	AY-5-1013A - See Fig.26
I_{CC} } 25°C,all inputs +5V	—	21	23	mA	AY-6-1013
AC CHARACTERISTICS					T_A = 25°C, output load capacitance 50pF max.
Clock Frequency	DC	—	640	kHz	AY-5-1013A
	DC	—	360	kHz	AY-6-1013
Baud	0	—	40	kbaud	AY-5-1013A
	0.	—	22.5	kbaud	AY-6-1013
Pulse Width					
Clock Pulse	750	—	—	ns	AY-5-1013A - See Fig.9
	1.5	—	—	µs	AY-6-1013-See Fig.9
Control Strobe	300	—	—	ns	AY-5-1013A-See Fig. 15, 16
	600	—	—	ns	AY-6-1013
Data Strobe	190	—	—	ns	AY-5-1013A-See Fig. 14
	250	—	—	ns	AY-6-1013
External Reset	500	—	—	ns	AY-5-1013A - See Fig. 13
	1.0	—	—	µs	AY-6-1016
Status Word Enable	500	—	—	ns	AY-5-1013A - See Fig. 21
	600	—	—	ns	Ay-6-1013 - See Fig. 21
Reset Data Available	250	—	—	ns	Ay-5-1013A - See Fig. 22
	350	—	—	ns	AY-6-1013 - See Fig. 22
Received Data Enable	500	—	—	ns	AY-5-1013A - See Fig. 21
	600	—	—	ns	AY-6-1013 - See Fig. 21
Set Up & Hold Time					
Input Data Bits	0	—	—	ns	See Fig.14
Input Control Bits	0	—	—	ns	See Fig. 15, 16
Output Propagation Delay					
TPD0	—	—	500	ns	AY-5-1013A - See Fig. 21 & 24
	—	—	650	ns	AY-6-1013 - See Fig. 21 & 24
TPD1	—	—	500	ns	Ay-5-1013A - See Fig. 21 & 24
	—	—	650	ns	AY-6-1013 - See Fig. 21 & 24

**Typical values are at +25°C and nominal voltages.

TELECOM

TIMING DIAGRAMS

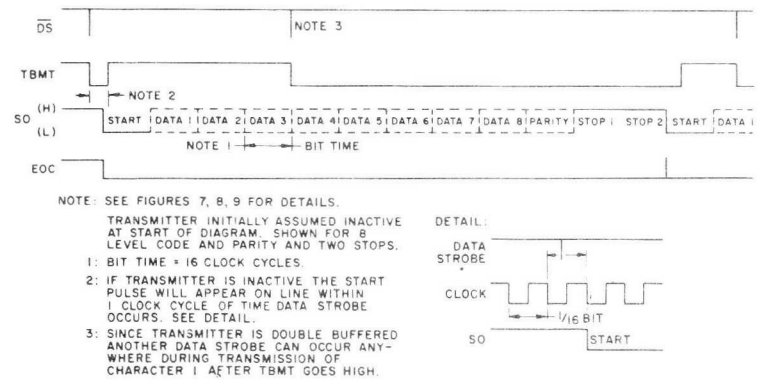


Fig.5 UAR/T TRANSMITTER TIMING

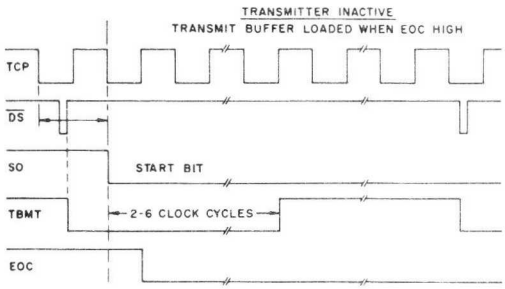


Fig.6 TRANSMITTER AT START BIT

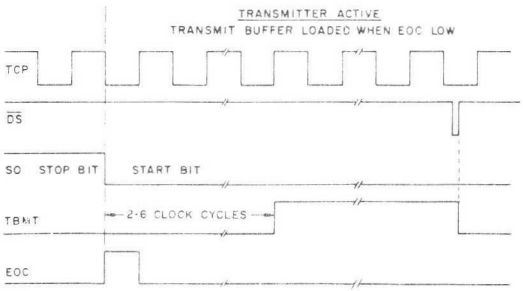


Fig.7 TRANSMITTER AT START BIT

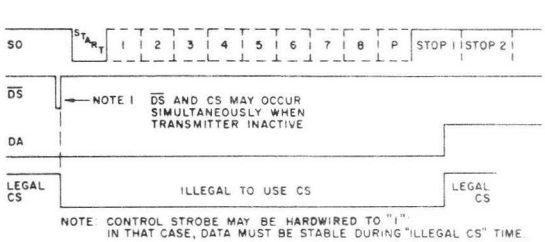


Fig.8 ALLOWABLE POINTS TO USE CONTROL STROBE

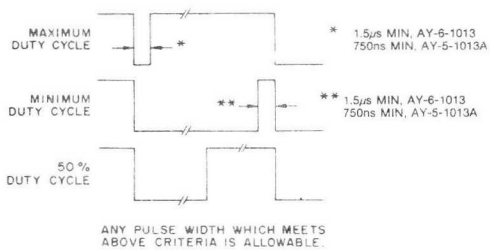
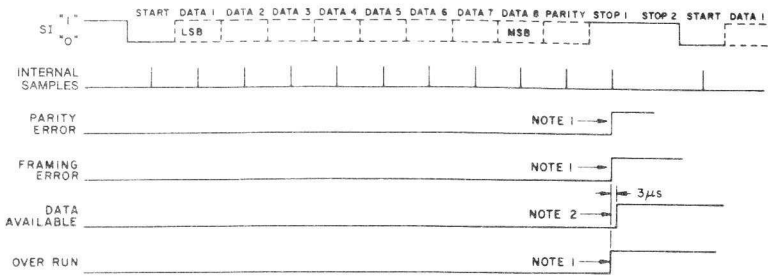


Fig.9 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Fig.10 UAR/T RECEIVER TIMING

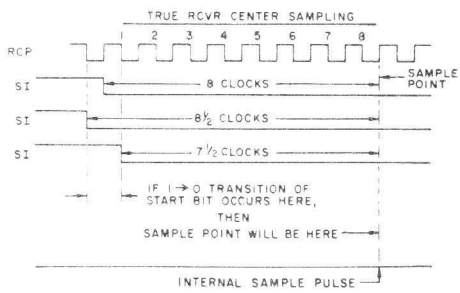


Fig.11

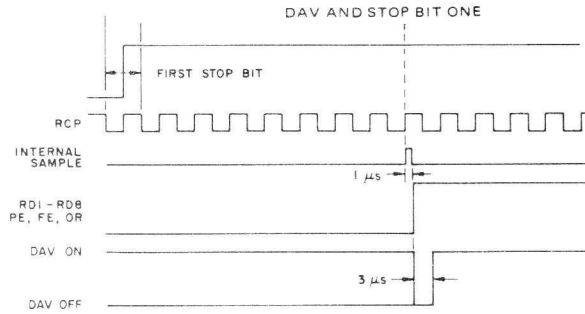
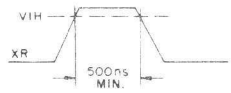


Fig.12 RECEIVER DURING 1st STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER AND RECEIVED DATA. SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO 0V.

Fig.13 XR PULSE

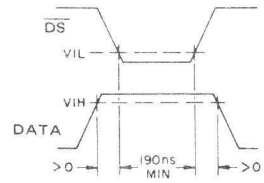
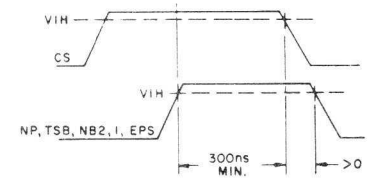
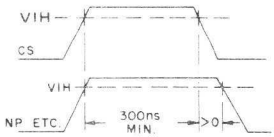


Fig.14 DS



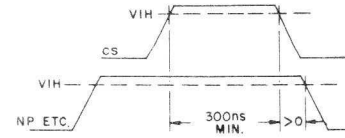
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS.

Fig.15a CS



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM.

Fig.15b CS



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

Fig.16 CS

TELECOM

TIMING DIAGRAMS

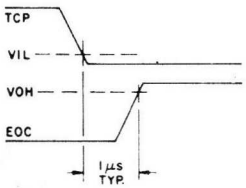


Fig.17 EOC TURN-ON

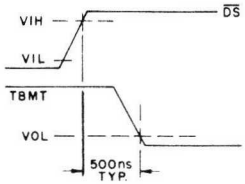


Fig.18 TBMT TURN-OFF

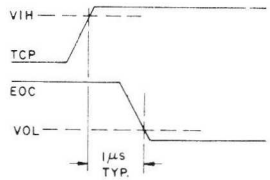


Fig.19 EOC TURN-OFF

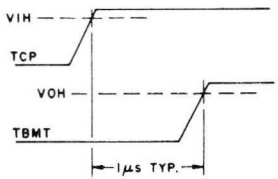


Fig.20 TBMT TURN-ON

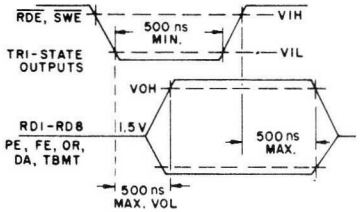


Fig.21 RDE, SWE

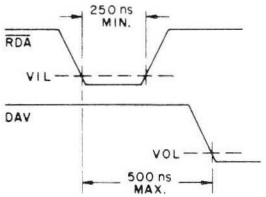


Fig.22 RDAV

TYPICAL CHARACTERISTIC CURVES

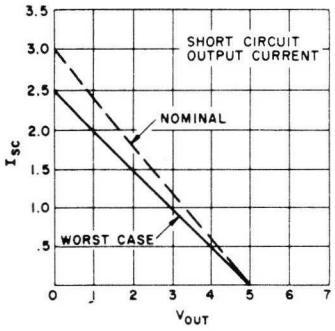


Fig.23 SHORT CIRCUIT OUTPUT CURRENT

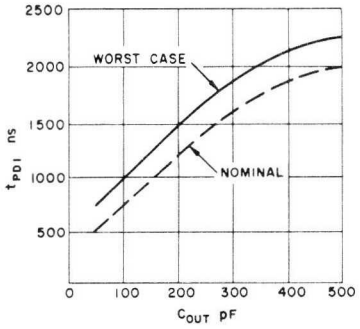


Fig.24 RE1, RD8, PE, FE, OR, TBMT, DAV

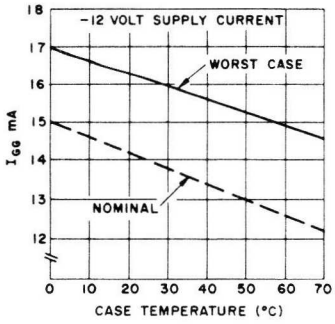


Fig.25 -12 VOLT SUPPLY CURRENT

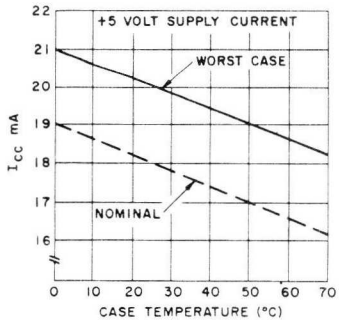


Fig.26 +5 VOLT SUPPLY CURRENT

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with respect to GND) . . . . . −0.3 to +16V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . 0°C to +70°C
Lead Temperature (Soldering, 10 sec) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

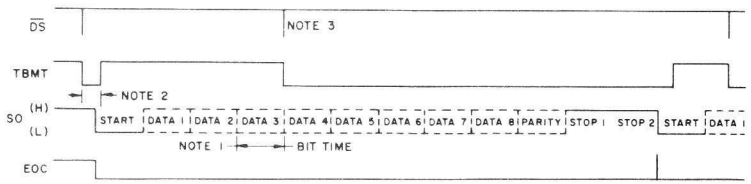
V_{CC} = +4.75 to +14V (AY-3-1014A)
V_{CC} = +4.75V to +5.25V (AY-3-1015D)
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels (AY-3-1014A)					
Logic 0	0	—	0.8	Volts	
Logic 1: at V_{CC} = +4.75V	2.0	—	V_{CC} +0.3	Volts	
at V_{CC} = +14V	3.0	—	V_{CC} +0.3	Volts	
Input Logic Levels (AY-3-1015)					
Logic 0	0	—	0.8	Volts	
Logic 1	2.0	—	V_{CC}+0.3	Volts	AY-3-1015 has internal pull-up resistors to V_{CC}.
Input Capacitance					
All inputs	—	—	20	pF	0 volts bias, f = 1 MHz
Output Impedance					
Tri-State Outputs	1.0	—	—	MΩ	
Data Output Levels					
Logic 0	—	—	+0.4	Volts	I_{OL} = 1.6mA (sink)
Logic 1: AY-3-1014A/1015D	2.4	—	—	Volts	I_{OH} = -40μA (source) - at V_{CC} = +5V
AY-3-1014A only	3.5	—	—	Volts	I_{OH} = -50μA (source) - at V_{CC} = +14V
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig.45.
Power Supply Current					
I_{CC} at V_{CC} = +5V (AY-3-1014A)	—	10	15	mA	See Fig.47.
I_{CC} at V_{CC} = +14V (AY-3-1014A)	—	14	20	mA	See Fig.48.
I_{CC} at V_{CC} = +5V (AY-3-1015D)	—	10	15	mA	
A.C. CHARACTERISTICS					T_A = 25°C, Output load capacitance 50 pF max.
Clock Frequency	DC	—	480/400	kHz	at V_{CC} = +4.75V/+14V
Baud	0	—	30/25	kbaud	at V_{CC} = +4.75V/+14V
Pulse Width					
Clock Pulse	1.0	—	—	μs	See Fig.31
Control Strobe	200		—	ns	See Fig.37
Data Strobe	200	—	—	ns	See Fig.36
External Reset	500	—	—	ns	See Fig.35
Status Word Enable	500		—	ns	See Fig.43
Reset Data Available	200	—	—	ns	See Fig.44
Received Data Enable	500	—	—	ns	See Fig.43
Set Up & Hold Time					
Input Data Bits	20	—	—	ns	See Fig36
Input Control Bits	20	—	—	ns	See Fig.37
Output Propagation Delay					
TPD0	—	—	500	ns	See Fig.43 & 46
TPD1	—	—	500	ns	See Fig.43 & 46

**Typical values are at +25°C and nominal voltages.

TELECOM

TIMING DIAGRAMS



NOTE: SEE FIGURES 28, 29, 30 FOR DETAILS.
TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.
1: BIT TIME = 16 CLOCK CYCLES.
2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE 1 TO 2 CLOCK CYCLES AFTER THE DATA STROBE OCCURS. SEE DETAIL.
3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

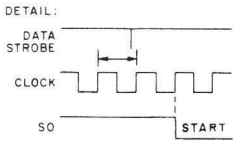


Fig.27 UAR/T — TRANSMITTER TIMING

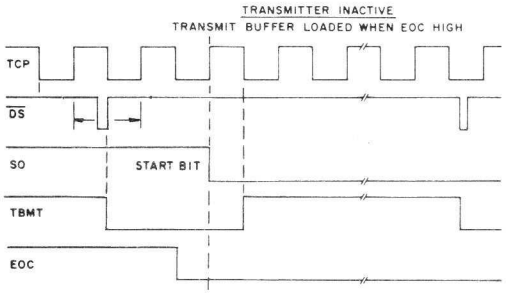


Fig.28 TRANSMITTER AT START BIT

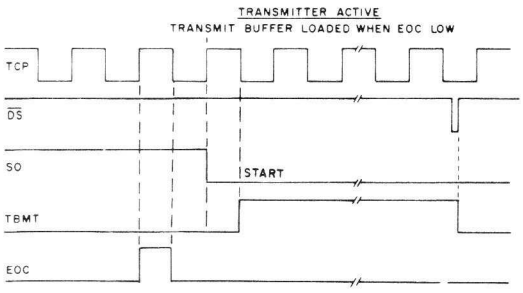
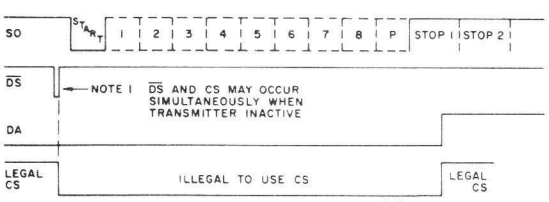
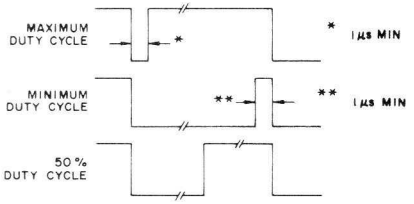


Fig.29 TRANSMITTER AT START BIT



NOTE: CONTROL STROBE MAY BE HARDWIRED TO "1" IN THAT CASE, CONTROL DATA BITS MUST BE STABLE DURING "ILLEGAL CS" TIME.

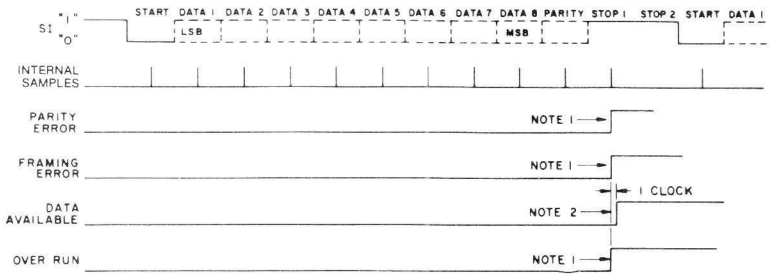
Fig.30 ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

Fig.31 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE. PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RDI (PIN 12).

Fig.32 UAR/T — RECEIVER TIMING

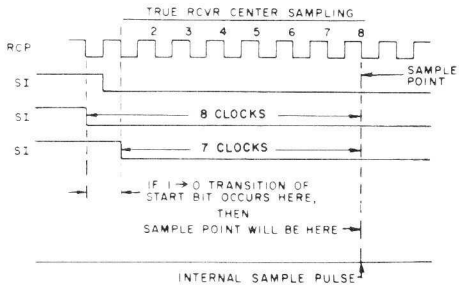


Fig.33

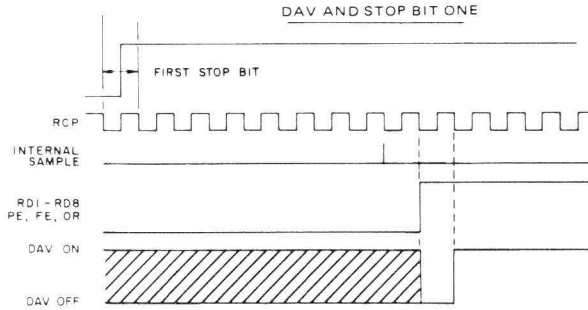
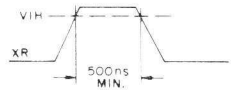


Fig.34 RECEIVER DURING 1ST STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT THE CONTROL REGISTER. SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO OV.

Fig.35 XR PULSE

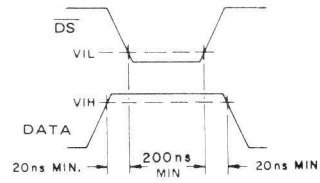
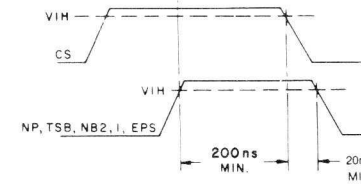
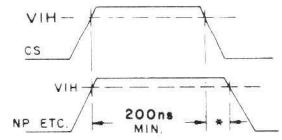


Fig.36 $\overline{DS}$



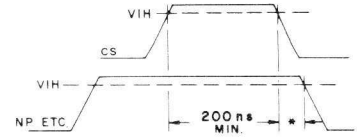
CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS.

Fig.37a CS



CONTROL STROBE AND CONTROL BITS MUST BE 200ns MINIMUM.

Fig.37b



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

* 20ns MIN.

Fig.38

TELECOM

TIMING DIAGRAMS

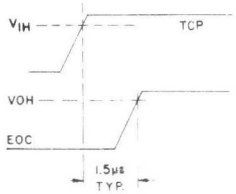


Fig.39 EOC TURN-ON

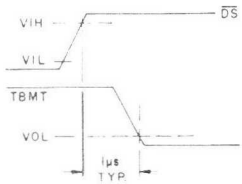


Fig.40 TBMT TURN-OFF

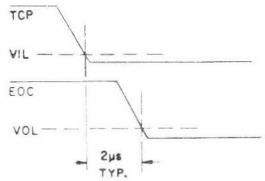


Fig.41 EOC TURN-OFF

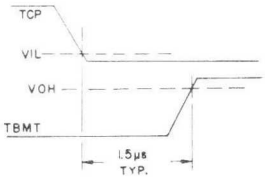


Fig.42 TBMT TURN-ON

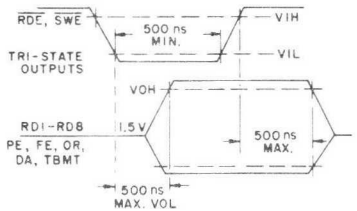


Fig.43 RDE, SWE

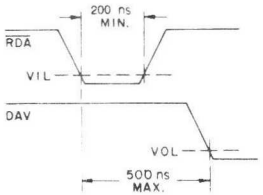


Fig.44 RDAV

TYPICAL CHARACTERISTIC CURVES

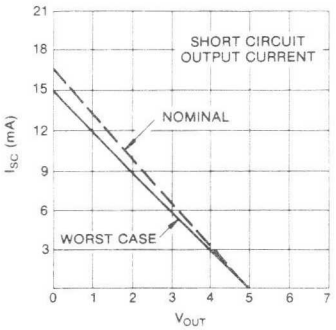


Fig.45 SHORT CIRCUIT OUTPUT CURRENT
(only 1 output may be
shorted at a time)

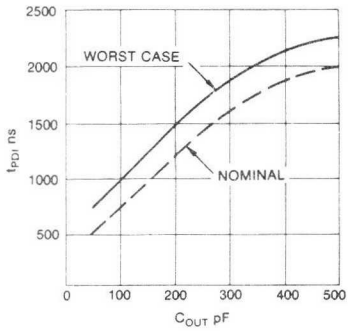


Fig.46 RD1-RD8, PE, FE, OR, TBMT, DAV

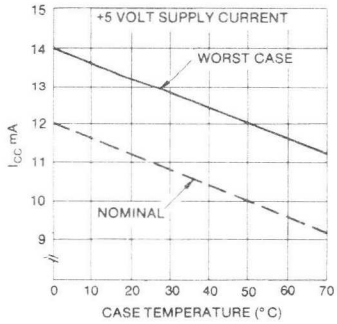


Fig.47 +5 VOLT SUPPLY CURRENT

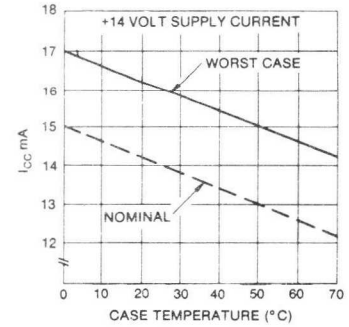


Fig.48 +14 VOLT SUPPLY CURRENT
(AY-3-1014A only)

P/SAR: Programmable Synchronous Asynchronous Receiver

FEATURES

- Directly TTL & DTL Compatible — Internal Active Input Pull-Up Devices & Push-Pull Output Buffers.
- Programmable Mode & Clock Rate Selection — Asynchronous & Isochronous — 1X, 16X, 32X or 64X Clock Rate; Synchronous — Internal or External Character Synchronization.
- Programmable Transmission Codes — Character Length of 5, 6, 7 or 8 data bits plus Parity; Parity Inhibit.
- DC High Speed Operation — Bit Rate to 640kbits/sec. with 1X Clock.
- Double Buffered Receiver

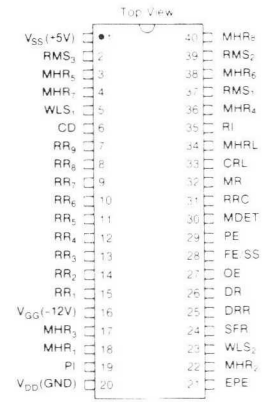
DESCRIPTION

The General Instrument AY-8-1472B P/SAR is a Programmable Receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

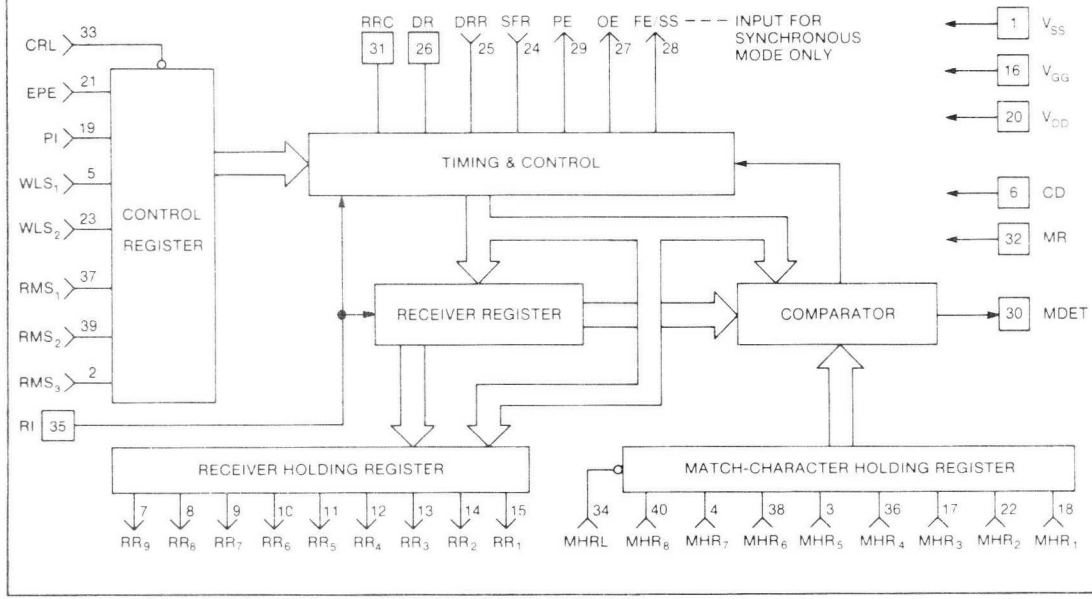
Contiguous synchronous serial characters are compared in a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit (s) which are stripped from the data. Four internal registers, in conjunction with Tri-State Output lines provide full system versatility.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



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PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{SS} Power Supply (V_{SS})	+5 volt supply
37, 39, 2	Receiver Mode Select (RMS_1, RMS_2, RMS_3)	These three pins select the receiver operating mode. **RMS_3 RMS_2 RMS_1 MODE** 0 0 0 Asynch. or Isoch. 1 ×Clock 0 0 1 Asynch. or Isoch. 16 × Clock 0 1 0 Asynch. or Isoch. 32 × Clock 0 1 1 Asynch. or Isoch. 64 × Clock 1 X 0 Synch, External Character Synchronization 1 X 1 Synch, Internal Character Synchronization When operating in asynchronous or isochronous mode with 1× clock, there is no protection against false start bits.
18, 22, 17, 36, 3, 38, 4, 40	Match-Character Holding Register Data (MHR_1-MHR_8)	Parallel 8-bit characters are loaded into the Match Character Holding Register. If a character of less than 8-bits has been selected, only the least significant are accepted.
5, 23	Word Length Select (WLS_1-WLS_2)	These two pins select the number of bits per character. **WLS_2 WLS_1 Selected Word Length** 0 0 5-bits 0 1 6-bits 1 0 7-bits 1 1 8-bits
6	Chip Disable (CD)	A logic '1' applied to this pin will disable the busable inputs and tri-state outputs. The I/O lines controlled by Chip Disable are: **Input Lines** **Tri-State Outputs** CRL DRR PE EPE SFR FE PI MHRL OE WLS_1-WLS_2 MHR_1-MHR_8 RR_1-RR_8 RMS_1-RMS_3
7-15	Receiver Holding Register Data Outputs (RR_1-RR_9)	The parallel character, including parity (RR_9), appears on these lines. Selection of a word length less than eight (8) bits will cause the most significant bits of the Character to be forced to a logic '0'. The character will be right justified including the parity bit if programmed. RR_1 is the least significant bit.
16	V_{GG} Power Supply (V_{GG})	−12 Volt Supply
19	Parity Inhibit (PI)	A logic '1' on this pin will eliminate the parity bit from the received character. If not used, this lead must be tied to a logic '0'.
20	V_{DD} Power Supply (V_{DD})	Ground
21	Even Parity Enable (EPE)	The logic level on this pin selects the type of parity which will be verified by the receiver or each incoming character. A logic '0' selects odd parity and a logic '1' will select even parity.
24	Status Flag Reset (SFR)	A logic '0' applied to this pin resets the PE, FE and OE status flags.
25	Data Received Reset (DRR)	A logic '0' applied to this pin resets the DR flag.
26	Data Received Flag (DR)	A logic '1' on this pin indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first Sync Character will not cause DR to go to a logic '1' level, but will cause MDET to do so.
27	Overrun Error Flag (OE)	A logic '1' indicates that the previously received Character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character or in the center of the first stop bit of an asynchronous or isochronous character at which time this flag is updated.
28	Framing Error/Sync Search (FE/SS)	FE/SS is a two-way I/O bus. If programmed for the asynchronous or isochronous mode, the Framing Error Flag indicates the status of the stop bit detection circuit. A logic '1' indicates that the Character transferred to the Receiver Holding Register has no valid stop bit. When programmed for the synchronous mode, this line is an input and is not under control of CD. If programmed for internal character synchronization, a logic '0' to logic '1' transition on the Sync Search (SS) line initiates the automatic Sync Character search operation. A transition from a logic '1' to a logic '0' transition on the SS line will cause the P/SAR to lose character synchronization. When programmed for external character synchronization, a logic '1' causes character synchronization to be initiated.

PIN FUNCTIONS cont'd

Pin No.	Name (Symbol)	Function
29	Parity Error (PE)	This pin goes to a logic '1' if the received character parity does not agree with the selected parity.
30	Match Detect Flag (MDET)	A logic '1' on this pin indicates that the contents of the Receiver Register are identical to the contents of the Match Character Holding Register
31	Receiver Register Clock (RRC)	This is a fifty (50) percent duty cycle clock. The negative going edge of this clock shifts data into the Receiver register at a rate determined by RMS_1-RMS_3.
32	Master Reset (MR)	A logic '1' on this pin will reset timing and control logic to an idle state, sets the contents of the receiver Holding Register to a logic '1', and resets the contents of the Match Character Holding Register, MDET, DR, PE, FE and OE flags.
33	Control Register Load Strobe (CRL)	A logic '0' on this pin will enter the control bits (EPE, PI, RMS_1-RMS_3, WLS_1-WLS_2), into the Control Register. This can be strobed or hard wired to a logic '0' level.
34	Match Character Holding Register Load Strobe (MHRL)	A logic '0' applied to this pin enables DC latches of the Match Character Holding Register and loads it with the Match Character data MHR_1-MHR_8. A logic '1' applied to this pin disables the Match Character Holding Register. This line may be strobed or hard-wired to a logic '0'.
35	Receiver Input (RI)	The serial input stream received on this pin will enter the Receiver Register.

ASYNCHRONOUS AND ISOCHRONOUS MODE

The completed assembly of a parallel character from a serial data stream and buffered by its Receiver Holding Register is indicated by the status of the Data Received (DR) Flag. The assembly of a character from a serial data stream consisting of a start bit, data, parity (if programmed) and a stop interval is initiated by the start bit transition.

Verification of parity and receipt of a valid stop bit is accomplished prior to character transfer to the Receiver Holding Register. This data is simultaneously compared with a preprogrammed character in the Match Character Holding Register. Status Flags, Data Received, Parity Error, Framing Error, Overrun Error and Match Detect are loaded into status registers during character transfer to the Receiver Holding Register.

Referring to the block diagram of the Receiver, the Chip Disable enables or disconnects various inputs and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match Character Holding Register and their respective load strobes CRL and MHRL are under CD control. In addition, DRR, SFR, PE, FE, OE and the outputs of the Receiver Holding Register are also Controlled by CD. It is necessary that CD enable these lines to allow strobing of information into associated registers, and to allow examination of output data and flags.

The receiver operating mode is determined by programming the Receiver Mode Select inputs RMS_1, RMS_2, RMS_3.

Table 1 summarizes all the programmable asynchronous and isochronous formats. A mark to space transition on the receiver input initializes the clock counter, causing it to count to the theoretical center of the start bit. At this time the input is sampled. A logic '1' input voltage at the Receiver Input causes the first mark to space transition to be interpreted as a noise spike and resets all timing and control logic. This provides one-half data bit noise immunity on all clock selection rates except for the 1X. A logic '0' input voltage at the Receiver Input at the theoretical center of the start bit causes timing and control circuitry to sample the theoretical center of succeeding data bits. This data is shifted through the Receiver Register. When an entire character (as defined by the Control Register) is assembled in the Receiver Register the line is "tested" for a valid stop bit at its theoretical center. This character is also compared with the contents of the Match Character Holding Register at the center of the stop bit and its parity is verified. A parallel transfer occurs, loading the contents of the Receiver Register (less start and stop bits) into the Receiver Holding Register. The status of the parity verification, framing error, and overrun error circuitry are also loaded into their appropriate registers to provide output error flags when the Data Received Flag is set. If the Data Received Flag has not been reset prior to the assembly of the current character, the previous character is lost and this is indicated by a logic '1' on the Overrun Error (OE) Flag.

Table 1
ASYNC OR ISOC MODE CONTROL DEFINITION

RMS3	WLS2	WLS1	PI	EPE	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
0	0	0	0	0	1	5	ODD	1 OR MORE
0	0	0	0	1	1	5	EVEN	1 OR MORE
0	0	0	1	X	1	5	NONE	1 OR MORE
0	0	1	0	0	1	6	ODD	1 OR MORE
0	0	1	0	1	1	6	EVEN	1 OR MORE
0	0	1	1	X	1	6	NONE	1 OR MORE
0	1	0	0	0	1	7	ODD	1 OR MORE
0	1	0	0	1	1	7	EVEN	1 OR MORE
0	1	0	1	X	1	7	NONE	1 OR MORE
0	1	1	0	0	1	8	ODD	1 OR MORE
0	1	1	0	1	1	8	EVEN	1 OR MORE
0	1	1	1	X	1	8	NONE	1 OR MORE

↳Set to ASYNC or ISOC Mode

When RMS_3 is 0 (ASYNC or ISOC Mode), RMS_2 and RMS_1 determine the clock frequency according to the following table:

RMS_2	RMS_1	CLOCK FREQUENCY
0	0	1X BAUD RATE
0	1	16X BAUD RATE
1	0	32X BAUD RATE
1	1	64X BAUD RATE

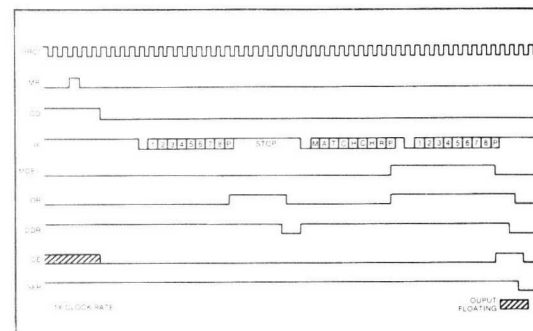

Fig.1 ASYNCHRONOUS & ISOCHRONOUS TIMING EXAMPLE

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SYNCHRONOUS MODE OPERATION

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no start or stop bits. Character synchronization is the "framing" of this continuous bit stream into characters of predetermined length.

Synchronization requires receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly. The P/SAR is designed to accommodate internal or external character synchronization by program control.

The mode of synchronization, character length and selected parity if required, is determined by loading the appropriate control bits into the Control Register. Table 2 illustrates all programmable synchronous formats.

When programmed for internal character synchronization, the Sync Search line is set to a logic '1' in order to initiate the automatic Sync Character search operation. Before synchronization takes place, the Receiver Holding register is "transparent" and its contents are identical to the Receiver Holding Register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver Register Clock (RRC) shifts through the Receiver Register and is compared with the preprogrammed character in the Match Character Holding Register. A match, indicated by a logic '1' on Match Detect (MDET), returns the Receiver Holding Register to its nontransparent state and initializes timing and Control logic. It does not set the Data Received Flag to a logic '1' level. The character following the match will be transferred to the Receiver Holding Register at the receipt of the Center of its last bit, and the Data Received Flag is set to a logic '1' level.

Depending on line discipline, this last character may also be a synchronizing character, in which case Match Detect will continue to be a logic '1', when the Data Received Flag is set. This allows sequence verification to be performed by the system.

If parity is programmed, verification takes place upon receipt of the center of the parity bit. The parity bit is the last bit of a synchronous character. If a parity error exists, the associated PE flag is set to a logic '1' level.

Transfer of a character to the Receiver Holding Register sets the associated Data Received Flag (DR) to a logic '1'. The transfer of a character to the Receiver Holding register, if the Data Received Flag had already been set to a logic '1', causes the previous character to be lost (written over) and is alerted by an Overrun Error (OE) Flag, which is at a logic '1' level. In normal operation, the Data Received Flag is reset by DRR when the Receiver Holding Register is serviced (unloaded). The status flags PE and OE, are also provided with an external reset SFR so that block status and character status may be verified. If the Sync Search line is brought to a logic '0' at any time, character synchronization will be lost and the Receiver Holding Register will become "transparent".

External Character synchronization is similar to the description above, with the exception that the Sync Search line controls the transparency of the Receiver Holding Register directly and comparison is done externally.

The system external to the P/SAR examines the data stream for Sync Characters while holding the SS line to a logic '0'. The Receiver Holding Register is "transparent" which allows the contents of the Receiver Register to be monitored as it ripples through the shift register. Upon recognition of the appropriate Sync Character, the external logic sets the Sync Search line to a logic '1' level. The low to high transition occurs during the last bit of the Sync Character. The first bit received after a logic '1' is applied to Sync Search defines the start of a "character frame". Character length defined by the Control Register defines the end of the "frame". At this point the Receiver Holding Register returns to a "non-transparent" condition. Subsequent characters are transferred to the Receiver Holding Register when the center of the last bit is recognized, which also raises the DR flag. A logic '0' on the SS line causes character synchronization to be lost and initiates transparency of the Receiver Holding Register.

Table 2
SYNC MODE CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT	
RMS3	WLS2	WLS1	PI	EPE	DATA BITS	PARITY BIT CHECKED
1	0	0	0	0	5	ODD
1	0	0	0	1	5	EVEN
1	0	0	1	X	5	NONE
1	0	1	0	0	6	ODD
1	0	1	0	1	6	EVEN
1	0	1	1	X	6	NONE
1	1	0	0	0	7	ODD
1	1	0	0	1	7	EVEN
1	1	0	1	X	7	NONE
1	1	1	0	0	8	ODD
1	1	1	0	1	8	EVEN
1	1	1	1	X	8	NONE

↑ Sets to SYNC Mode

If $RMS_1 = 1$, the receiver operates in the internal character SYNC mode.

If $RMS_1 = 0$, character SYNC must be externally provided.

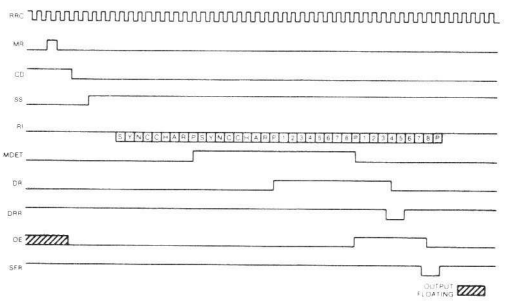

Fig. 2 SYNCHRONOUS TIMING EXAMPLE (Internal Synchronization)

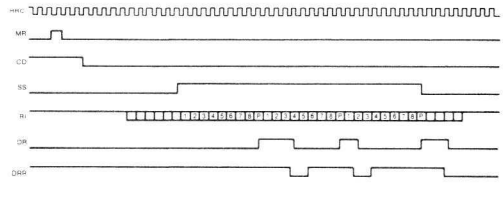

Fig. 3 SYNCHRONOUS TIMING EXAMPLE (External Synchronization)

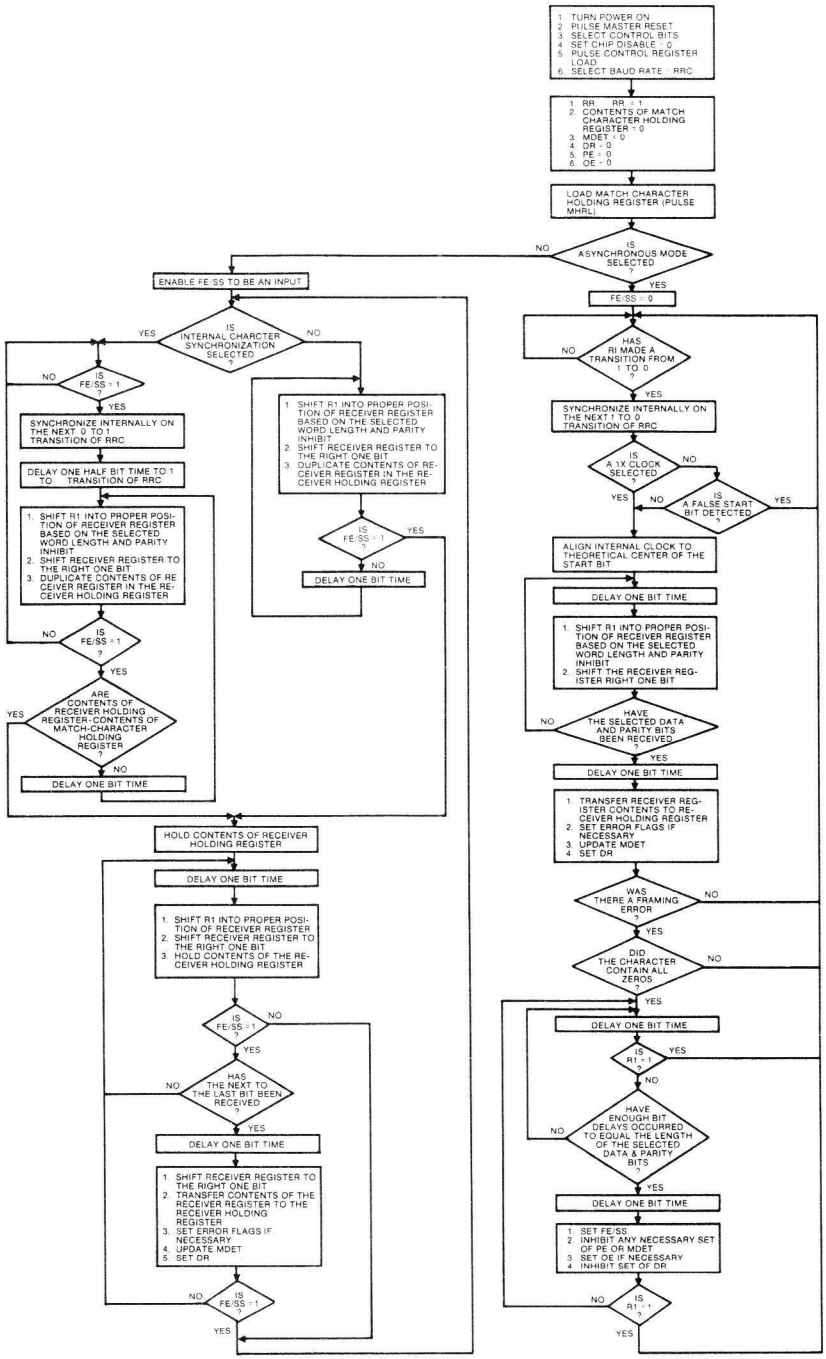

Fig. 4 FLOW CHART

ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

Maximum Ratings*

V_{GG} (with respect to V_{SS}) . . . . . −20 to +0.3V
Clock and logic input voltages (with respect to V_{SS}) . . . . . −20 to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$V_{GG} = -12V \pm 5\%$
$V_{SS} = +5V \pm 5\%$
Operating Temperature (T_A) = 0°C to 70°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
DC CHARACTERISTICS					
Input Logic Level					
Logic 0	0	–	0.8	Volts	V_{SS} = 4.75V
Logic 1	V_{SS}-1.5	–	V_{SS} + 0.3	Volts	
Input Capacitance					
All Inputs	–	–	20	pF	0 volt bias, f = 1MHz
Leakage Currents					
Tri-state Outputs	–	–	1.0	μA	0 volts
Disabled Inputs	–	–		μA	
Output Impedance					
Tri-state Outputs	1.0	–	–	MΩ	
Data Output Levels					
Logic 0	–	–	+0.4	Volts	V_{SS} = 5.25V, I_{OL} = 1.6mA (sink)
Logic 1	V_{SS}-1.0V	–	–	Volts	V_{SS} = 4.75V, I_{OH} = 100μA (source)
Output Capacitance	–	10	15	pF	
Short CKT Current	–	–	−2.2	mA	V_{SS} = 5.25 V V_{OUT} = OV
Power Supply Current					
I_{GG}	–	10	–	mA	
I_{SS}	–	15	–	mA	
AC CHARACTERISTICS					
Clock Frequency	DC	–	640	kHz	
Baud	0	–	640	kbaud	1 × Clock
Control Register Load	250	–	–	μs	See Fig. 7
Match Character					
Holding Register Load	250	–	–	ns	See Fig. 7
Master Reset	500	–	–	ns	See Fig. 6
Data Received Reset	200	–	–	ns	See Fig. 8
Hold Time	20	–	–	ns	See Fig. 7
Status Flag Rest	200	–	–	ns	See Fig. 8
Rise Time	–	–	150	ns	
Fall Time	–	–	150		
Output Enable Delay	–	–	500	ns	

** Typical values at +25°C and nominal voltages

TIMING DIAGRAMS

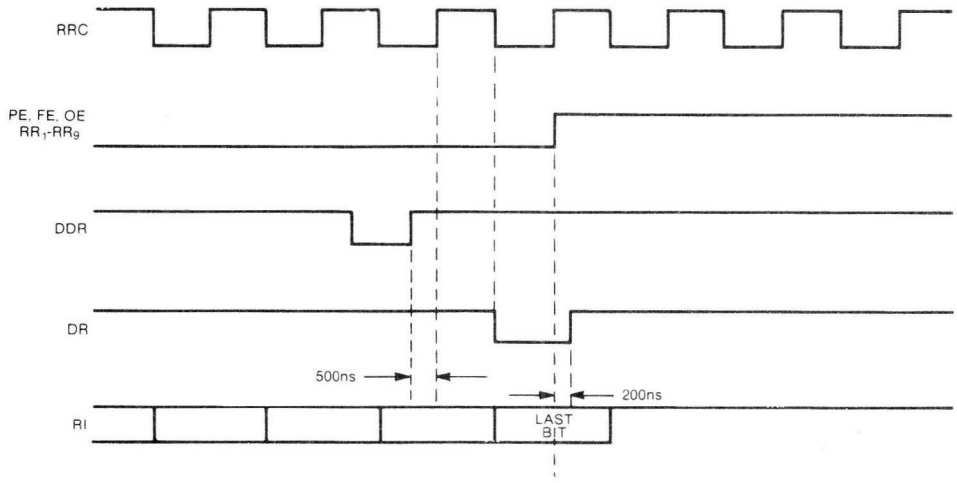

Fig. 5 P/SAR TIMING

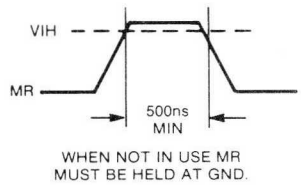

Fig. 6 MR PULSE

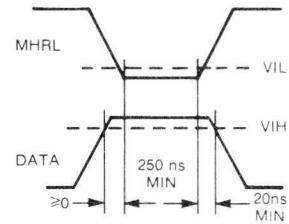

Fig. 7 DATA LOAD

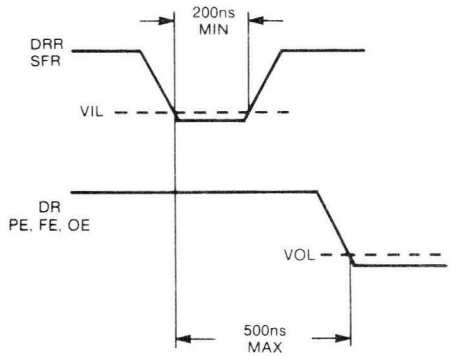

Fig. 8 DRR, SFR

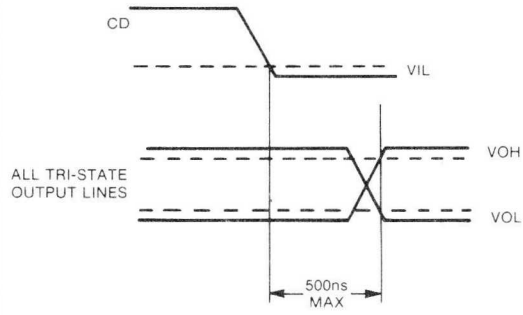

Fig. 9 CD

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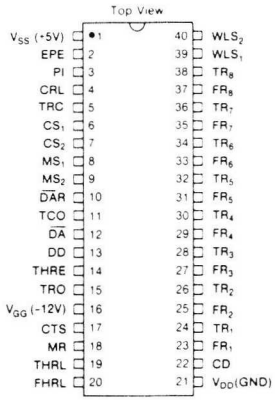
P/SAT: Programmable Synchronous Asynchronous Transmitter

FEATURES

- Directy TTL & DTL Compatible — Internal Active Input Pull-Up Devices & Push-Pull Output Buffers.
- Programmable Mode Selection —
  Synchronous — Programmable Fill (Idle) Character;
  Isochronous — Programmable Fill Character with Start & Stop Bit;
  Asynchronous — Single or Double Stop Bit Generation with 1.5 Stop Bits or 5-level Codes.
- Programmable Transmission Codes —
  Character Length of 5, 6, 7 or 8 data bits plus Parity;
  Even/Odd Parity Generation; Parity Inhibit.
- Programmable Clock Rate —
  Selectable Divider Ratios
  for 1X, 16X, 32X or 64X Clock Rate.
- DC to High Speed Operation —
  Bit Rate to 640k bits/sec. with 1 X Clock.
- Double Buffered Transmitter

PIN CONFIGURATION

40 LEAD DUAL IN LINE

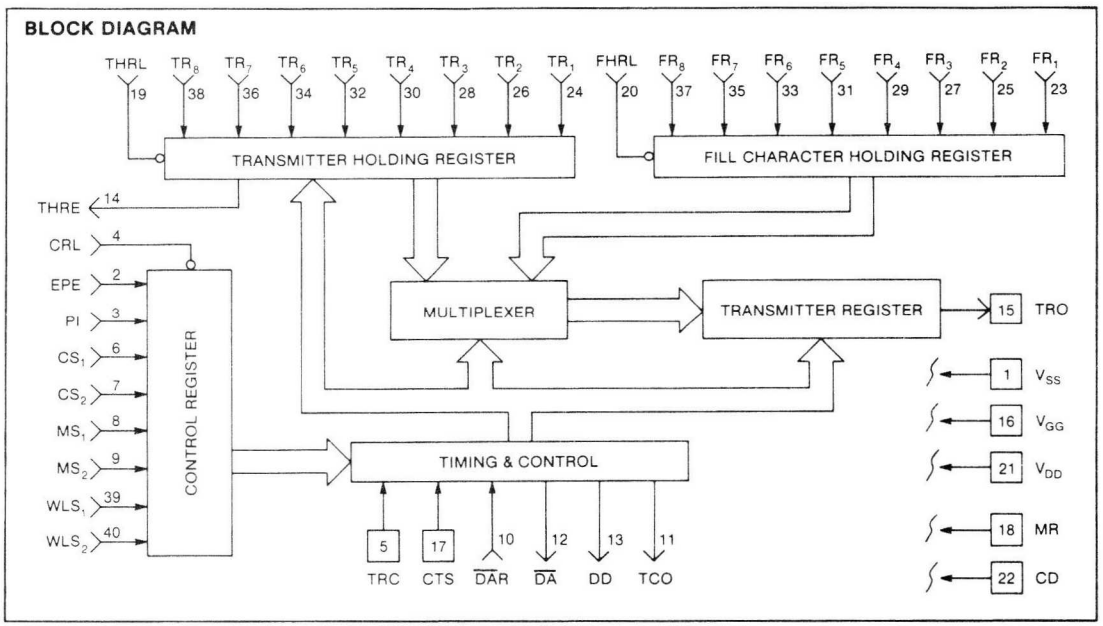


DESCRIPTION

The General Instrument AY-8-1482B P/SAT is a Programmable Transmitter that interfaces variable length parallel input data to a serial channel. The Transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isochronous data communication media.

Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous mode provides "Start-Stop" serial data transmission with automatic insertion of Start and Stop Bits(s). Isochronous mode selection provides data transmission with a single Start and Stop Bit with the added capability of programmable Fill (Idle) Character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Tri-State Output Lines, provide full system versatility.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{SS} Power Supply (V_{SS})	+5 volt supply
2	Even Parity Enable (EPE)	The logic level on this pin selects the type of parity which will be inserted immediately after the data bits. A logic '0' will insert odd parity and a logic '1' will insert even parity.
3	Parity Inhibit (PI)	A logic '1' on this pin will eliminate the parity bit from the transmitted character. If not used, this lead must be tied to a logic '0'.
4	Control Register Load Strobe (CRL)	A logic '0' on this pin will enter the control bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2) into the Control Register. This line can be strobed or hard wired to a logic '0' level.
5	Transmitter Register Clock (TRC)	This is a fifty (50) percent duty cycle clock. The positive going edge of this clock shifts data out of the Transmitter Register at a rate determined by the Control Bits CS_1, and CS_2.
6-7	Clock Rate Select (CS_1 - CS_2)	These two pins select the internal clock rate divider ratio to produce the transmitter bit rate. CS_2 — CS_1 — BIT RATE 0 — 0 — 1 X Clock Rate 0 — 1 — 16 X Clock Rate 1 — 0 — 32 X Clock Rate 1 — 1 — 64 X Clock Rate
8-9	Mode Select (MS_1 - MS_2)	These two pins select the transmitter operating mode. MS_2 — MS_1 — MODE 0 — 0 — Asynchronous — One stop bit 0* — 1* — Asynchronous — Two stop bits 1 — 0 — Synchronous 1 — 1 — Isochronous * Selects 1½ stop bits for 5 bits per character
10	Data not available Reset ($\overline{DAR}$)	A logic '0' on this pin will reset the Data Not Available Flag.
11	Transmitter Clock Output (TCO)	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive edge corresponds to the start of each data bit transition. All wave forms in this specification are referenced to TCO.
12	Data not Available Flag ($\overline{DA}$)	A logic '1' on this pin indicates that a Fill Character has been transmitted. This occurs when a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character or the center of the Stop Bit of an Isochronous character.
13	Data Delimit/End of Character (DD/EOC)	During Asynchronous or Isochronous operation, a logic '1' indicates data is being transmitted. A logic '0' indicates a start or stop bits are being transmitted. A low-level output voltage during synchronous operation indicates that the last bit of a character is being transmitted.
14	Transmitter Holding Register Empty (THRE)	A logic '1' on this pin indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a logic '0' level when THRL goes to a logic '0'.
15	Transmitter Register Output (TRO)	The contents of the Transmitter Holding Register and/or the Fill Character Holding Register are serially shifted out as an NRZ waveform.
16	V_{GG} Power Supply (V_{GG})	−12 volt supply
17	Clear-To-Send (CTS)	A logic '1' on this pin initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A logic '0' applied to this pin during transmission allows completion of that character only, after which the output will continue to mark until a logic '1' is applied.
18	Master Reset (MR)	A logic '1' on this pin will reset timing and control logic to an idle state, and sets THRE, the contents of the Fill Character Holding Register, and TRO to a logic '1' level. Must be tied to logic '0' when not used.
19	Transmitter Holding Register Load Strobe (THRL)	A logic '0' applied to this line enables DC latches of the Transmitter Holding Register and loads it with the Transmitter data TR_1 -TR_8, and forces THRE to a logic '0' level. A logic '1' applied to this line disables the transmitter holding register.
20	Fill-Character Holding Register Load Strobe (FHRL)	A logic '0' applied to this pin enables DC latches of the Fill Character Holding Register and loads it with the Fill Character data FR_1, - FR_8. A logic '1' applied to this line disables the Fill Character Register. This line may be strobed or hardwired to a logic '0'
21	V_{DD} Power Supply (V_{DD})	Ground
22	Chip Disable (CD)	A logic '1' applied to this pin will disable the busable inputs and tri-state outputs The I/O lines controlled by Chip Disable are:

PIN FUNCTIONS cont'd

Pin No.	Name (Symbol)	Function
		Input Lines — **Tri-State Outputs** CRL THRL EPE FHRL — $\overline{DA}$ PI FR_1 - FR_8 CS_1-CS_2 TR_1-TR_8 — THRE MS_1-MS_2 WLS_1-WLS_2 $\overline{DAR}$ Must be tied to logic '0' when not used.
23, 25, 27, 29, 31, 33, 35, 37.	Fill Character Holding Register Data Inputs (FR_1 - FR_8)	Parallel 8-bit characters are loaded into the Fill Character Holding Register. If a character of less than 8-bits has been selected, only the least significant bits are accepted.
24, 26, 28, 30 32, 34, 36, 38.	Transmitter Holding Register Data Inputs (TR_1 - TR_8)	Parallel 8-bit characters are loaded into the Transmitter Holding Register. If a character of less than 8-bits has been selected, only the least significant bits are accepted.
39, 40	Word Length Select (WLS_1 - WLS_2)	These two pins select the number of bits per character. **WLS_2** **WLS_1** **Selected Word Length** 0 0 5-bits 0 1 6-bits 1 0 7-bits 1 1 8-bits

ASYNCHRONOUS MODE OPERATION

An asynchronous character consists of a start bit, followed by 5 to 8 data bits, parity (if so programmed), and either 1 or 2 stop bits. The combined selection of 2 stop bits and 5-bits per character will produce 1½ stop bits.

The P/SAT will enter a defined "idle" state when the Master Rest (MR) is strobed to a logic '1' level. At this point, all timing and control logic are reset, the Transmitter Register Output continues to mark, the THRE flag is set to a logic '1' and the DD/EOC flag is reset to a logic '0'.

When the transmitter is enabled by CD, the control bits are loaded into the Control Register by strobing the CRL line to a logic '0'. The Control bits define the mode of operation, character length, selected parity, if required, and the clock rate selection. Table 1 summarizes all the programmable asynchronous formats for any one clock rate.

Transmission of characters with the minimum number of stop bits programmed is accomplished by loading the Transmitter Holding Register within a character of when the THRE flag goes to a logic '1' level. A logic '1' level on the THRE flag indicates that the Transmitter Holding Register is empty and may be loaded with a new character. Data on the inputs of the Transmitter Holding Register is loaded when the THRL line is strobed to a logic '0', forcing the THRE flag to a logic '0'. This data must be stable prior to THRL going to a logic '1' since this register is a set of DC latches which are enabled by THRL If the Clear-To-Send (CTS) line is at a logic '0' level, or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE flag will remain at a logic '0' level. Raising the CTS line to a logic '1' level and completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register and the THRE flag wil be set to a logic '1' level.

A logic '0' applied to CTS during transmission allows completion of that character only, after which the output will continue to mark until a logic '1' is applied.

Table 1
ASYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT			
MS2	MS1	WLS2	WLS1	PI	EPE	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
0	0	0	0	0	0	1	5	ODD	1
0	1	0	0	0	0	1	5	ODD	1½
0	0	0	0	0	1	1	5	EVEN	1
0	1	0	0	0	1	1	5	EVEN	1½
0	0	0	0	1	X	1	5	NONE	1
0	1	0	0	1	X	1	5	NONE	1½
0	0	0	1	0	0	1	6	ODD	1
0	1	0	1	0	0	1	6	ODD	2
0	0	0	1	0	1	1	6	EVEN	1
0	1	0	1	0	1	1	6	EVEN	2
0	0	0	1	1	X	1	6	NONE	1
0	1	0	1	1	X	1	6	NONE	2
0	0	1	0	0	0	1	7	ODD	1
0	1	1	0	0	0	1	7	ODD	2
0	0	1	0	0	1	1	7	EVEN	1
0	1	1	0	0	1	1	7	EVEN	2
0	0	1	0	1	X	1	7	NONE	1
0	1	1	0	1	X	1	7	NONE	2
0	0	1	1	0	0	1	8	ODD	1
0	1	1	1	0	0	1	8	ODD	2
0	0	1	1	0	1	1	8	EVEN	1
0	1	1	1	0	1	1	8	EVEN	2
0	0	1	1	1	X	1	8	NONE	1
0	1	1	1	1	X	1	8	NONE	2

Sets to ASYNC Mode

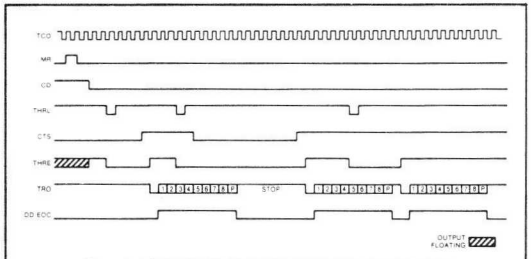


Fig. 1 ASYNCHRONOUS TIMING EXAMPLE

SYNCHRONOUS MODE OPERATION

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits, plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiguous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding Register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding Register. This character is defined as the Fill or idle Character, and a separate register has been provided to load this character upon initialization. The Fill-Character Holding Register is loaded by strobing the Fill-Character Register Load (FHRL) line or hard-wiring it to a logic '0'. Table 2 illustrates all the programmable synchronous character formats for any one clock rate.

To initialize transmission the CTS signal must be set to a high state and the transmitter holding register must be loaded with a character to be transmitted. The transmitter will remain in an idle state until this is accomplished.

The character transferred into the Transmitter Register, from either the Transmitter Holding Register or the Fill-Character Holding Register, is determined at the center of the last bit of the character being transmitted. If at this time, no character has been loaded into the Transmitter Holding Register, the Fill-Character is loaded into the Transmitter Register at the end of the bit being transmitted and the Data Not Available ($\overline{DA}$) Flag is set to a logic '1' level. The Fill-Character will be repeatedly transmitted until a character is loaded into the Transmitter Holding Register, at which time the Fill-Character will be completed and the newly loaded synchronous character will follow. The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. The DD/EOC Flag is defined as a logic '0' during transmission of the last bit of a synchronous character and when the P/SAT is in the "idle" state.

Table 2
SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
MS2	MS1	WLS2	WLS1	PI	EPE	DATA BITS	ADDED PARITY BIT
1	0	0	0	0	0	5	ODD
1	0	0	0	0	1	5	EVEN
1	0	0	0	1	X	5	NONE
1	0	0	1	0	0	6	ODD
1	0	0	1	0	1	6	EVEN
1	0	0	1	1	X	6	NONE
1	0	1	0	0	0	7	ODD
1	0	1	0	0	1	7	EVEN
1	0	1	0	1	X	7	NONE
1	0	1	1	0	0	8	ODD
1	0	1	1	0	1	8	EVEN
1	0	1	1	1	X	8	NONE

Sets to SYNC Mode

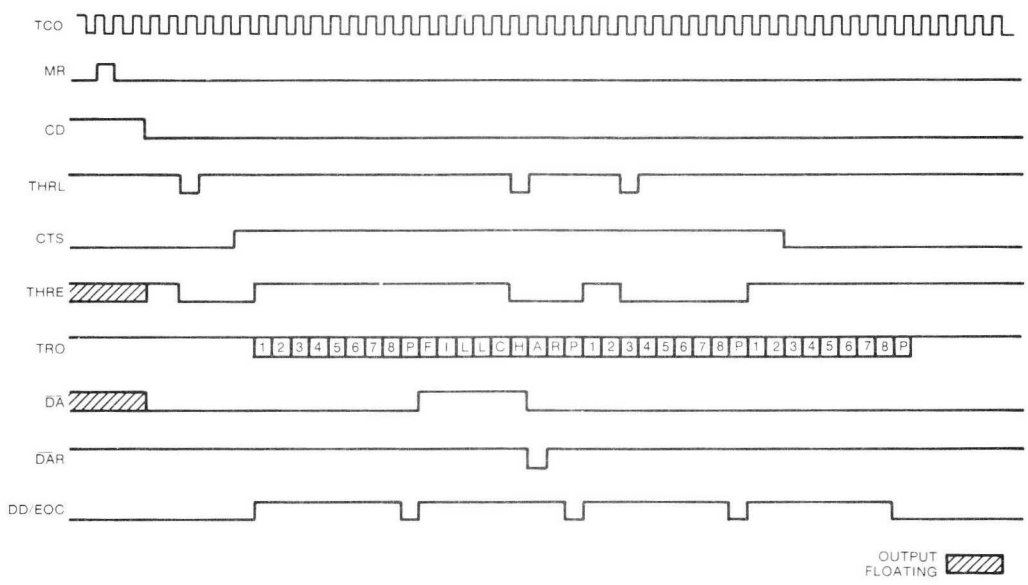


Fig. 2 SYNCHRONOUS TIMING EXAMPLE

ISOCHRONOUS MODE OPERATION

In the Isochronous Mode of operation all Synchronous Mode definitions apply with the exception of those for Data Delimit/End of Character (DD/EOC) Flag and the Data Not Available ($\overline{DA}$) Flag.

Isochronous Data Transmission requires contiguous characters with the addition of a start and a single stop bit added to each character.

The DD/EOC Flag is at a logic '0' level during start and stop bits, and is a logic '1' during transmission of data and parity. The $\overline{DA}$ Flag is set to a logic '1' level at the end of the stop bit if a character has not been loaded into the Transmitter Holding Register at the center of the stop bit. The contents of the Fill Character Holding Register will be transferred into the Transmitter Register and repeatedly transmitted until a character is loaded into the Transmitter Holding Register. At this time the Fill-Character will be completed and the newly loaded isochronous Character will follow.

Table 3 summarizes all the programmable isochronous character formats for any one Clock rate.

Table 3
ISOC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT			
MSB 2	MSB 1	WLS 2	WLS 1	PI	EPE	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
1	1	0	0	0	0	1	5	ODD	1
1	1	0	0	0	1	1	5	EVEN	1
1	1	0	0	1	X	1	5	NONE	1
1	1	0	1	0	0	1	6	ODD	1
1	1	0	1	0	1	1	6	EVEN	1
1	1	0	1	1	X	1	6	NONE	1
1	1	1	0	0	0	1	7	ODD	1
1	1	1	0	0	1	1	7	EVEN	1
1	1	1	0	1	X	1	7	NONE	1
1	1	1	1	0	0	1	8	ODD	1
1	1	1	1	0	1	1	8	EVEN	1
1	1	1	1	1	X	1	8	NONE	1

Sets to ISOC Mode

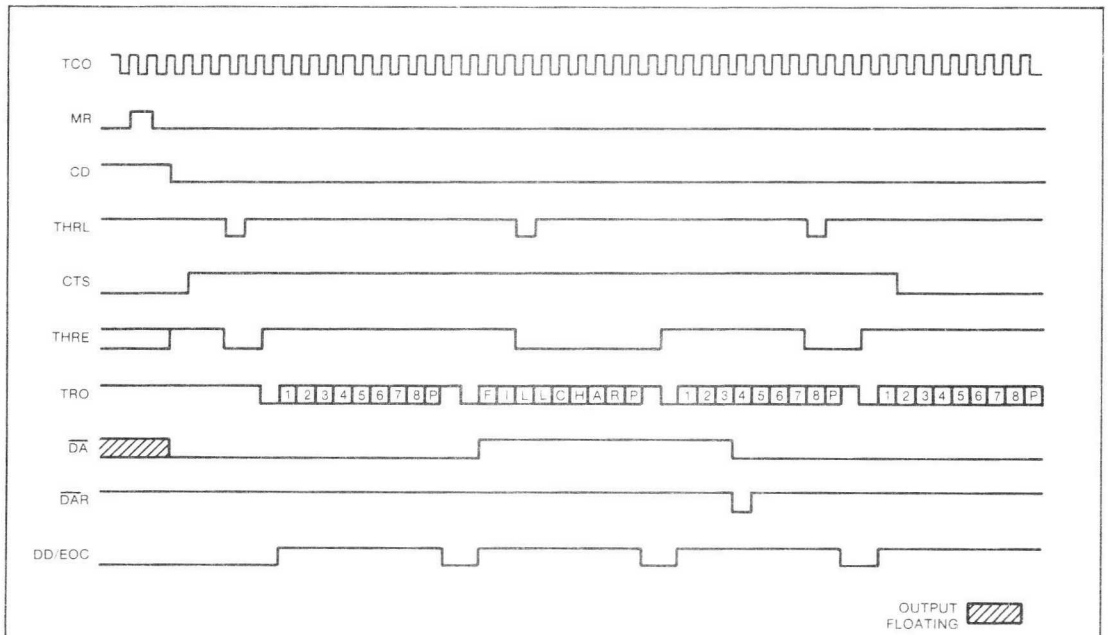


FIG. 3 ISOCHRONOUS TIMING EXAMPLE

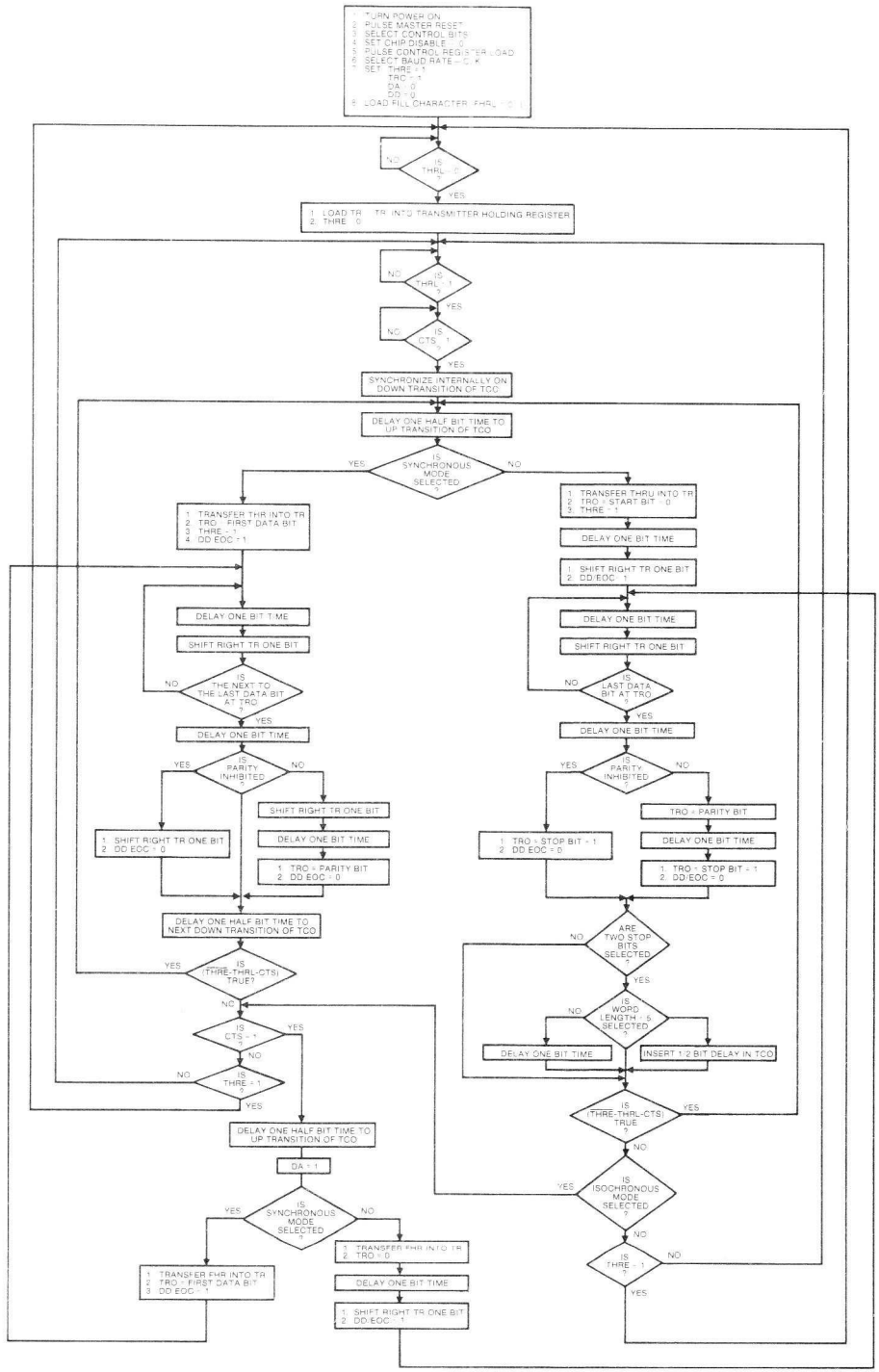


Fig. 4 FLOW CHART

ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

Maximum Ratings*

V_{GG} (with respect to V_{SS}) . . . . . −20 to +0.3V
Clock and logic input voltages (with respect to V_{SS}) . . . . . −20 to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$V_{GG} = -12V \pm 5\%$
$V_{SS} = +5V \pm 5\%$
Operating Temperature (T_A) = 0°C to + 70°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
DC CHARACTERISTICS					
Input Logic Level					
Logic 0	0	–	0.8	Volts	V_{SS} = 4.75V
Logic 1	V_{SS}-1.5	–	V_{SS} +0.3	Volts	
Input Capacitance					
All inputs	–	–	20	pF	0 volt bias, f = 1MHz
Leakage Currents					
Tri-state outputs	–	–	1.0	μA	0 volts
Disabled Inputs	–	–		μA	
Output Impedance					
Tri-state Outputs	1.0	–	–	MΩ	
Data Output Levels					
Logic 0	–	–	+0.4	Volts	V_{SS} = 5.25V, I_{OL} = 1.6mA (sink)
Logic 1	V_{SS}-1.0	–	–	Volts	V_{SS} = 4.75V, I_{OH} = 100μA (source)
Output Capacitance	–	10	15	pF	
Short Ckt Current	–	–	−2.2	mA	V_{SS} = 5.25V, V_{out} = 0V
Power Supply Current					
I_{GG}	–	10	–	mA	
I_{SS}	–	25	–	mA	
AC CHARACTERISTICS					
Clock Frequency	DC	–	640	kHz	
Baud	0	–	640	K baud	1 × Clock
Pulse Width					
Control Register Load	250	–	–	ns	See Fig. 7
Transmitter Holding Register Load	250	–	–	ns	See Fig. 7
Fill-Char. Holding Register Load	250	–	–	ns	See Fig. 7
Master Reset	500	–	–	ns	See Fig. 6
Data Not Available Reset	200	–	–	ns	
Hold Time	20	–	–	ns	See Fig. 7
Skew Time	–	–	250	ns	See Fig. 9
Rise Time	–	–	150	ns	
Fall Time	–	–	150	ns	
Output Enable Delay	–	–	500	ns	See Fig. 8

** Typical values at +25°C and nominal voltages

TIMING DIAGRAMS

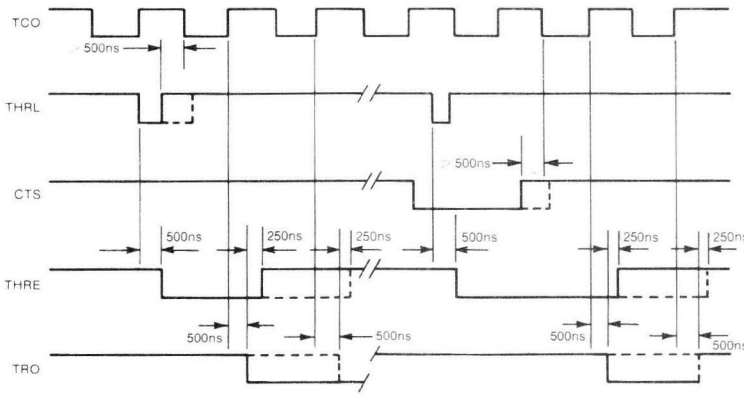


Fig. 5 P/SAT TIMING

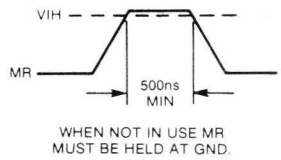


Fig. 6 MR PULSE

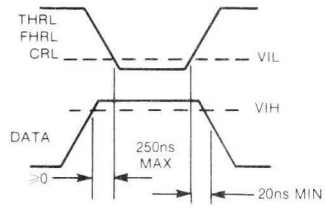


Fig. 7 DATA LOAD

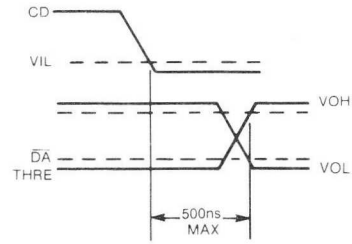


Fig. 8 CD

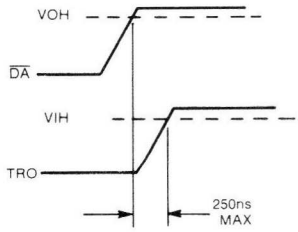


Fig. 9 SKEW TIME

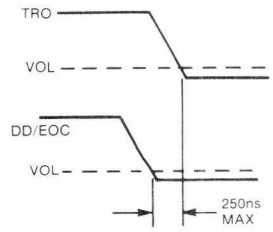


Fig. 10 DD/EOC TURN-OFF

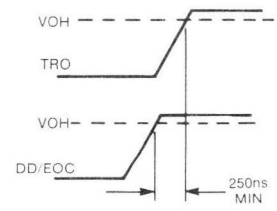


Fig. 11 DD/EOC TURN-ON

Random/Sequential Access Multiplexers

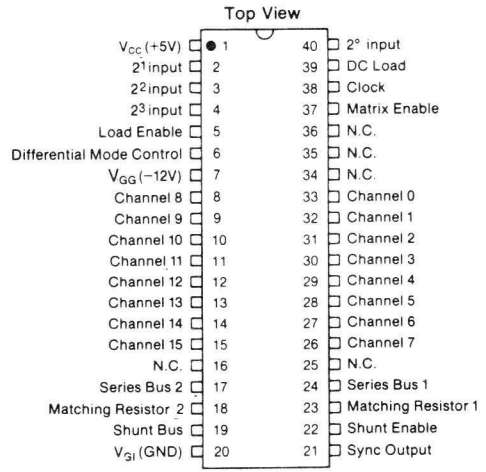
FEATURES

- Directly interfaces with TTL/DTL and MOS
- Current or voltage modes of operation
- Random or sequential access
- Single ended or differential operation
- Expandable in either the sequential or random access modes
- Programmable length counter for sequential applications
- DC to 2MHz operation
- Extremely high off-resistance
- Choice of Operating Temperature Ranges:
  AY-5-1016 — 0°C to +70°C
  AY-6-4016 — −55°C to +125°C
- Zener network protection on all input leads

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

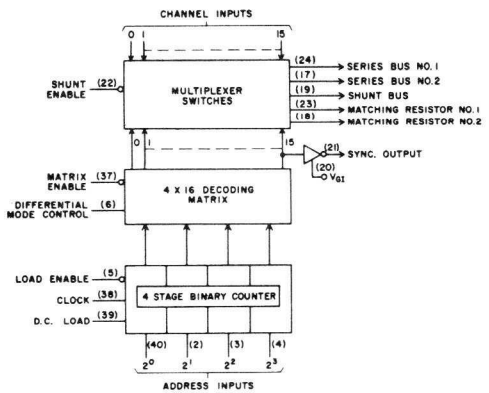


DESCRIPTION

The AY-5-1016 and AY-6-4016 are each a 16 Channel Random/Sequential Access Multiplexer containing a programmable 4 stage binary counter, a 4 × 16 decode matrix, and 16 single-pole double-throw switches.

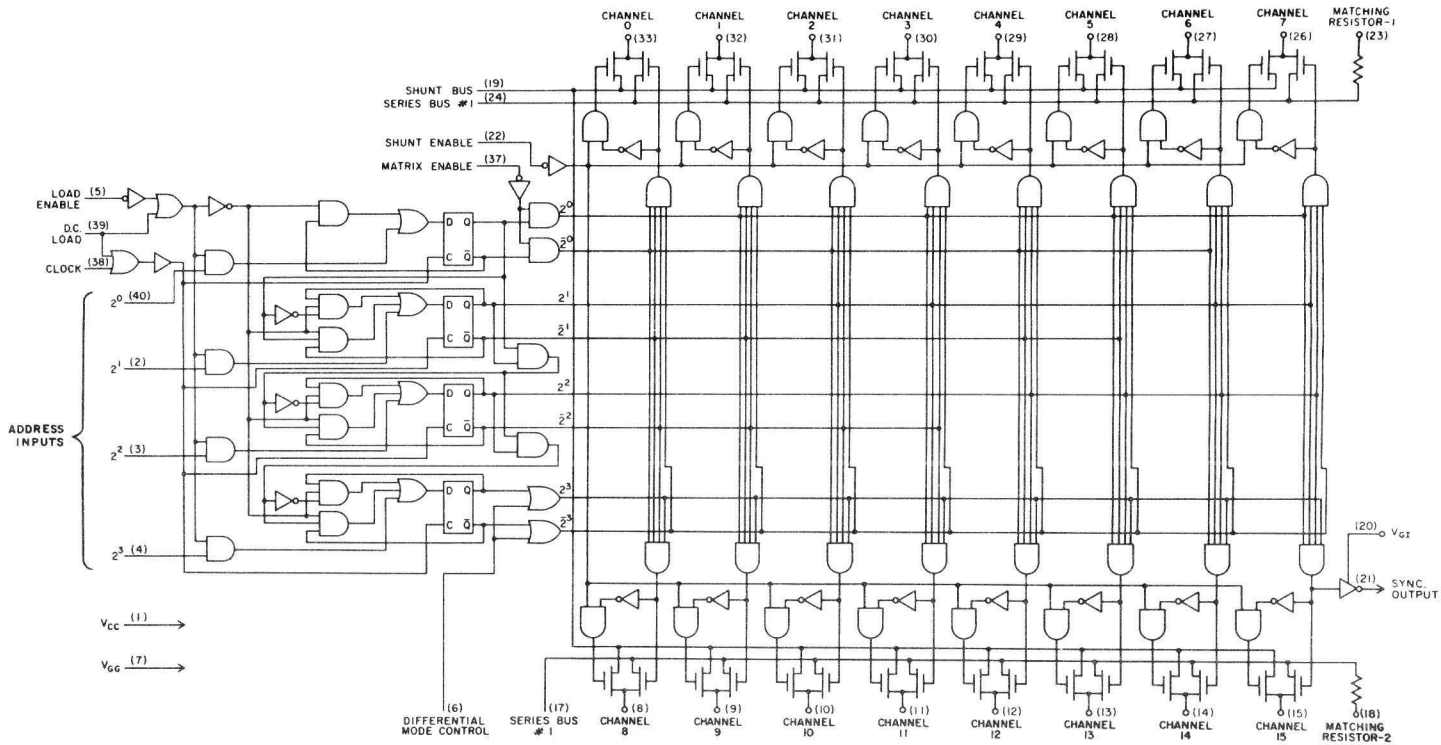
The Shunt Enable control line permits the selection of Current Mode or Voltage Mode operation and in conjunction with the Current Mode, matching resistors are provided to improve accuracy. The Differential Mode Control allows the switches to operate as eight ganged pairs, while the Matrix Inhibit line allows multiple AY-5-1016's (or AY-6-4016's) to be connected to form larger multiplexing arrays. The Load Enable control allows synchronous loading of the 4 address inputs on a low to high transition of the Clock. The DC load control is provided for asynchronous loading of the address inputs independent of the Clock and Load Enable inputs. The Sync Output occurs whenever Channel 15 is selected and is provided to allow expansion in the sequential mode of operation. Also by connecting the Sync Output to the Load Enable Input, the counter length can be programmed via the address inputs. Any desired length of from 1 to 16 states can be programmed in this manner.

BLOCK DIAGRAM



LOGIC DIAGRAM

( ) = Pin Numbers



NOTES:

1. Direct Address gated when either DC Load = "1" or Load Enable = "0".
2. DC Load gives permanent high clock.
3. Matrix Enable = "1" inhibits matrix.
4. Shunt Enable = "0" connects shunt FETS into circuit.
5. Differential Mode Control = "1" connects channels 8-15 ganged to channels 0-7.
6. Sync Output = "0" when channel 15 is accessed.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Clock and Logic Input Voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Bus Voltages (Bus 1, Bus 2, and Shunt Bus with respect to V_{CC}) . . . −20V to .3V
Matching Resistor Nodes (with respect to V_{CC}) . . . . . −20V to .3V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature Range: . . . . . 0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} = Substrate voltage)
V_{GG} = −12 Volts ±1 Volt
V_{GI} = GND

Operating Temperature (T_A) = −0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Inputs (See Fig.1)					
Repetition Rate	DC	—	2.0	MHz	
Clock Pulse Width (ϕpw)	200	—	—	ns	at 2MHz, (See NOTE 1)
Clock Pulse Width (ϕpw)	1.0	—	—	μs	at 200Hz
Clock Pulse Delay (ϕd)	200	—	—	ns	See NOTE 1
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	12	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Rise & Fall Time (tr, tf)	—	—	1.0	μs	at 100KHz
Rise & Fall Time (tr, tf)	—	—	50	ns	at 2MHz
Noise Immunity	+0.4	—	—	V	
Address Inputs (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
Load Enable Input (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
DC Load Input (See Fig.2)					
Pulse Width (90% points)	400	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	8	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	

**Typical values are at +25°C and nominal voltages.
NOTE 1: ϕpw + ϕd ≥ 500ns

TIMING DIAGRAMS

Fig.1

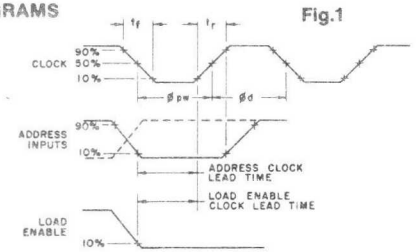
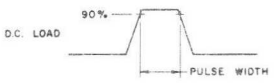


Fig.2



NOTE: Address Inputs and the Load Enable Input must be present during the 0 to 1 transition of the Clock.

Characteristic	Min	Typ**	Max	Units	Conditions
Shunt Enable					
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
Matrix Enable					
Response Time (See Fig. 3)					
T_{ON}	—	230	—	ns	} at 25°C Output voltage
T_{OFF}	—	120	—	ns	} response with10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN}= +5V to −V
Noise Immunity	+0.4	—	—	V	
Differential Mode Control					
Response Time (See Fig. 4)					
T_{ON}	—	200	—	ns	} at 25°C Output voltage
T_{OFF}	—	600	—	ns	} response with 10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	5	—	pF	
Input Impedance	1.0	—	—	MΩ	
Noise Immunity	0.4	—	—	V	
Series Switches					
R on (Current Mode)	—	460	750	Ω	I_{IN} = 100 μA Series Bus 1 = Series Bus 2 = OV (V_{CC} −5V) T_A = 25°C V_{CC} = +5V V_{GG} = 12V
R on (Voltage Mode)	—	300	500	Ω	V_{IN} = +5V, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{GG} = −12V
	—	460	750	Ω	V_{IN} = OV, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{GG} = −12V
R off	—	5	—	GΩ	V_{IN} = V_{CC} −10V T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load T_A = 25°C

**Typical values are at 25°C and nominal voltages.

TIMING DIAGRAMS

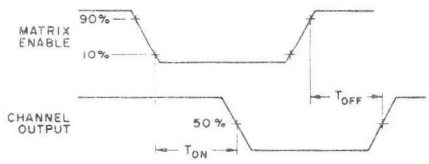


Fig.3

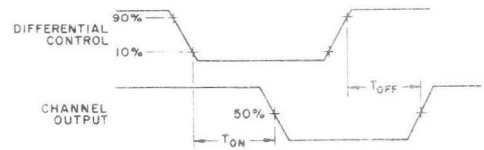


Fig.4

TELECOM

Characteristic	Min	Typ**	Max	Units	Conditions
Sync Output (See Fig.5)					
Logic "0"	—	—	+0.4	V	C = 10pF, I_{SINK} = 1.6mA min., I_{OF} = 100 μA min. } Output Load
Logic "1"	V_{CC}−1.0	—	—	V	
Rise Time (tr)	—	110	—	ns	at 25°C
Fall Time (tf)	—	40	—	ns	at 25°C
Response Time					
tpd −	—	200	—	ns	at 25°C
tpd +	—	160	—	ns	at 25°C
Input Leakage					
Channels 0-15 (Per Channel)	—	1.0	10	nA	V_{IN} = V_{CC} −5V at 25°C
Series Bus 1, 2	—	3.0	30	nA	V_{BUS} = V_{CC} −5V at 25°C
Shunt Bus	—	3.0	30	nA	V_{BUS} = V_{CC} −5V at 25°C
Shunt Switches					
R on	—	850	1300	Ω	I_{IN} = 100 μA, Shunt Bus = OV, V_{CC} = +5V, V_{GG} = −12V, T_A = 25°C
	—	550	900	Ω	I_{IN} = 100 μA, Shunt Bus = +5V, V_{CC} = +5V, V_{GG} = −12V, T_A = 25°C
R off	—	5	—	GΩ	V_{IN} = V_{CC} −10V, T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load, T_A = 25°C
Matching Resistors	—	460	750	Ω	i_{IN} = 100 μA, V_{BUS} = OV
R on	—	300	500	Ω	I_{IN}= 100 μA, V_{BUS} = +5V
Channel Input Capacitance, Channels 0-15 (Per Channel)	—	4	—	pF	
Power Consumption	—	200	—	mW	Series MODE, V_{GG} = −12V, V_{CC} = +5V
	—	290	—	mW	Shunt MODE, V_{GG} = −12V, V_{CC} = +5V
Current Drain					
I_{CC}	—	12	—	mA	Series MODE, V_{GG} = −12V, V_{CC} = +5V
I_{GG}	—	12	—	mA	Series MODE, V_{GG} = −12V, V_{CC} = +5V
I_{CC}	—	17	—	mA	Shunt MODE, V_{GG} = −12V, V_{CC} = +5V
I_{GG}	—	17	—	mA	Shunt MODE, V_{GG} = −12V, V_{CC} = +5V
Power Dissipation (Device)	—	—	600	mW	
Per Channel	—	—	100	mW	

Typical values are at 25°C and nominal voltages.

TIMING DIAGRAMS

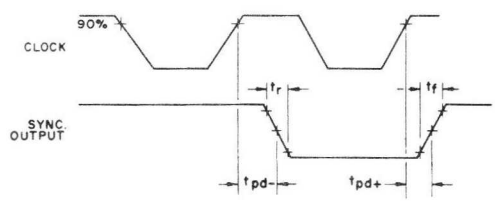
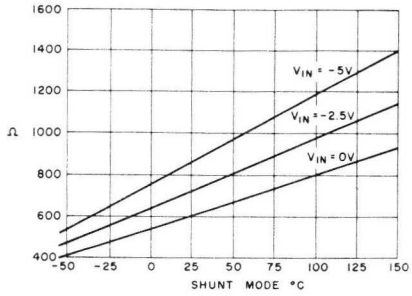
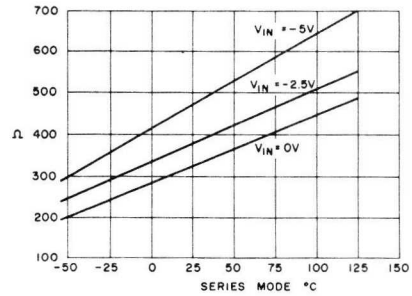
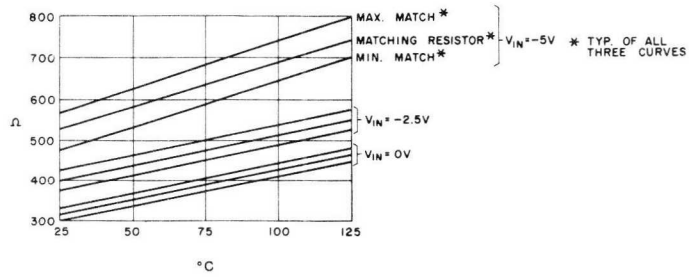


FIG.5

TYPICAL CHARACTERISTIC CURVES



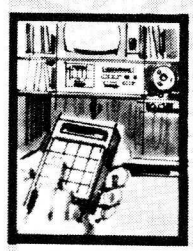


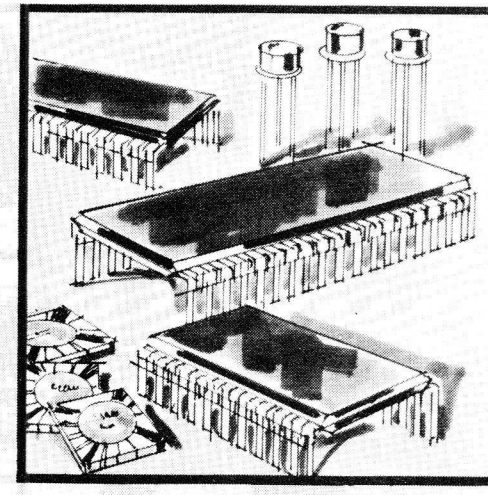


TELECOM

ENTERTAINMENT 6

Radio 6- 3
Television 6-29
Remote Control 6-61





RADIO

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
FREQUENCY COUNTERS	Counts & displays MW, SW, and VHF frequencies.	AY-5-8100	6-4
		AY-5-8102	6-4
FREQUENCY COUNTERS WITH CLOCK	Counts and displays AM/FM frequencies, with a 4-digit clock.	AY-3-8110	6-8
		AY-3-8112	6-8
		AY-3-8114	6-8
STEREOMEGA PLL DIGITAL TUNING SYSTEM	Provides full electronic control of a varactor-tuned AM/FM radio. Includes storage of 5 AM & 5 FM "favorite" stations.	AY-3-8115	6-12
		ER1400	6-20
		AY-3-8116	6-23
		AY-3-8117	6-26

Radio Receiver Frequency Counter / Display Drivers

FEATURES

- Three frequency ranges: MW 2999kHz, SW 29.995MHz, VHF 299.95MHz.
- IF offset: 460kHz (AY-5-8100) or 455kHz (AY-5-8102) on MW and SW, 10.7MHz on VHF.
- Channel mode 0-99 channel spacing 300kHz. Standard part channel 0 is 87MHz.
- High voltage segment and digit outputs give direct drive of fluorescent displays.
- Inversion control for segment outputs.
- Direct drive of liquid crystal displays.
- 1.28MHz master clock input frequency.
- 300kHz input with 8ms sample time.
- TTL compatible inputs and outputs.
- 50Hz output to drive the AY-5-1200A digital clock.

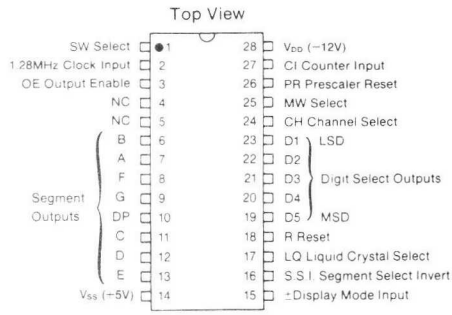
DESCRIPTION

The AY-5-8100/8102 are 4½ digit frequency counters for use in Radio Receivers. Three main frequency ranges are provided: 2999kHz and 29.995MHz (with a 460kHz IF offset on the AY-5-8100 and a 455kHz IF offset on the AY-5-8102) and 299.95MHz with a 10.7MHz IF offset. For use in VHF FM receivers a channel mode is available. In this mode a channel number from 0 to 99 is displayed together with a "+" or "−" sign for tuning indication. In this mode the IF is 10.7MHz and channel 0 is 87MHz.

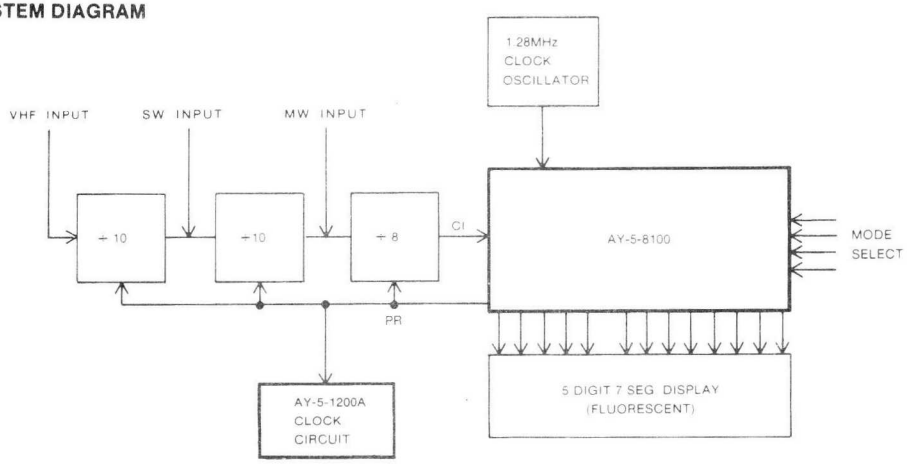
The outputs are multiplexed in five time slots onto a seven segment bus. Digit and segment outputs have high voltage capability and will drive fluorescent displays directly. A pin option allows the driving of liquid crystal displays using the two-frequency multiplexing system.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	SW Select	Selects 29.995MHz counter range when at logic '0'. See Mode Select truth table.
2	1.28MHz Clock	Master clock input controls timing of whole system.
3	Output Enable	Disables the outputs when taken to logic '0'.
4	N.C.	
5	N.C.	
6-13	Segment Outputs	The digits to be displayed are output on these pins in 7 segment code. They are at logic '1' to display. These outputs will also drive fluorescent, liquid crystal and low current LED displays.
14	V_{SS}	Positive supply.
15	±Display Mode Input	Selects either combined or separate + or − display when in channel mode. Logic '0' selects combined mode. In the combined mode the horizontal bar is output on segment "g" and the vertical bar on segment "f". In the separate mode the − sign is output on segment "g" and the + sign on segment "f".
16	Segment Select Invert	When taken to logic '1' inverts the Segment Select outputs (Note 1).
17	Liquid Crystal Select	When taken to logic '1' the output timing is arranged to drive liquid crystal displays using two frequency multiplexing.
18	Reset	Master reset to all counters and registers. Resets when at logic '1'.
19-23	Digit Select Outputs D1-D5	These outputs sequentially select the digit to be displayed. They are normally at logic '1' to display. The outputs are high voltage and are capable of driving fluorescent and liquid crystal displays directly. Each digit is on for 4ms. A bonding option gives inverted outputs.
24	Channel Select	Selects channel mode when at logic '0' and SW and MW are at logic '1'. See Mode Select truth table.
25	MW Select	Selects 2999kHz counter range when at logic '0'. See Mode Select truth table.
26	Prescaler Reset	This output resets the external prescaler divider, at logic '0' during count interval.
27	Counter Input	Frequency measuring input. Frequency range 10kHz to 600kHz.
28	V_{DD}	Negative supply.

NOTE:
1. If the digit invert bonding option is used (bonding to logic '1') the SSI input logic sense will be inverted.

FREQUENCY COUNTER OPERATION

The frequency counter section is intended to work with an external prescaler. The three frequency ranges require division ratios of 8, 80 and 800. The appropriate IF offset is loaded into the counter before measuring. The local oscillator must always be at a higher frequency than the receiver frequency.

Measurement period	8m
Reading rate	50 per second
Master clock frequency	1.28MHz

Mode	Display Range D5	D4	D3	D2	D1		Discrimination	Prescaler	IF
MW	2	9	9	9		kHz	1kHz	÷ 8	460
SW	2	9 •	9	9	5	MHz	5kHz	÷ 80	460
FM	2	9	9 •	9	5	MHz	50kHz	÷800	10.7
CH	±	9	9				300kHz	÷800	10.7
COUNT	2	9	9	9	5		0.5kHz	÷ 8	10

NOTES:
1. Leading zeros are blanked.
2. In Channel Mode the + or - signs are lit if the receiver is more than 50 kHz off tune.
3. The IF offset is mask programmed and can in principle be made to any value.
4. In Channel Mode, Channel 0 = 87 MHz.

MODE SELECTION

MW	SW	CH	OE	Mode
0	1	X	1	MW
1	0	X	1	SW
1	1	1	1	VHF
1	1	0	1	VHF/Channel
0	0	0	1	Counter mode
X	X	X	0	Clock

DISPLAY OUTPUT

The output is in 7 segment form multiplexed into five time slots at a rate of 50Hz. All the display outputs have high voltage capability and will drive fluorescent displays directly. LED displays can either be driven directly or with simple interfacing depending on the digit size.

A pin selected option allows the direct driving of liquid crystal displays using two frequency multiplexing (125Hz and 8000Hz).

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Digit Outputs) . . . . . +0.3V to −20V
Voltage on Segment and Digit Outputs with respect to V_{SS} pin . . . +0.3V to −35V
Ambient operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C
Power dissipation. 600mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

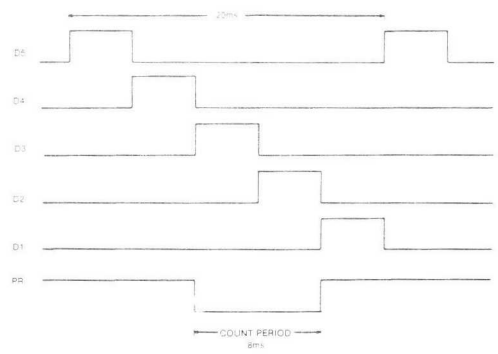
V_{SS} = +5V ±0.5V
V_{DD} = −12V ±1V
} or: $V_{SS} - V_{DD}$ = 15.5V to 18.5V
V_{IH} = −28V ±2V
Operating Temperature (T_A) = 0°C to +70°C
Fc = 1.28MHz ±0.01%

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Input logic '0' level	V_{IL}	—	—	+0.8	Volts	
Input logic '1' level	V_{IH}	V_{SS} −1	—	—	Volts	
Input load current (SW, 1.28MHz, OE, MW, CI, CH)	I_{IL}	—	—	0.2	mA	$V_{IN} = -V_{DD}$ Note 1
Input sink current (DMI, SSI, LQ, R)	I_{IH}	—	—	0.2	mA	$V_{IN} = +V_{SS}$ Note 2
Input capacitance	C_{IN}	—	—	10	pF	V_{IN} = OV f = 1MHz
Digit Select Outputs				—		
Logic '1' On Current		5	—		mA	$V_{OUT} = (V_{SS} - 2)V$
Logic '0' Off Current		—	—	10	μA	$V_{OUT} = (V_{H} + 1)V$
Segment Outputs						
Logic '1' On Current		2	—	—	mA	$V_{OUT} = (V_{SS} - 2)V$
Logic '0' Off Current		—	—	10	μA	$V_{OUT} = (V_{H} + 1)V$
PR Output						
Logic '0'	V_{OL}	—	—	0.5	Volts	} Load = 2TTL gates (3.2mA), 3.3K
Logic '1'	V_{OH}	V_{SS} −2.2		—	Volts	} to V_{DD}, 20pF
Clock input frequency	f_c	—	1.28	1.4	MHz	Note 3
Clock pulse width		350	—	—	ns	logic '0' or '1'
Count input frequency		10	—	600	kHz	
Count input pulse width		600	—	—	ns	logic '0' or '1'
Multiplex rate		—	50	—	kHz	
Power consumption		—	450	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These inputs have resistors of nominally 170K connected to V_{SS}.
2. These inputs have resistors of nominally 170K connected to V_{DD}.
3. For correct frequency readings the clock input frequency must be 1.28 MHz ± 1 in 10^5.

TIMING DIAGRAM



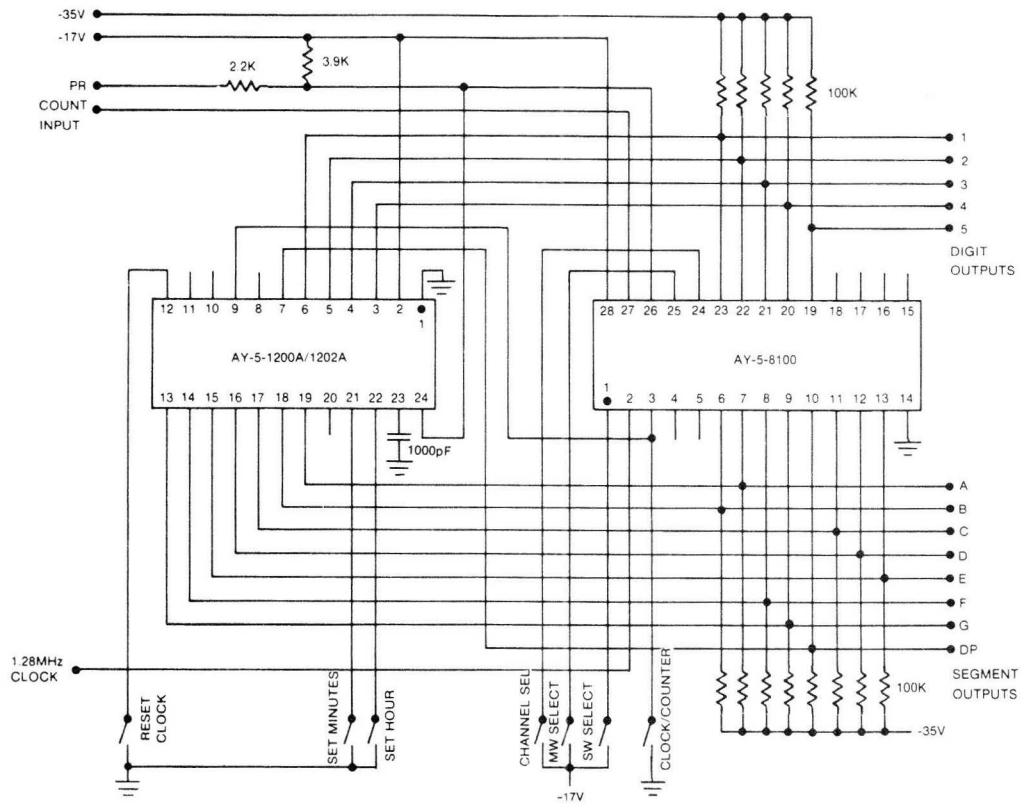


Fig.1 FREQUENCY COUNTER/CLOCK CONNECTION DIAGRAM — DIRECT FLUORESCENT DISPLAY DRIVE.

ENTER-TAINMENT

AY-3-8110
AY-3-8112
AY-3-8114

Radio Receiver Frequency Counter / Display Drivers with 4 Digit Clock

FEATURES

- Low current drain (10 mA)
- Wide supply voltage range (10V to 16V) — clock functions down to 5V
- Intensity control on-chip with external RC
- Display disable
- Mask programmable display frequency 100, 200, 400, 800 or 2000 Hz
- Inter digit blanking — 10μs
- Latched outputs to avoid blanking or flashing during counting.

RADIO FEATURES

- Measures standard AM and FM frequencies
- Displays frequencies on 3½ digit display
- Externally programmable FM IF offset
- 262.5 kHz AM IF offset (AY-3-8110)
- 455kHz AM IF offset (AY-3-8112, AY-3-8114)
- 10kHz steps on AM
- 200kHz steps on FM (AY-3-8110, AY-3-8112)
- 100kHz steps on FM (AY-3-8114)

CLOCK FEATURES

- 12 hour clock (AY-3-8110, AY-3-8112)
- 24 hour clock (AY-3-8114)
- Hour and minute display
- Second reset control
- Easy time set controls
- Time set inhibit input

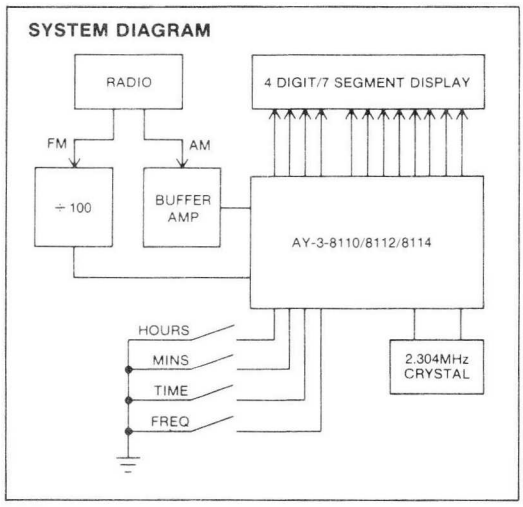
DESCRIPTION

The AY-3-8110/8112/8114 circuits are each an LSI system that contains all the necessary circuitry for displaying time of day or radio tuning frequency on a common 3½ digit display.

The time is derived from an on-chip crystal oscillator and internal countdown circuitry. An internal digit counter and seven segment decoder provides the signals to drive the display. The radio station frequency is determined by measuring the local oscillator of the radio and subtracting the IF frequency.

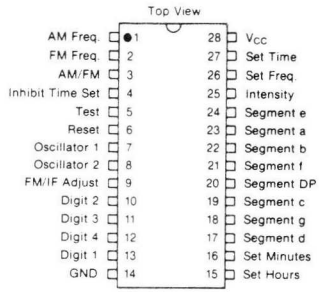
The chip is a monolithic N-channel metal gate MOS device using Ion Implant to achieve both enhancement and depletion devices.

SYSTEM DIAGRAM



PIN CONFIGURATION

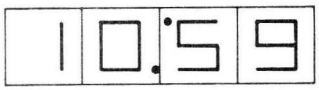
28 LEAD DUAL IN LINE



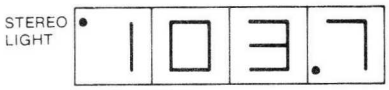
OPERATION

The keyboard consists of two momentary 2-pole switches: Time/Frequency and Set Hours/Set Minutes. The hours or minutes are advanced at 2 per second after a one second delay. A momentary depression of the set minutes resets the seconds without altering the minutes. The display switches from time to frequency and remains there on the momentary depression of the Time/Frequency switch to frequency. The display automatically switches to time when the radio is turned off.

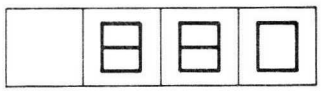
The clock colon is automatically displayed using the decimal points as shown.



When displaying frequency the decimal points are also used to indicate stereo and the radio station. There are no decimal points in the AM mode. Below is the FM display. (The least significant digit is a LH DP. All others are RH DP.)



The AM display is as follows:



OPERATION (Continued)

Four external diodes program the chip to accept 16 different FM IF offset frequencies from .1046 MHz to .1076 MHz in 200 Hz steps. The program code is as follows: (A '1' represents a diode from the digit line to the IF input pin, pin 9.)

The code is shown below:

Frequency	Digit Lines 10 Hour	Hour	10 Min.	Min.
.1076	1	1	1	1
.1074	1	1	1	0
.1072	1	1	0	1
.1070	0	1	1	0
.1068	0	1	0	0
.1066	0	0	1	1
.1064	0	0	1	0
.1062	1	0	1	0
.1060	0	0	0	0
.1058	1	0	0	1
.1056	1	0	0	0
.1054	1	1	0	0
.1052	0	0	0	1
.1050	0	1	0	1
.1048	0	1	1	1
.1046	1	0	1	1

The AM display always ends in zero.

The AM IF offset is 262.5 kHz on the AY-3-8110 and 455 kHz on the AY-3-8112 and AY-3-8114.

The display reads the center of the band even if the radio is tuned up to ±5kHz off center.

DISPLAY OUTPUT INTERFACE

There are twelve output lines to drive the digital display: seven to drive the segments of the display, four for the digit drive, and one for the colon, decimal point and stereo light. The decimal point, colon and stereo light follow the truth table below:

	AM	FM	Time	Digit Time
Colon	OFF	OFF	ON	10 min., hrs.
Decimal Point	OFF	ON	OFF	min.
Stereo Light	OFF	ON	OFF	10 hrs.

DETAILED CRYSTAL SPECIFICATIONS

Frequency	2.30400 MHz ± .003% @ 25°C
Temperature Stability	± 20 parts per million (ppm) over a range of −40°C (−40°F) to 85°C (185°F)
Aging Rate	5 ppm Max.
Shock Resistance	40g in all planes
Vibration	5g from 10 Hz to 55 Hz in all planes
Crystal Resistance	200 Ω Max.
Frequency Trimming Range	± .004% min. with Δ C of 8 pF

PIN FUNCTIONS

Pin No.	Name	Function
1,2	AM Freq., FM Freq.	The local oscillator output frequencies from the radio are connected here.
3	AM/FM	A high on this pin sets the logic to expect an FM frequency in. A low sets the internal logic to AM.
4	Inhibit Time Set	A high level enables the set hours or set minutes switches. Open circuit disables these switches.
5	Test	An 8 Hz signal can be observed here.
6	Reset	A low level resets the chip.
7,8	Oscillator 1, Oscillator 2	The crystal and associated trimmer capacitors are connected here.
9	FM/IF Adjust	The diode programming is input here.
10-13	Digit 2,3,4,1	These pins go to ground to select the appropriate digit.
14	GND	0.0V
15,16	Set Hours, Set Min.	A ground on these pins causes the hours or minutes to update at a 2 per second rate. There is a one second delay before updating starts. If set min. is grounded for more than 0.02 seconds but less than 1 second, the seconds counter is reset. (See Note 1 below).
17-24	Segments a-g & DP	These pins go positive to indicate the desired segment and decimal point.
25	Intensity	An external RC network of 1MΩ and 300pF controls the display intensity.
26,27	Select Freq., Select Time	A momentary ground on one of these pins selects frequency or time to be displayed.
28	V_{CC}	The B+ supply, +10V to +16V (clock functions down to +5V).

NOTE 1: There is a "display disable" feature — grounding pins 15 and 16 simultaneously disables the display (pins 17-24 become three-state).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

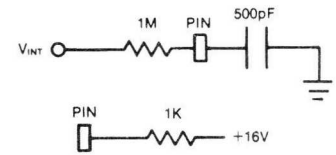
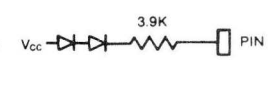
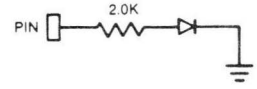
Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +18V
Storage temperature range ..... -55° C to +125° C
Ambient operating temperature range ..... 0° to +60° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

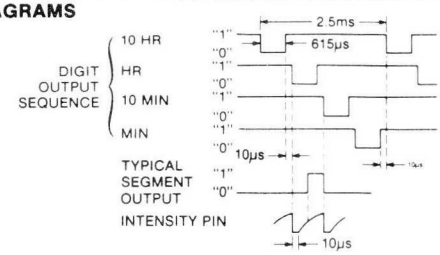
Standard Conditions (unless otherwise noted)

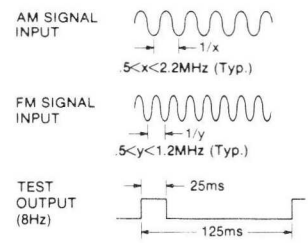
V_{SS} = 0V
V_{CC} = +10V to +16V (clock functions down to V_{CC} = +5V)
Operating Temperature (T_A) = 0° C to +60° C

NOTE 2: Pins 3, 6, 15, 16 and 26 have on-chip pull-up resistors to V_{CC}.
NOTE 3: Pins 4 and 27 have on-chip pull-down resistors to V_{SS}.
**Typical values are at +25° C and nominal voltages.

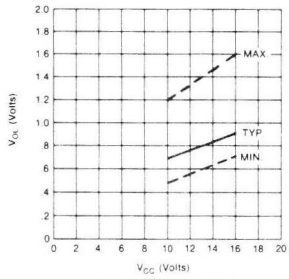
Characteristic	Min	Typ**	Max	Units	Conditions
Clock					
Input Freq.	—	2.304000	—	MHz	
Logic '0'	0.0	—	0.5	Volts	
Logic '1'	3.5	—	V_{CC}	Volts	
Capacitance	—	—	10	pF	
Leakage	—	—	10	μA	
Control Inputs					
Logic '1'	3.5	—	V_{CC}	Volts	
Logic '0'—(Note 2 above)	0.0	—	0.5	Volts	
—(Note 3 above)	0.0	—	0.75	Volts	
Input Current (Note 2—above)	−3	—	−40	μA	Input connected to V_{SS}.
Input Current (Note 3—above)	3	—	40	μA	Input connected to V_{CC}.
AM Freq.; FM Freq Inputs					
Logic '0'—Pin 1 (AM)	0.0	—	0.75	Volts	
—Pin 2 (FM)	0.0	—	0.5	Volts	
Logic '1'	3.5	—	5.5	Volts	
Leakage	—	—	10	μA	
Pulse Width—Pin 1 (AM)	180	—	—	ns	Positive or negative, duty cycle 40-60%.
—Pin 2 (FM)	360	—	—	ns	
Frequency—Pin 1 (AM)	500	—	2200	kHz	
—Pin 2 (FM)	0.5	—	1.2	MHz	
FM IF Input					
Logic '0'	0.0	—	1.8	Volts	
Logic '1'	4.0	—	V_{CC}	Volts	
Intensity Input					
Logic '0'	0.0	—	1.5	Volts	
Logic '1'	4.0	—	—	Volts	
50% Segment Duty Cycle	3.75	—	7.25	Volts	
75% Segment Duty Cycle	6.0	—	13.5	Volts	
Leakage	—	—	10	μA	
Logic '0' (as an output)	—	—	1.2	Volts	
Outputs					
Digit—Pins 10 to 13					
Logic '0'	—	—	1.6	Volts	V_{CC} = 16V 
	—	—	1.2	Volts	V_{CC} = 10V
Logic '1'	14	—	—	Volts	V_{CC} = 16V
	8	—	—	Volts	V_{CC} = 10V
Output Current					
with outputs disabled: to V_{SS}	−0.1	—	−0.4	mA	Pins 15 and 16 = 0V
to V_{CC}	—	—	20	μA	
Segment—Pins 17 to 24					
Logic '0'	—	—	0.5	Volts	V_{CC} = 16V 
	—	—	0.5	Volts	V_{CC} = 10V
Logic '1'	8	—	—	Volts	V_{CC} = 16V
	5.5	—	—	Volts	V_{CC} = 10V
Output Leakage					
with outputs disabled	—	—	±20	μA	Pins 15 and 16 = 0V
Oscillator—Pin 7					
Logic '0'	—	—	0.6	Volts	V_{CC} = 16V, Pin 8 = 0V
Logic '1'	3.6	—	—	Volts	V_{CC} = Pin 8 = 5V
Supply Current	—	—	8	mA	Display outputs disabled, V_{CC} = 16V

TIMING DIAGRAMS

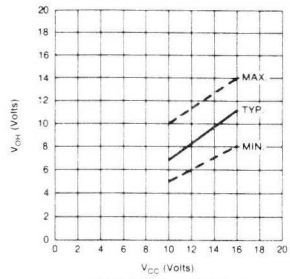




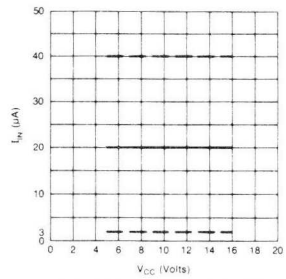
TYPICAL CHARACTERISTIC CURVES



DIGIT OUTPUT VOLTAGE
3.9K to V_{CC}

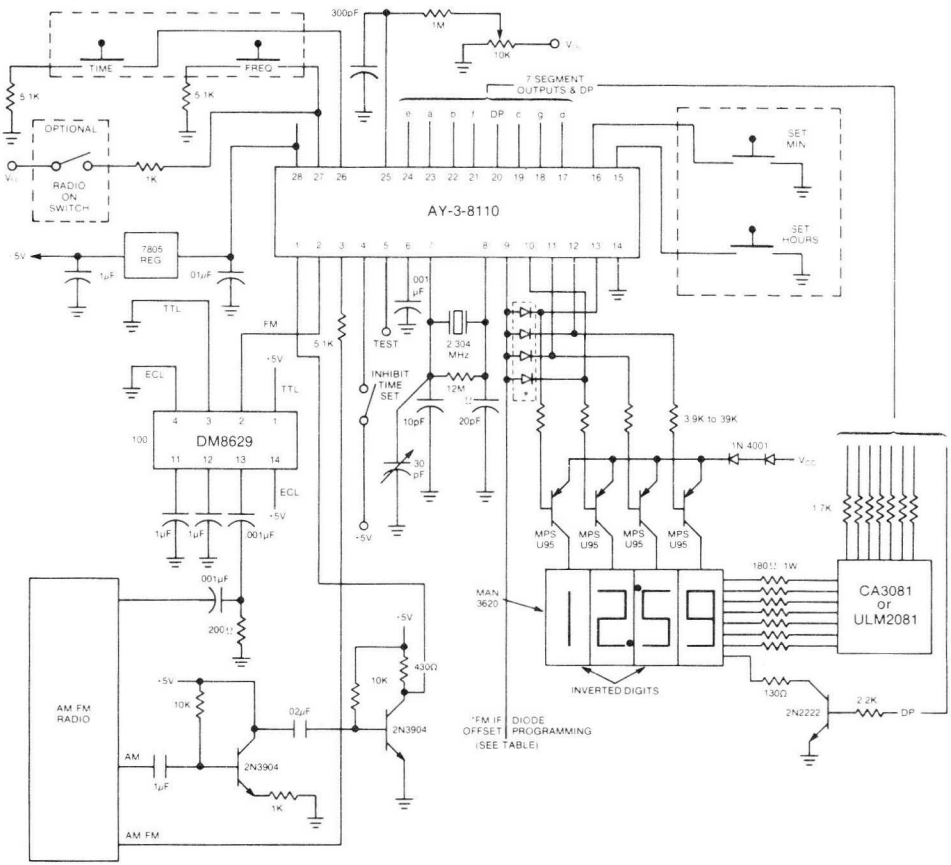


SEGMENT OUTPUT VOLTAGE
2.0K to +0.7V



INPUT CURRENT (PINS 3,9,15,16,26,4,27)

SYSTEM DIAGRAM



ENTER-TAINMENT

STEREOMEGA / Phase-Locked Loop Digital Tuning System

FEATURES

- Full electronic control of a varactor-tuned AM/FM radio.
- Four station selection modes, including Tune Up/Down, Scan, Search Stereo, Select favorite stations.
- EAROM non-volatile memory for storage of "last station tuned" and five favorite stations on each band.
- Display of tuned frequency on a 3½ digit LED display.
- Optional AY-3-8116 clock circuit for time display.
- Optional AY-3-8117 display driver.
- Optional operation with SAA1024/1025 and AY-5-8450/60 circuits for partial or full remote control operation of all functions.

DESCRIPTION

The Stereomega Phase-Locked Loop Digital Tuning System consists of two chips (Controller and Memory) which provide full electronic control of a varactor-tuned AM/FM radio.

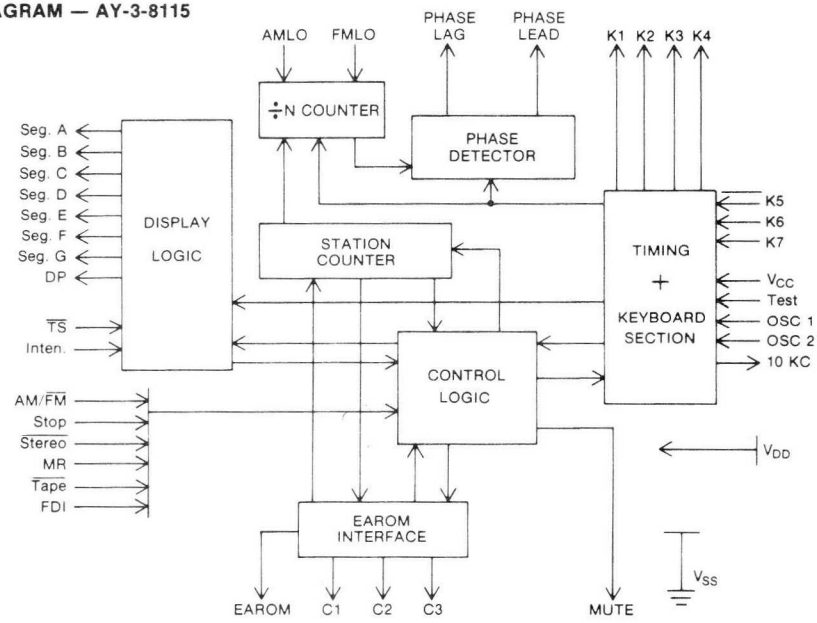
The Controller chip (AY-3-8115) provides phase-locked loop capability with on-chip frequency division, reference oscillator, and comparator circuitry. It directly accepts AM/FM local oscillator inputs, and outputs control signals for closed loop operation of these oscillators. It also provides signals to display on a 3½ digit LED display the center frequency of the tuned station.

The EAROM chip (ER1400) is an electrically alterable read-only memory which features non-volatile, un-powered data retention capability. Five favorite stations on each band can be stored as well as "last station tuned" information.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8115

BLOCK DIAGRAM — AY-3-8115



PIN FUNCTIONS

Pin No.	Symbol	Function
1, 2, 3	C1, C2, C3	These outputs provide the control signals to the EAROM ER1400 for function select. See Table 3 for the function decodes.
4, 5, 6, 7	K1, K2, K3, K4	These outputs supply the horizontal drive for the Keyboard matrix. They are also used as digit drivers for the LED display. See Fig. 1 for the digit identification.
8, 9, 10	K5, K6, K7	These inputs are from a three by four Keyboard matrix. Various functions are entered through the Keyboard. All three inputs are provided with internal pull up resistors. See Table 2 for the Keyboard assignments.
11	V_{DD}	+10 Volts to +13 Volt supply to the chip.
12, 13	PHASE LAG, PHASE LEAD	These two tri-state outputs are used (via a CMOS switch and filters) to supply analog voltages to the tuner varactors for controlling the AM and FM local oscillator frequencies.
14	$\overline{\text{STEREO}}$	This input is used for controlling the search of stereo stations. If the input is pulled low, a stereo station is indicated. This signal is also used internally to control the stereo light. A pull up resistor is provided internally.
15, 16	V_{SS}	System Grounds.
17	STOP	This input is used to control the station searching operation. It is high to indicate the presence of a station. NO internal pull up resistor is provided.
18	AM/$\overline{\text{FM}}$	This input is for band select. It is high for AM and low for FM stations. A pull-up resistor is provided internally.
19	10kHz	This output provides a 10kHz signal to the EAROM ER1400 and to the clock chip. Going to the EAROM, it provides a time base for data and address strobes. Going to the clock chip, it provides a time base for real time down count.
20	V_{CC}	This is a +5 to +13 Volt standby supply input for time keeping. This power line should be connected at all times if the clock option is used. When V_{DD} is on, V_{CC} must be greater than or equal to V_{DD}.
21	TEST	This input is for reset testing.
22, 23	OSC2, OSC1	These inputs are for connection to a 2.6MHz crystal.
24	FMLO	This input is the FM band local oscillator input. The frequency range is from 900kHz to 1200kHz. The frequency is divided down by 100 using an FM prescaler.
25	AMLO	This input is the AM band local oscillator input. The frequency range is from 900kHz to 2100kHz.
26	INTEN	This input is for display intensity control. See Fig. 2.
27-34	SEG A - SEG G & DP	These outputs are the tri-stated segment drivers. An output is high for a segment to be on, and low for off.
35	$\overline{\text{TS}}$	This input is for tri-stating all the segment outputs. When pulled low, the segments are tri-stated. A pull up resistor is provided internally. See Table 1 for display controls.
36	FDI	This input provides an option of interfacing the controller chip with a digital clock chip. The clock chip can allow this input to go high and all segments will then be enabled by the controller (Frequency Display Inhibit). The clock chip can then blank individual segments for real time display. A pull up resistor is provided internally. See Table 1 for display controls.
37	EAROM	This is a tri-stated input and output line used for data and address transfers between the controller chip and the EAROM ER1400.
38	MUTE	This output line is high to mute the radio in the case of station changes, band changes or radiotaped deck conversions. See Fig. 3 for Mute durations.
39	$\overline{\text{TAPE}}$	This input provides an option of interfacing the display circuit with a tape deck for tape track indication. When this input is pulled low, the controller will enable all display lines showing all segments. Individual segments can then be blanked for track indication. All keys and switches are disabled at this time. On the trailing edge of this signal, a status restoration routine is initiated to recall the last station. A pull up resistor is provided internally.
40	MR	Master reset for the chip. On the trailing edge of this signal, a status restoration routine is initiated to recall the last station tuned.

OPERATION

Tune Up: The Tune Up Key is a dual function key.

a) A single momentary depression will cause a single step up band.

b) Continuous depression allows traversing up the entire band at a rate of 240 ms per channel (200kHz). Mute is held high continuously.

The Tune Up function is automatically disabled at the top of the band.

Tune Down: The Tune Down Key is exactly analogous to the Tune Up Key except that the band is traversed downwards.

Search AM/FM Stereo: Continuous depression of either of the Search Keys will result in traversing up the complete band within 4.5 to 5.5 seconds. If the top of the band is reached, the searching operation will flyback to the bottom and continue searching up the band. Upon release of a Search Key, an examine sequence will be initiated.

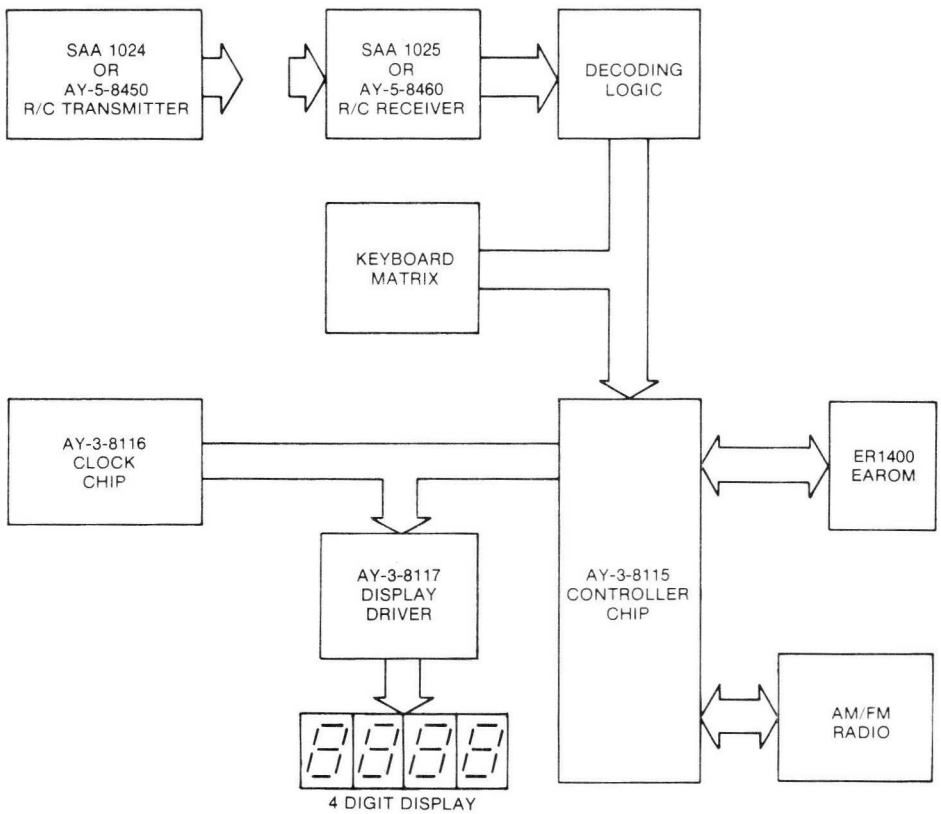
The examine sequence consists of two "look windows" and a wait period in between. See Fig. 5 for a detailed description.

Scan: After the Scan line is activated, the controller will cause the radio to search until a station is acquired and will remain locked to that station for a period of 7.5 to 8.5 seconds to allow the user to monitor the channel. If no action is taken by the user, the controller will automatically reactivate the operation. If the Scan Key is again activated, the Controller will lock up on the selected channel and terminate the Scan operation. If the Scan Key is activated while the controller is actively searching, it will terminate the Scan as soon as it acquires a station. See Table 4 for Scan and Search defeats.

Station 1-5: Five favorite stations can be recalled from the ER1400 for each band.

Program: Tuning information is stored into the EAROM ER1400 by depressing Program and then the desired Station key within 4.5 to 5.5 seconds from the time Program was initially depressed. If any other key other than a Station key is depressed within this time, the Program function is terminated.

SYSTEM DIAGRAM



ELECTRICAL CHARACTERISTICS

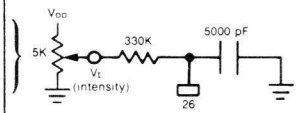
Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −.3 to +20V
Storage temperature range ..... −50°C to 150°C
Ambient operating temperature range ..... −10°C to +60°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5.0 to +13.0 Volts
V_{DD} = +10.0 to +13.0 Volts
V_{SS} = 0 Volts
T_A = −10°C to +60°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
AM Local Oscillator:					
Logic "1"	4.0	—	V_{DD}	V	
Logic "0"	−0.3	—	1.0	V	
Duty factor @ 1.5V Threshold	40	—	60	%	
Frequency	900	—	2100	kHz	
FM Local Oscillator:					
Risetime (0.5V to 3.0V) @ 1.2MHz	—	—	100	ns	
Falltime (3.0V to 0.5V) @ 1.2MHz	—	—	100	ns	
Logic "0"	−0.3	—	1.0	V	
Logic "1"	3.0	—	V_{DD}	V	
Duty factor @ 1.5V Threshold	40	—	60	%	
Frequency	900	—	1200	kHz	
FDI, $\overline{\text{STEREO}}$, $\overline{\text{TS}}$					
Logic "0"	0	—	0.5	V	
Logic "1"	4.0	—	V_{DD}	V	
Internal Pull Up	80	—	1500	kΩ	
K5, K6, K7:					
Logic "0"	0	—	1.5	V	
Logic "1"	4.0	—	V_{DD}	V	
Internal Pull Up	80	—	1500	kΩ	
MR, STOP, $\overline{\text{TAPE}}$, AM/$\overline{\text{FM}}$					
Logic "0"	0	—	0.5	V	
Logic "1"	4.0	—	V_{DD}	V	
Internal Pull Up	80	—	1500	kΩ	No internal pull up on MR or STOP
Intensity:					
% of full intensity duty cycle with control voltage V_I=12V.	40	—	80	%	
Return to full intensity voltage (V_I)	3.5	5.0	6.0	V	
Phase Lag, Phase Lead					
Logic "0"	—	—	1.5	V	
Logic "1"	V_{DD}−1	—	—	V	@ .05mA
MUTE:					
Current source	—	—	0.5	mA	@ (V_{DD}−4.0V)
Current sink	—	—	0.5	mA	@ 0.5V
Seven Segments + DP					V_{DD} = 11.0V
Current sink	—	—	0.5	mA	@ 0.5V
Current source	2.0	—	—	mA	into 2Kohm resistor
K1, K2, K3, K4:					
Current sink	1.0	—	—	mA	@ 0.5 Volts
Current source	—	—	0.1	mA	@ (V_{DD}−1.0V)
10kHz					
Current sink	0.1	—	—	mA	@ 0.5V
Current source	0.1	—	—	mA	@ (V_{DD}−1.5V)
C1, C2, C3:					
Current sink	0.5	—	—	mA	@ 0.5V
Current source	0.1	—	—	mA	@ (V_{DD}−1.5V)
Power Supply Current:					
I_{DD}	—	—	65	mA	
I_{CC}	—	—	6	mA	

ENTER-TAINMENT

Table 1. DISPLAY CONTROL TRUTH TABLE

$\overline{TAPE}$	FDI	$\overline{TS}$	Segment Status
H	L	H	Frequency Display
*	*	L	Tri-stated
L	*	H	All lit
*	H	H	All lit

*Don't Care

Table 3. EAROM ER1400 FUNCTION INPUTS

	C1	C2	C3
Standby	H	H	H
Read	L	H	H
Write	L	L	H
Erase	H	L	H
Shift Data into EAROM	L	L	L
Shift Data out of EAROM	L	H	L
Shift Address into EAROM	H	L	L

Table 2. KEYBOARD KEY ASSIGNMENT

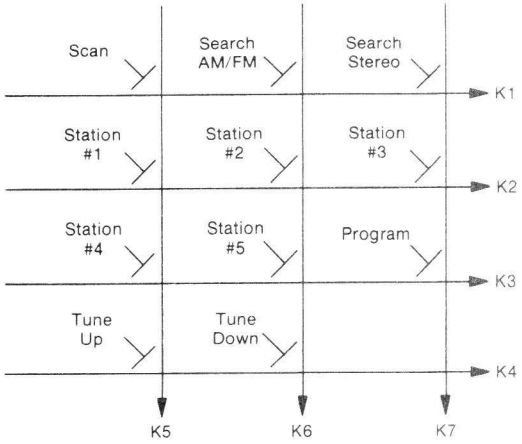


Table 4: SCAN AND SEARCH DEFEATS

	Present Mode	
Push button or Switch Activated	**Search**	**Scan**
Tune up, down; Station; Program; Reset; AM/$\overline{FM}$; $\overline{TAPE}$ (trailing edge)	Terminate	Terminate
Scan	Goes into Scan	Terminate as soon as a station is found
FDI	Stays in Search	1. Terminates as soon as a station is found. 2. Disables 8 second listening window
Search	Goes into appropriate Search Mode	Goes into appropriate Search Mode

Table 5. EAROM ER1400 ADDRESS DECODE

Station On	AM																				FM																
1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
2	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
3	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0
4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
5	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0
Power On	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 6. EAROM ER1400 DATA DECODE

	Frequency	Data in BCD	Data in Binary												
AM	53	53	1	0	0	1	1	0	1	0	1	1	1	1	1
	90	90	1	1	1	1	1	0	1	1	0	1	1	1	1
	161	161	1	0	1	1	1	1	0	0	1	0	1	1	1
FM	88.1	81	1	0	1	1	1	1	1	1	0	1	1	1	1
	103.5	235	1	0	1	0	1	0	0	1	1	1	0	1	1
	107.9	279	1	0	1	1	0	0	0	0	1	1	0	1	1

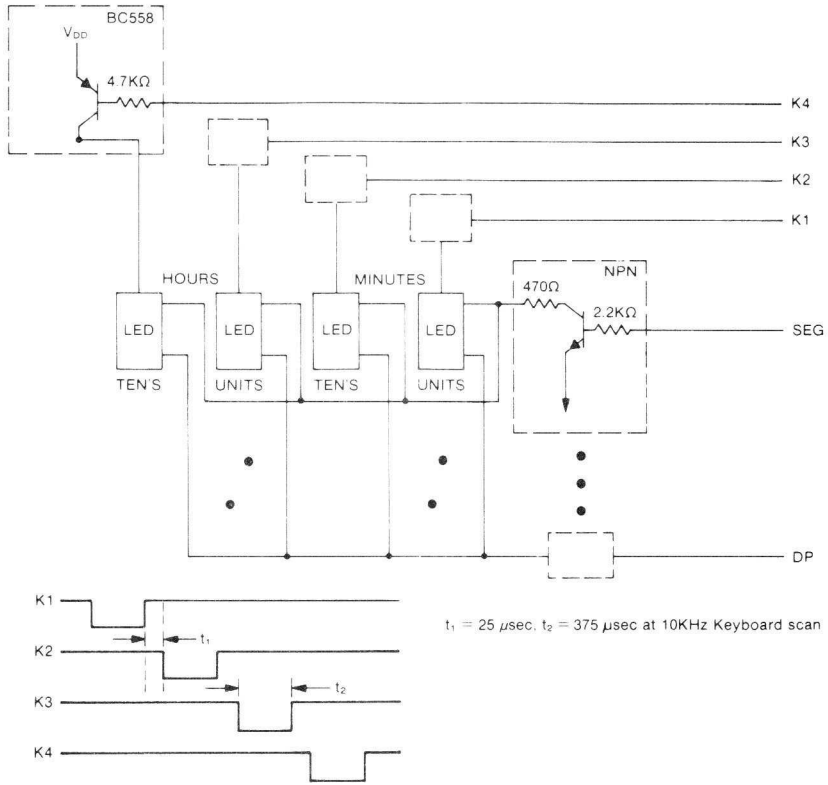


Fig. 1 LED DISPLAY SET UP (without AY-3-8117)

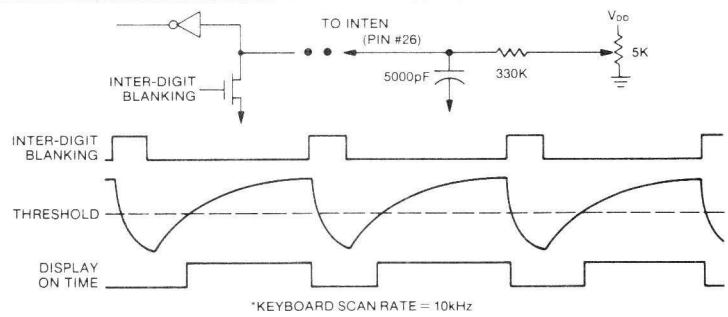
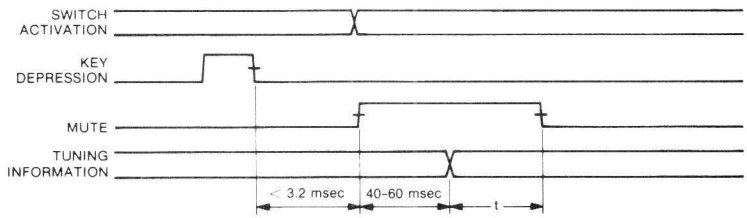


Fig. 2 INTENSITY CIRCUIT



t = 225 to 275 msec for Tune Up, Tune Down, Station, Program.
t = 700 to 800 msec for AM-FM band changes, Master Reset.
t = 225 to 275 msec after a station is acquired for Search Functions and Scan.

Fig. 3 MUTE DURATION

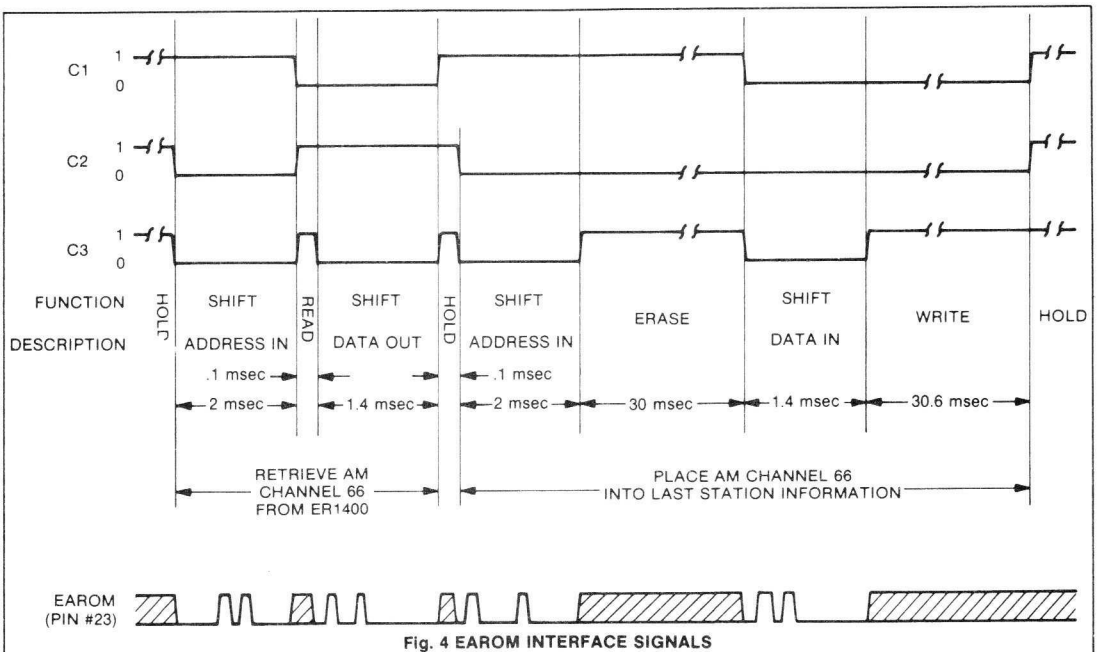
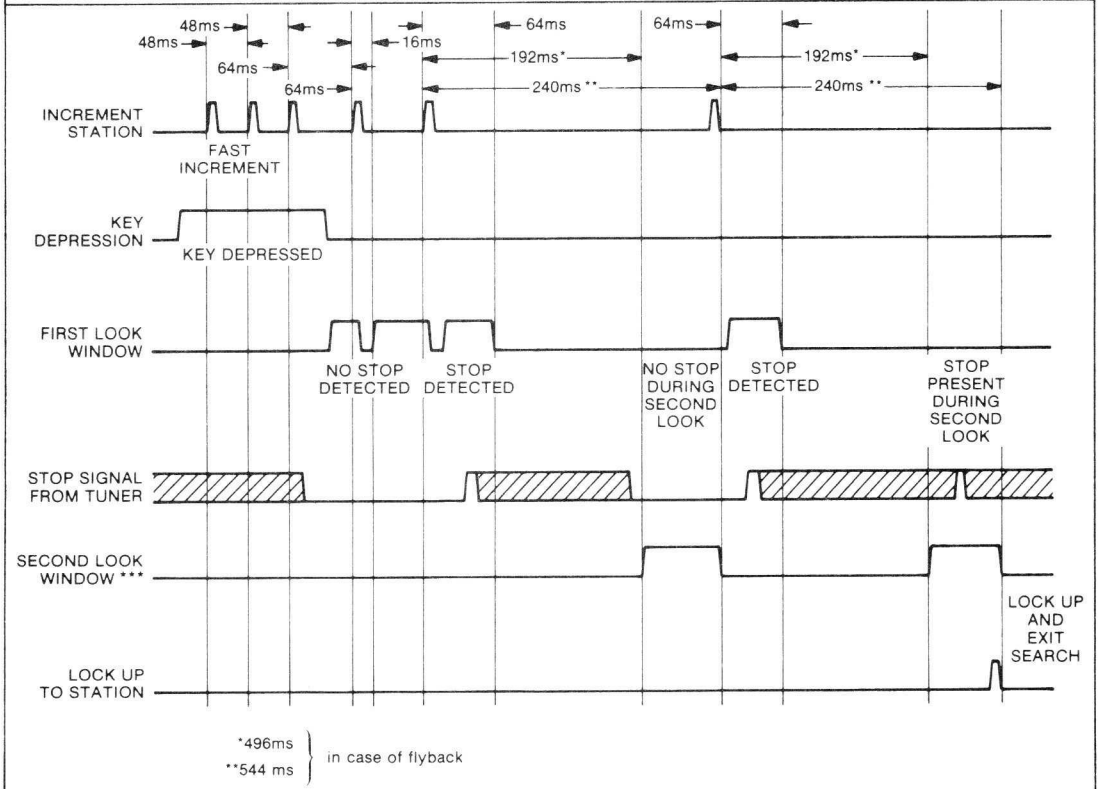


Fig. 4 EAROM INTERFACE SIGNALS



***Second look window included stereo examine in case of Stereo Search operation.

Fig. 5 SEARCH LOGIC TIMING

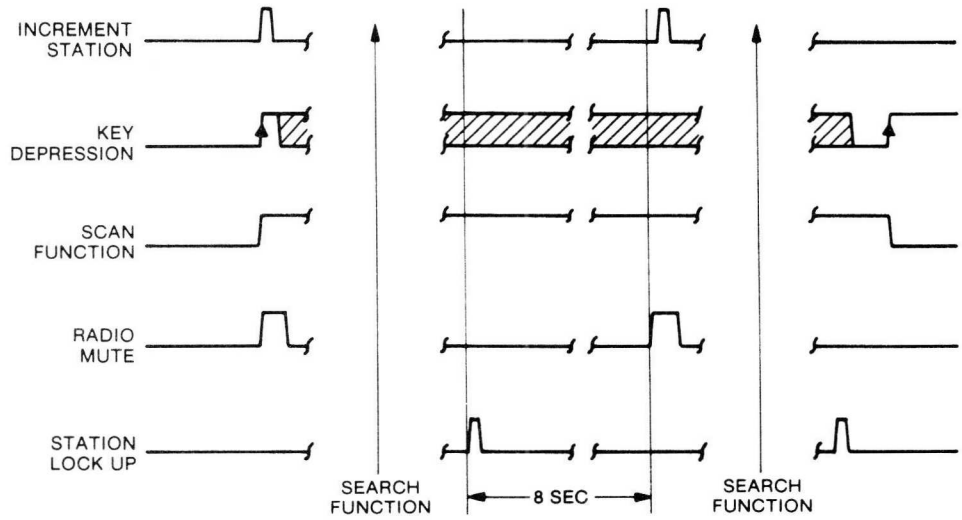


Fig. 6 SCAN FUNCTION TIMING

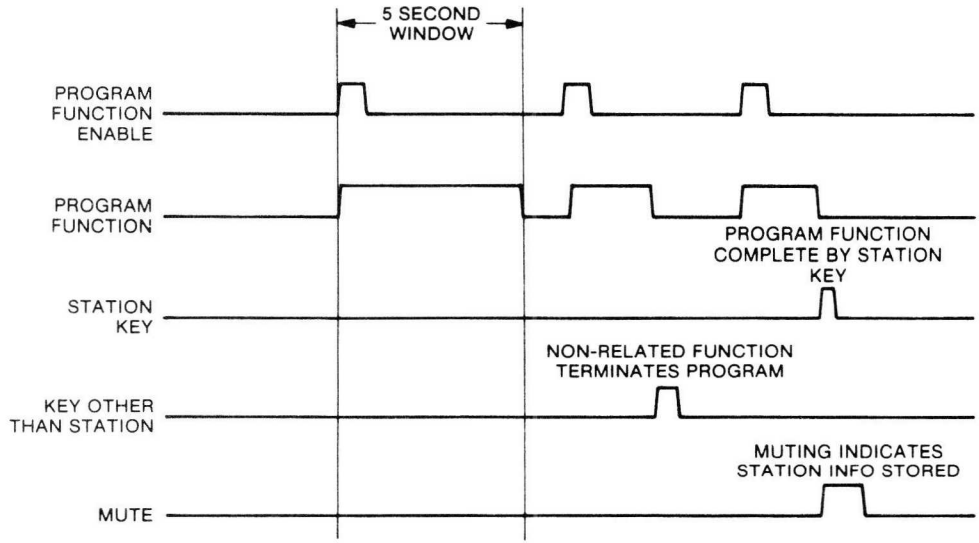


Fig.7 PROGRAM TIMING

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 Word × 14 bit organization
- Word alterable
- 10 years unpowered data storage
- Write/Erase time 20ms/word
- Single −35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

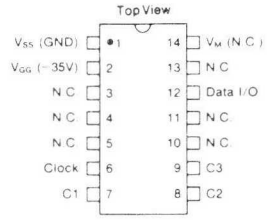
Addressing is by two consecutive one-of-ten codes.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

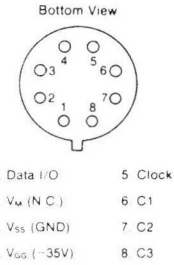
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

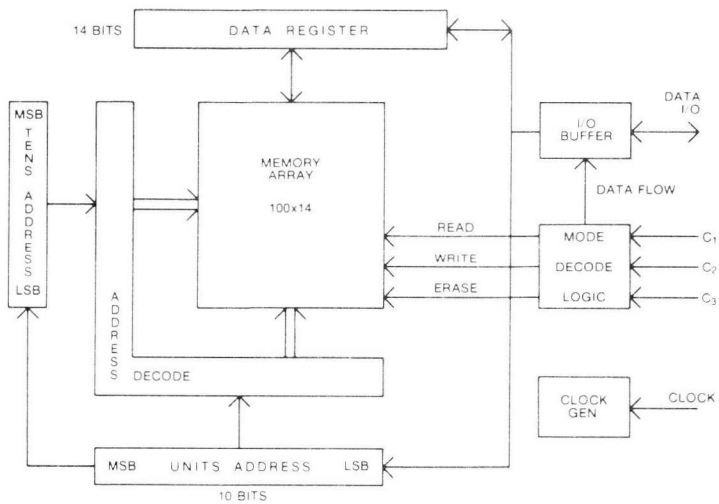
Standard package
14 LEAD DUAL IN LINE



Special Order Package
8 LEAD TO-8 (ER1400T)



BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to −35 volt supply.
Clock	14kHz timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

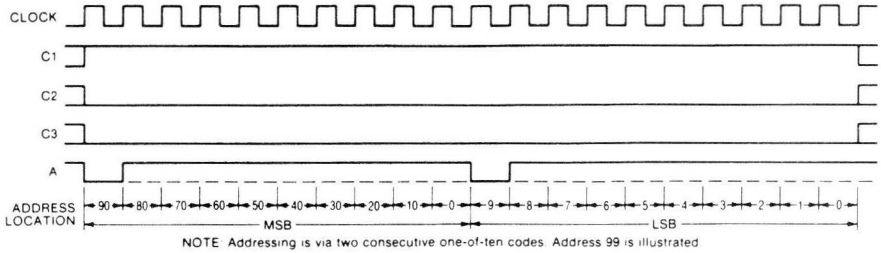
Standard Conditions (unless otherwide noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	VIL	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	VIH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	VOL	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	VOH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply currrent	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	11.2	14.0	16.8	kHz	
Clock duty cycle	Dϕ	45	50	55	%	
Write time	tw	16.0	20.0	24.0	ms	
Erase time	te	16.0	20.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set-up and hold time	t_{CS}, t_{CH}	0	—	—	ns	
Propagation delay	tpw	—	—	20.0	μs	Load = 1 Meg, 100pF
Unpowered non-volatile data storage	T_S	10	—	—	Years	
Number of erase/write cycles	N_W	—	—	10^5	—	Per word
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25°C and nominal voltages.

ENTER-TAINMENT

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

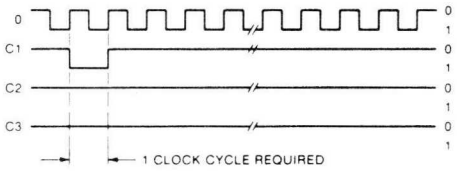
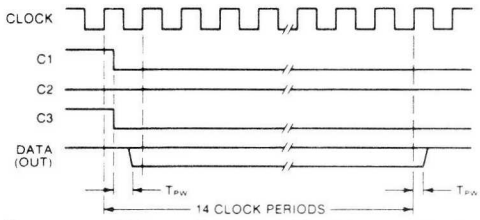


Fig.2 READ



T_{PW} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at V_{SS} -2 and -10 volt points.

Fig.3 SHIFT DATA OUT

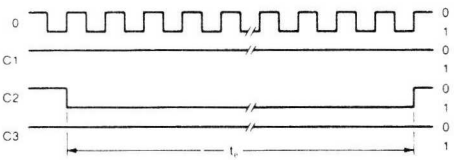


Fig.4 ERASE

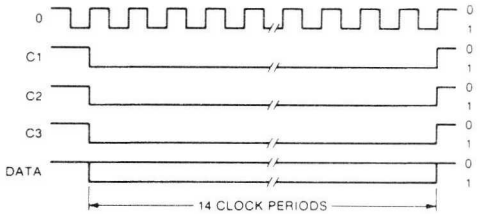


Fig.5 ACCEPT DATA

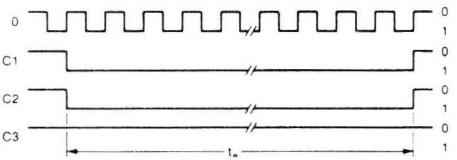


Fig.6 WRITE

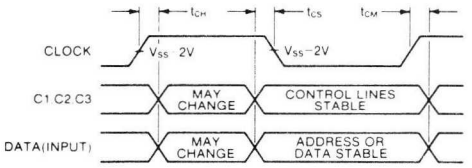


Fig.7 INPUT TIMING

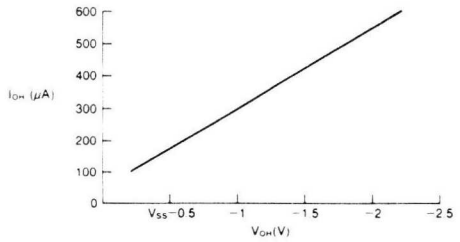


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

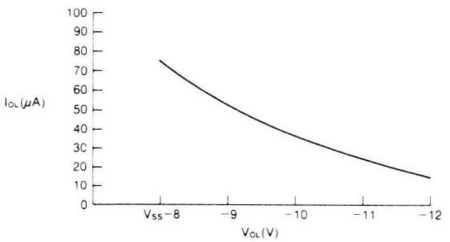


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

Stereomega Clock Circuit

FEATURES:

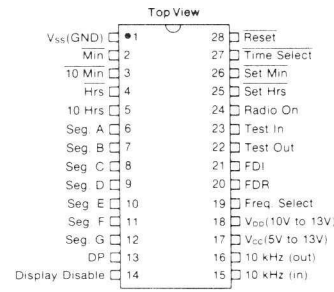
- Basic 3½ digit clock with colon
- Switched V_{DD} to reduce power consumption when time display is not required.

DESCRIPTION

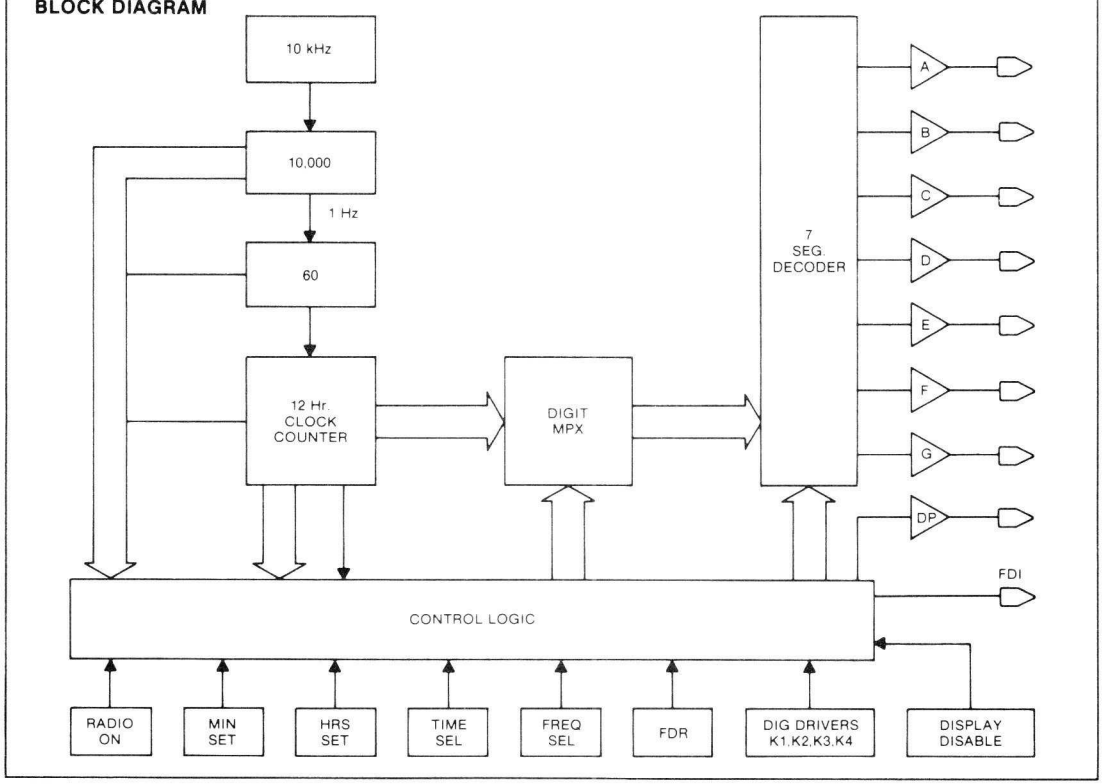
This is the basic clock designed to interface to the AY-3-8115 controller IC. The Reference Frequency, Digit MPX, and Segment Driving Functions are supplied by the controller. The display is 3½ digits and a colon.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

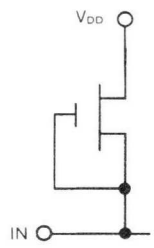
Pin No.	Name	Function
1	V_{SS}	Ground.
2	$\overline{\text{MIN}}$	These lines, generated by the controller, are used by the clock to multiplex the digits.
3	$\overline{\text{10 MIN}}$	
4	$\overline{\text{HRS}}$	
5	$\overline{\text{10 HRS}}$	
6	Seg. A	The seven segment outputs and decimal point are multiplexed to show the time on a 3½ digit display. The decimal point is turned on during the hours time and 10 min. time to display the colon.
7	Seg. B	
8	Seg. C	
9	Seg. D	
10	Seg. E	
11	Seg. F	
12	Seg. G	
13	DP (Decimal Point)	
14	$\overline{\text{Display Disable}}$	While this line is low the eight display lines are off.
15	10 kHz IN	This is the clock reference frequency supplied by the controller, AY-3-8115.
16	10 kHz OUT	This is the buffered reference frequency for the ER1400 EAROM.
17	V_{CC}	5V—13V continuous supply voltage.
18	V_{DD}	10V—13V supply switched off when clock display is not required.
19	$\overline{\text{Frequency Select}}$	A momentary low on this line causes the clock to enter the frequency mode.
20	FDR (Frequency Display Request)	When the clock is in the time mode and the radio is on, a momentary high on this line causes frequency to be displayed for approx. 6-7 seconds (Retriggerable).
21	FDI (Frequency Display Inhibit)	When time is being displayed, this output is high. This is an open drain output which is pulled up when connected to pin 36 of the AY-3-8115 Controller.
22	Test Out	G.I. Test output (Normally Open). A 1Hz signal may be observed on this pin.
23	Test In	G.I. Test input (must be tied to V_{SS} for normal operation).
24	Radio On	When the radio is "on", this input is high. When the radio is "off", this line is pulled low, time is displayed but the mode of the clock remains unchanged.
*25	$\overline{\text{Set HRS}}$	When this line is held low, hours are incremented at the rate of 2 hours per second after a one second delay.
*26	$\overline{\text{Set MIN}}$	When this line is momentarily low, seconds are reset. If it is held low for more than one second, minutes increment at the rate of two minutes per second. The hours carry is inhibited.
*27	$\overline{\text{TIME SELECT}}$	A momentary low on this line causes the clock to enter the time mode.
28	$\overline{\text{RESET}}$	G.I. Test input (must be tied to V_{CC} for normal operation).

*TIME SETTiNG (ref. Fig. 3)
To set the time, the Time Select input (pin 27) should be momentarily pulled low. This initiates a 3 second time-set interval during which the hours or minutes may be set. This interval is re-initiated by the Set Hours or Set Minutes inputs or by another Time Select input.

Table 1: On-Chip Pull-up Resistors

Input Pins	Pull Up Resistors	
	Yes	No
$\overline{\text{Digit Drivers}}$		X
$\overline{\text{Display Disable}}$	X	
$\overline{\text{Freq. Select}}$	X	
$\overline{\text{Set HRS.}}$	X	
$\overline{\text{Set MIN.}}$	X	
Time Select	X	
Radio On		X
Freq. Display Request		X
G.I. Test IN	X	
$\overline{\text{Reset}}$	X	
10 kHz IN		X

Fig.1



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −.3 to +20V
Storage temperature range ..... −55°C to 150°C
Ambient Operating temperature range ..... −10°C to +60°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

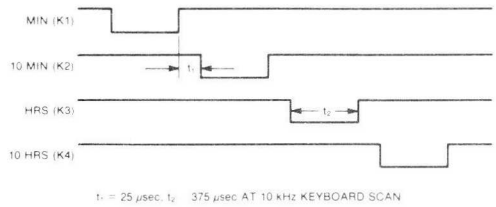
Standard Conditions (Unless otherwise noted)

V_{SS} = 0V
V_{DD} = +10V to +13V
V_{CC} = +5V to +13V
T_A = +25°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
10kHz Reference Frequency Input:					
Frequency	—	10	—	kHz	
Low Level	0	—	1.0	Volts	
High Level	4.0	—	16	Volts	
All Control, Reset, Digit Driver and Test Inputs:					
Low Level	0	—	1.0	Volts	
High Level	4.0	—	16.0	Volts	
Pull up Resistance	0.2	—	2.0	MΩ	See Table 1 and Fig. 1; measured at V_{CC} = V_{DD} = 13V Input = GND
Segment Driver Outputs:					
Low Level	—	—	0.5	Volts	I_{sink} = 7.1mA; Open ended device
High Level	500	—	—	kΩ	Open ended device
Frequency Display Inhibit Output (Open Drain):					
Low Level	0	—	0.5	Volts	@ 0.1 mA } V_{CC} =
Off Leakage	—	—	3.5	μA	@ V_{OH} = 4.0V min. } V_{DD} =13V
10 kHz Buffer Out:					
Low Level	0	—	1.0	Volts	@ 0.1 mA
High Level	V_{CC}−1.0	—	V_{CC}	Volts	@ 0.1 mA
Power Consumption:					
V_{DD} Supply	—	—	300	mW	@ V_{DD} = 13V
V_{CC} Supply	—	—	30	mW	@ V_{CC} = 13V

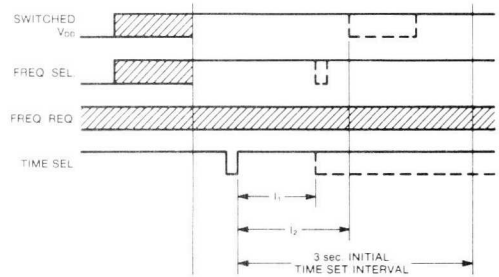
ENTER-TAINMENT

TIMING DIAGRAMS



t_1 = 25 μsec, t_2 = 375 μsec AT 10 kHz KEYBOARD SCAN

Fig.2 DIGIT DRIVER TIMING



t_1 & t_2 are time set intervals that have been shortened by Freq. Sel. and Switched V_{DD} respectively.

NOTE: When the time set interval is active it can be retriggered by another time sel (low) or either set min or set hrs.

Fig.3 TIME SETTING

PRELIMINARY INFORMATION

Stereomega Display Driver

FEATURES

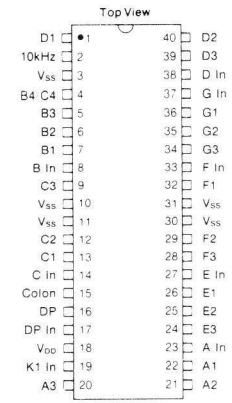
- Eliminates RFI found in multiplexed LED displays.
- Fully compatible with Stereomega Controller circuit (AY-3-8115) and Clock circuit (AY-3-8116).
- Sinks 10mA per segment.
- Displays decimal point for FM and colon for clock.

DESCRIPTION

The AY-3-8117 is a 3½ digit LED display driver which accepts time-multiplexed display data, stores it in latches, and directly drives the segment lines of a 3½ digit LED display. The inputs accept 7-segment information—compatible with the display outputs of the Stereomega Controller circuit, AY-3-8115.

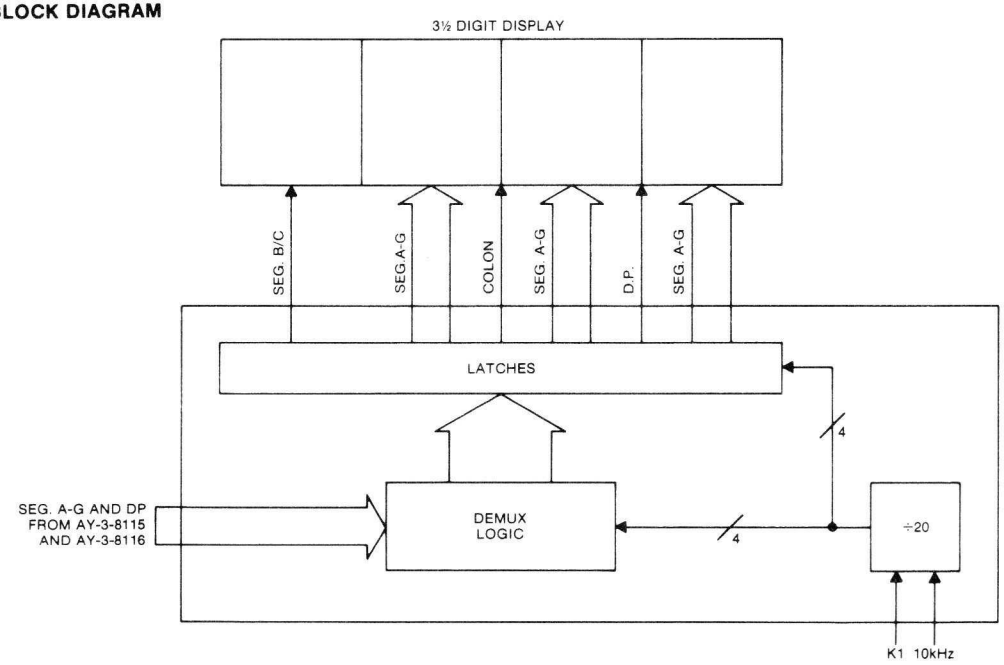
PIN CONFIGURATION

40 LEAD DUAL IN LINE



NOTE: There are five V_{SS} pins—these should all be tied to the same voltage level.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −.3 to +20V
Storage temperature range ..... −55°C to 150°C
Ambient Operating temperature range ..... −10°C to +60°C
Power dissipation 800mW

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (Unless otherwise noted)

V_{SS} = 0V
V_{DD} = +10V to +13V
T_A = +25°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs:					
Logic '0'	V_{SS}	–	1.0	V	
Logic '1'	4.0	–	V_{DD}	V	
Outputs:					
Segment Sinking Current					
Outputs B4/C4 and Colon	20	–	30	mA	
All other outputs	10	–	15	mA	
Segment Leakage	–	–	10	μA	
Segment Voltage	–	–	1.2	V	@ 10mA sinking current
Power Supply Current	–	–	10	mA	Outputs open

ENTER-TAINMENT

MICRO ELECTRONICS

TELEVISION

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
OMEGA 82 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 82-channel television from a two-digit calculator-like keyboard entry.	T-1002	6-30
		T-1102	6-30
		ER1400	6-34
		MEM 4956	6-37
		T-1201	6-30
ECONOMEGA 16 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 8, 12 or 16 channel television, featuring automatic or manual tuning.	AY-3-8203	6-40
		ER1400	6-34
		MEM 4956	6-37
ON-SCREEN CHANNEL/TIME DISPLAY	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display (ref. AY-5-1203A clock circuit)	AY-5-8300	6-46
		AY-5-8301	6-46
		AY-5-8310	6-46
		AY-5-8311	6-46
		AY-5-8320	6-46
		AY-5-8321	6-46
		AY-5-8322	6-46
		AY-5-8324	6-46
ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor-tuned TV sets.	AY-3-8330A	6-57
		AY-3-8331	6-57
		AY-3-8335	6-57

OMEGA / 82 Channel Digital Tuning System

SYSTEM DESCRIPTION

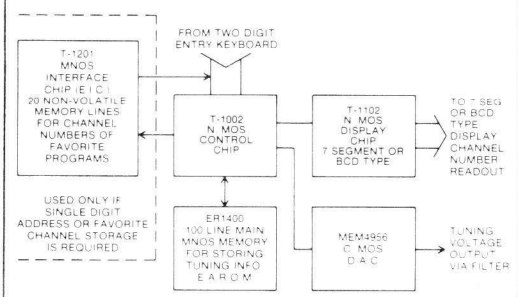
The Omega System combines an electronic solid state channel selector with a VHF/UHF varactor tuner pair. The system accepts a calculator-like 2 digit keyboard entry and provides the selected channel number on a two digit seven element display. Controls are also provided for fine-tune, coarse-tune, search, digital step tuning up and down. Single digit entry for favorite television channels is available as a design option.

The digital counterparts of the analog channel voltages corresponding to the frequencies tuned are stored in a non-volatile Electronically Alterable Read Only Memory (EAROM) which retains, without standby power, the desired coarse- and fine-tune data for all channels. The system has been designed to be extremely insensitive to supply voltage variations, component aging and environmental changes. The tuning accuracy depends only on a single well regulated reference voltage for its stability.

The method of D/A conversion used is a pulse width modulator driving a low-pass filter. The DC component out of the filter is applied to the varactor tuner. A complementary MOS device is used between the control chip and the low-pass filter to achieve the precise and stable amplitudes required at the input to the filter.

The EAROM is a 1400 bit solid state memory organized into one hundred words of 14-bits each. This technology provides a non-volatile memory for 98 channels of tuning information. Two words or lines in the EAROM are reserved to remember the two digit channel number for the last program selected by the viewer. When the set is turned on again after being off indefinitely, it automatically selects the last channel selected before shut down. Each word can be erased and rewritten without affecting the 99 other words and is updated any time the viewer adjusts the tuning of his set. Adequate space in the memory is provided for the 12 VHF and 70 UHF channels, plus 16 locations reserved for other services.

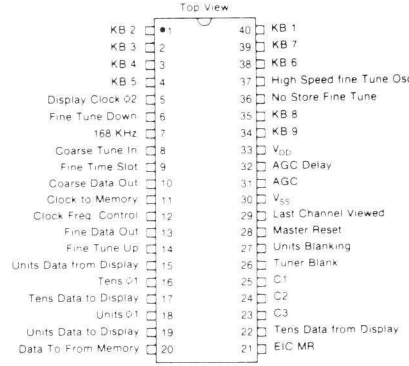
BLOCK DIAGRAM



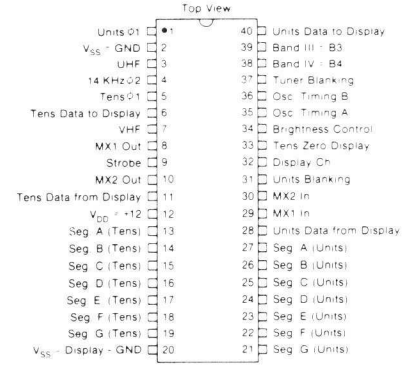
PIN CONFIGURATIONS

40 LEAD DUAL IN LINE

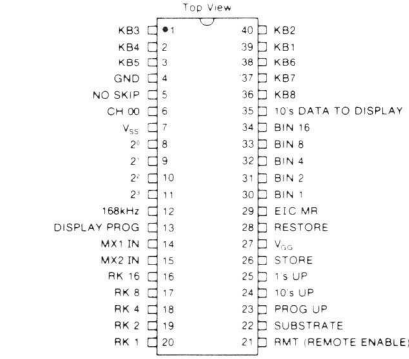
T-1002



T-1102



T-1201



Control Chip (T-1002)

The control chip scans the keyboard at a 14 KHz rate on constant alert for a switch closure. A closure may command one of the following functions:

(a) Two digit random channel selection
(b) Channel stepping (units or tens digits)
(c) Coarse-tune
(d) Fine-tune
(e) Search

The control chip also is designed to accommodate a signal input from a remote control receiver and a "power-up" signal from a power supply to trigger the last-channel-viewed function.

Display Chip (T-1102)

Each digit of the channel number entry is converted into a one-out-of-ten code and serially sent to the display chip where it is stored and decoded both for a seven segment or character generator display and for band switching.

EAROM Chip (ER1400)

This channel number is also used as a two digit address (00 thru 97) for the EAROM memory to locate the corresponding memory line. This twenty bit address is sent serially to the EAROM on a single wire bi-directional data bus.

The EAROM memory is designed to accept a two digit 20-bit address. This format was selected to provide ease of keyboard encoding, ease of display encoding, EAROM address decoding, and ease of address incrementation (one bit shift).

The slow speed and simple timing requirements of the memory permit address and data to flow both to and from memory on a single wire. A further economy of interconnects is achieved by using a three bit parallel code to command the memory into one of its seven modes of operation including: Input Address, Input Data, Erase, Write, Read, Data Out and Stand By.

For a complete description of the operation and specifications of the ER1400, refer to the separate data sheet in this section.

D/A Converter Chip (MEM4956)

The CMOS D-to-A converter chip provides interface between the control chip outputs and the filter. In order to achieve optimum trade-off in the D/A system between clock frequency, ripple content of the filter output, and filter settling time, the 14-bit conversion is done in two parts. The 10 most significant bits generate a variable duty factor waveform with 1000 resolution elements of fixed amplitude.

The four least significant bits are used to generate a narrow pulse (equal in width to one coarse resolution element) but variable in amplitude to 15 discrete levels. The variable width and variable amplitude components are multiplexed together in the CMOS chip and drive the input to the low-pass filter. The filter integrates the area under both component waveforms and delivers a dc voltage to the varactor tuner. The ripple is kept below 100 μV and the settling time is about 50 ms. This is accomplished with a maximum clock rate of 1 MHz and with a resolution of 1 part in 15,000 of the reference supply voltage.

For a complete description of the operation and specifications of the MEM4956, refer to the separate data sheet in this section.

Interface Chip (T-1201)

Where single digit entry is required for up to 20 favorite channels a fifth Chip (Interface Chip) is added to the system. This Interface Chip is a PMNOS device incorporating a 20 line non-volatile memory (EAROM) of 12 bits per line together with all logic functions to address the 20 line memory as well as to interface directly with the rest of the Omega system via the control chip keyboard input lines.

Each memory line in this chip is capable of storing a two digit channel number ("zero" before a single digit channel number) which is entered via a tens and ones input that can be sequenced through 0 to 9 with wrap around, but without carry over and can be stored by pressing a store button.

The channel number output from the display chip always shows the correct channel number that is stored in the data registers of the interface chip whenever any function on it is selected.

The tuning voltage output from the DAC also corresponds to the data stored in the main 100 line memory for that channel number. The Interface Chip uses a binary input keyboard to provide single digit access to each of up to twenty memory lines via a diode matrix or to directly interface with binary coded, remote systems for a single digit address.

Provision has been made for sequencing through all 20 memory lines for simplified remote control, with the capability of introducing a skip code (0,0) to bypass any memory line. Memory line or single digit button number outputs are also available in both binary and BCD format.

SYSTEM OPERATION

A. Two digit entry (4 chip OMEGA system)

To select a channel the viewer depresses two digits ("zero" before a single digit channel number) on a keyboard connected to the keyboard entry pins on the control chip. A one of six subroutine counter in the control chip is used to continuously scan the keyboard for a closure which then stops the scanner. A debounce device is used to confirm the closure after a debounce period of approximately 15 msecs. Confirmation of key closure converts the subroutine counter into a shift register which passes the data contained in it to a register in the display chip. The process is repeated when the second digit is entered. When both digits of a valid entry are received by the data registers in the display chip the following sequence occurs.

a) The control chip addresses word/line 99 in the 100 line main memory (EAROM) via the EAROM address register.

b) One digit of the channel number stored in the display chip registers is shifted via the control chip to the data register of the EAROM and upon receiving a "write" signal from the control chip the data is shifted into the EAROM memory line accessed by the address register (in this case line 99). This is repeated for writing the second channel number digit into line 98 and the combination represents the storing of the last channel viewed information used during power up of the system.

c) After storing the last channel viewed information the channel number stored in the display chip register is sent via the control chip to the address register of the EAROM so that the memory line corresponding to this channel number can be read on command from the control chip.

d) The read-from-memory command causes the data in the 14 bit memory line accessed to be read into the Data register of the EAROM and from there out to a 14 bit register in the control chip which also doubles as two polynomial counters of 10 and 4 bits.

e) After receiving the information from the data register of the EAROM, the 14 bit register in the control chip becomes a ten bit and a four bit polynomial counter. The 10 bit polynomial counter is used to produce, via a set/reset flip flop, a variable duty cycle square wave (amplitude is V_{DD} to V_{SS}) which is used to generate, via the CMOS DAC, the coarse tuning voltage corresponding to the code in the line of the EAROM that was accessed.

f) The four bit polynomial counter acts similarly to the 10 bit counter, but in a different time frame. It gives a variable duty cycle square wave at a frequency of approximately 67 KHz.

g) The coarse and fine tune data is fed from the control chip to the DAC where it is amplified to the level of V_{REF} (tuning voltage reference). The fine tune information is also filtered to a DC level and then inserted at the end of each coarse tune pulse. It is this combined output of the DAC that is filtered by a 5 pole filter network to produce the tuning voltage V_T for the varactor tuners. The output impedance of the filter is approximately 47 K ohm and its rise time is about 50 msecs.

Operation of the fine tuning controls (UP or DOWN) on the control chip alters the 4 bit polynomial counter which has carry over to the 10 bit polynomial counter. Therefore use of these controls allows the user to scan through the total tuning voltage range at a speed that is determined by the time constant of the network connected to pin 37 of the control chip. Alteration of the time constant is used to provide coarse tune speed for set up, as well as equalization of the tuning rate (MHz/sec) between VHF and UHF.

The action of the store-fine-tuning command, which may be made manually, or automatically on release of the fine tune button, cause the two polynomial counters to chain together into a 14 bit shift register which then shifts its contents into the data register of the EAROM which is then written into the memory line of the EAROM corresponding to the channel number that is in its address register.

The new tuning data is still retained in the control chip register which returns to its polynomial counter mode and continues operating as previously described.

On power-up, a master reset pulse is generated in the control chip to reset all clocks. The control chip then also addresses lines 99 and then line 98 of the EAROM in sequence causing the information stored in those lines (last channel number viewed) to be put into the display chip register (if last channel viewed option is used) which then starts up the sequence described previously just as if this data came from the control chip keyboard. Read and write times of the EAROM lines are approximately 20 msecs. All times are referenced to the internally generated 1 MHz clock in the control chip.

Channel number information in the display chip register is used to automatically decode the band information which is fed out as logic signals by the 4 band outputs of the display chip. The channel number information is also available (depending on display chip used) in a form suitable for common anode type seven segment displays (units and tens digit information are separate) or for character generator type display in BCD format. Timing waveform outputs and inputs are provided on the display chip for decoding channel number information where appropriate.

B. One digit entry (5 chip option)

The use of the Interface chip for single digit entry for up to 20 favorite channels does not basically modify the operation of the system as described above. This chip interfaces with the keyboard lines on the control chip and the operational sequence is identical to that of a two digit entry from the keyboard except that the two digit information comes from the Interface chip register which is fed the two digit channel number information stored in one of its twenty memory lines (non volatile), which can be accessed by single digit entry as described above.

When the Interface chip is used there is an option available as an alternative to the obtaining the last channel viewed on power-up. This alternative option always returns the system to memory line "one" on the Interface chip on power-up.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +.3V
Storage Temperature Range ..... -30°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

T-1002 Standards Conditions (unless otherwise stated)

V_{SS} = Ground
V_{DD} = +12V
T_A = 0°C to +70°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply Voltage, V_{DD}	10.8	12	13.2	V	
Supply Current, I_{DD}		15	35	mA	V_{DD} × 12.0 VDC
Master Clock, f_m	0.7	0.8	0.9	MHz	R = 100K ± 5% to V_{DD}
Fine Tune Clock, f_r	9.7	11.2	12.5	kHz	C = 68, 75, or 82pF ± 10% to V_{SS}
Inputs:					
Logic "1"	V_{SS} +8	—	V_{DD}	V	
Logic "0"	V_{SS}	—	V_{SS} +.5	V	
Outputs:					
Logic "1"	V_{DD} -2	—	V_{DD}	V	
Logic "0"	V_{SS}	—	V_{SS} +.5	V	
Rise & Fall TIme t_r, t_f			1	µs	

T-1102 Standard Conditions

V_{SS} = Ground
V_{DD} = +12V
T_A = 0°C to +70°C

Characteristic	Units	Min.	Max.	Conditions
V_{DD}	V	10.8	13.2	
I_{DD}	mA		10	With clock running
V_L	V	V_{SS}	V_{DD}	
Quiescent Current	mA		10	Clock Frequency = 0Hz
V_{LN} (Logic Low Signal In)	V	0.0	1.0	At all inputs unless otherwise specified.
V_{HN} (Logic High Signal In)	V	8.0	V_{DD}	At all inputs unless otherwise specified.
V_{LO} (Logic Low Signal Out)	V	0.0 0.0	1.0V 0.5V	For Pins 8, 9, & 10 into 1 MΩ, 20pF load
V_{HO} (Logic High Signal Out)	V	V_{DD} -2 V_{DD} -3	V_{DD} V_{DD}	For Pins 11, & 28 into 1 MΩ, 20pF load For Pins 8, 9, & 10 into 1 MΩ, 20pF load
Ø1 (Units & Tens Clock)	kHz	9.2	16.8	Pins 1, 4, 5
T_R, T_F	ns		550	Pins 1, 4, 5
Ø2	kHz	9.2	16.8	Pin 4.
Duty Cycle Ø1 (Typical)	1/12 of clock Frequency			Pins 1, 5.
Duty Cycle Ø2 (Typical)	1/6 of clock Frequency			Pin 4.
T_{DELAY}	µs	.45	.55	Delay between rise of Ø1 and Ø2 = 1/F
T_R, T_F	µs		1	Pins 8 thru 11 and 28 Load = 10pF
R_{OUT}	kΩ		24	I_L = 1 mA Pins 3,7,38,39
V_O	V	2.0V	Variations Between These Outputs on any 1 chip to be 1V Max.	At I_O Min. = 17 mA. Additionally each output shall be capable of sustaining I_O max 25 mA pins 13, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 27. For LED display only. In the off condition leakage current at +20V to be no greater than 10 µA.
I_O	mA	1.6		For indirect display drive — 13, 14, 15, 16, 24 thru 27. Outputs to be compatible to TTL or CMOS without interface. V_O = 0.6V.

ENTER-TAINMENT

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 Word × 14 bit organization
- Word alterable
- 10 years unpowered data storage
- Write/Erase time 20ms/word
- Single −35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

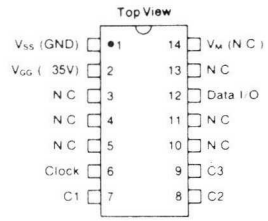
Addressing is by two consecutive one-of-ten codes.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

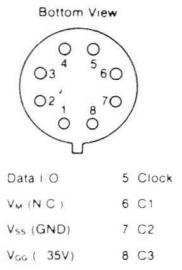
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

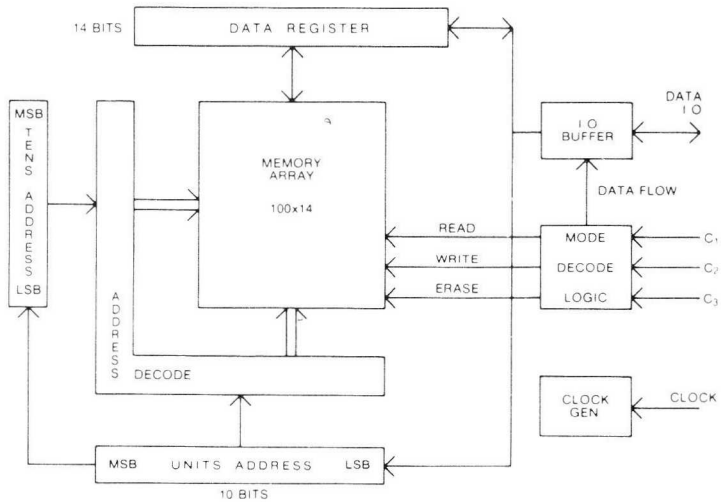
Standard package
14 LEAD DUAL IN LINE



Special Order Package
8 LEAD TO-8 (ER1400T)



BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to −35 volt supply.
Clock	14kHz timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

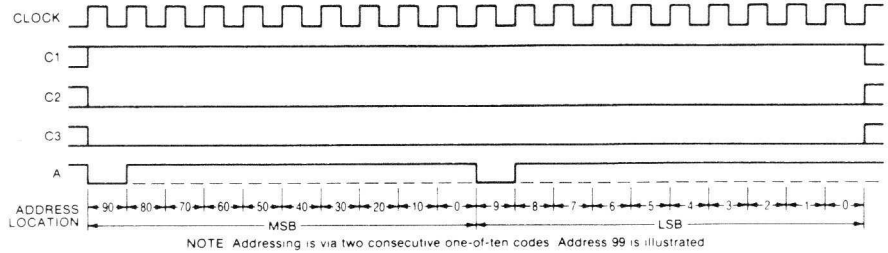
Standard Conditions (unless otherwide noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	VIL	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	VIH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	VOL	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	VOH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply currrent	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	11.2	14.0	16.8	kHz	
Clock duty cycle	Dϕ	45	50	55	%	
Write time	tw	16.0	20.0	24.0	ms	
Erase time	te	16.0	20.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set-up and hold time	t_{CS}, t_{CH}	0	—	—	ns	
Propagation delay	tpw	—	—	20.0	μs	Load = 1 Meg, 100pF
Unpowered non-volatile data storage	T_S	10	—	—	Years	
Number of erase/write cycles	N_W	—	—	10^5	—	Per word
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25°C and nominal voltages.

ENTER-TAINMENT

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

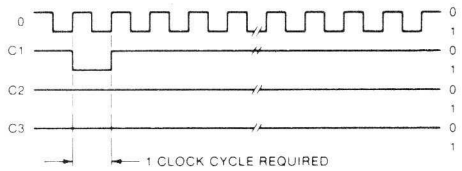
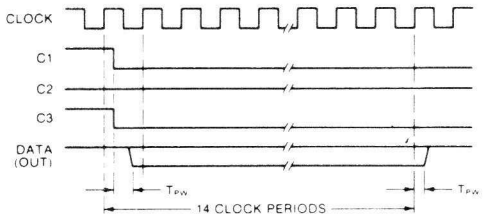


Fig.2 READ



T_{PA} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at V_{SS} -2 and -10 volt points.

Fig.3 SHIFT DATA OUT

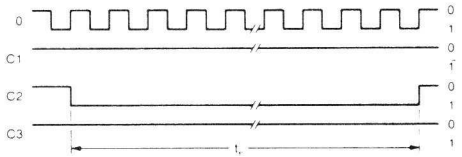


Fig.4 ERASE

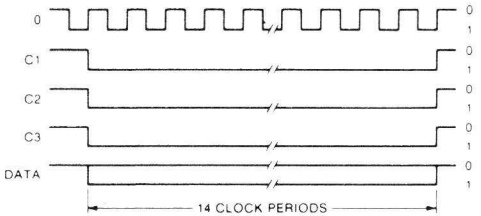


Fig.5 ACCEPT DATA

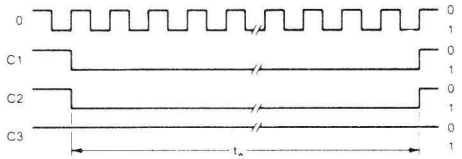


Fig.6 WRITE

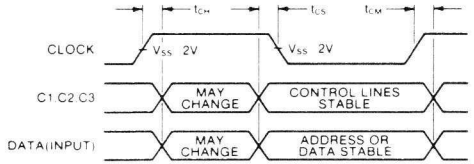


Fig.7 INPUT TIMING

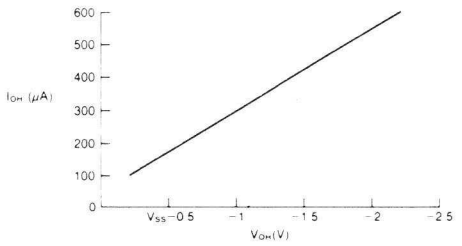


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

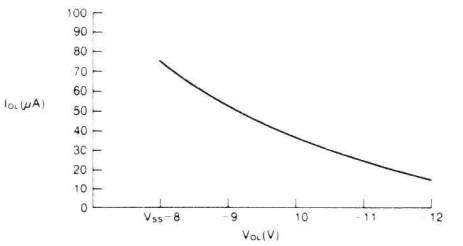


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

CMOS D/A Converter

FEATURES

- Combined and/or separate Coarse and Fine Tuning
- 30V Tuning Voltage Range
- High Stability
- Low Power Consumption

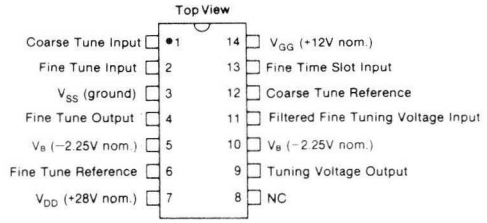
DESCRIPTION

The MEM 4956 is a CMOS D/A Converter designed to operate in conjunction with the GI Omega and Economega Digital Tuning Systems.

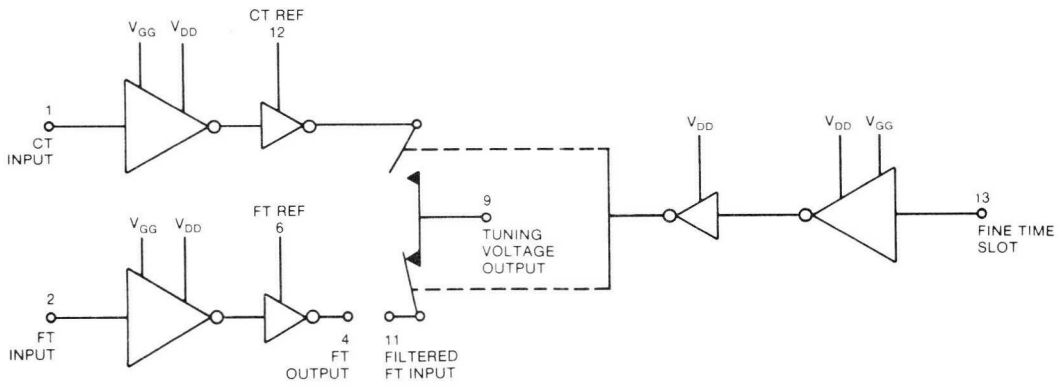
It consists of two level shifting amplifier-drivers with a common output. A control input determines which amplifier is connected to the output.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1.	Coarse Tune Input	Positive going pulse. The duty cycle determines the Tuning Voltage Output.
2.	Fine Tune Input	Positive going pulse. The duty cycle determines the Fine Tuning Voltage Output.
3.	V_{SS}	Negative power supply.
4.	Fine Tune Output	Amplified version of Fine Tune Input. Switches between Vss and Fine Tune Reference.
5.	V_B	−2.25 Bias used to increase breakdown voltage.
6.	Fine Tune Reference	Power supply to Fine Tune Buffer Amplifier: 28V nom.
7.	V_{DD}	Power supply for Logic: 28V nom. (V_{DD} must be the most positive power supply).
9.	Tuning Voltage Output	Combined Coarse and Fine tuning data which after filtering is used to tune the TV.
10.	V_B	−2.25 Bias used to increase breakdown voltage.
11.	Filtered Fine Tuning Voltage Input	The Filtered Fine Tuning Voltage connected to this input is combined with the Coarse Tuning Data by the action of the Fine Time Slot input.
12.	Coarse Tune Reference	Power supply to Coarse Tune Buffer Amplifier: 28V nom.
13.	Fine Time Slot Input	When at logic '0' the Coarse Tuning information is connected to the Tuning Voltage Output. When at logic '1' the Fine Tuning information is connected.
14.	V_{GG}	+12V reference for input level shifting circuit.

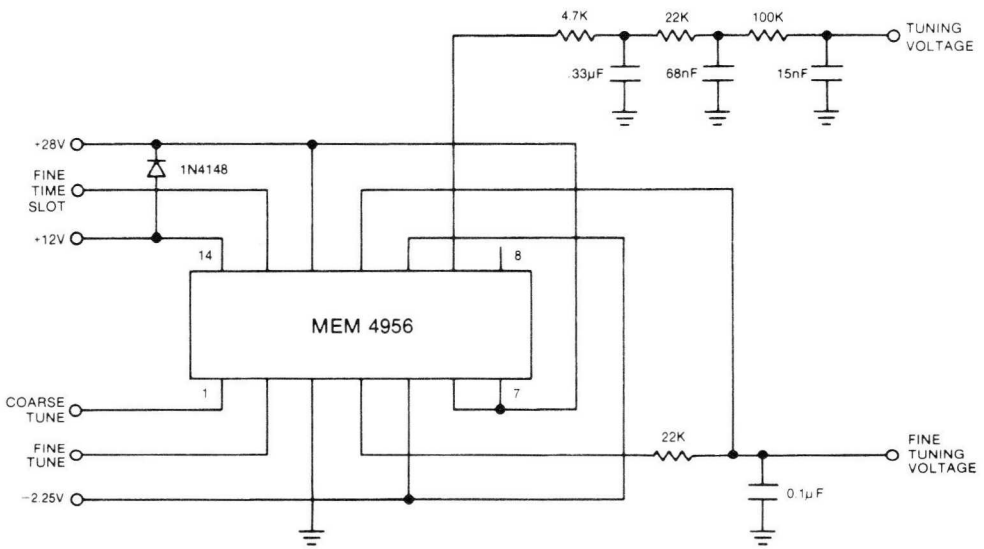
STANDBY

The −2.25 V_B supply may be reduced to 0V during standby provided that V_{DD}, V_{REF1} and V_{REF2} are reduced to +12V (V_{GG}). The V_B pins must not be open circuited.

BIAS SUPPLY

The −2.25 V_B supply must have a source impedance of 2.2K or less and be decoupled to V_{SS} by a 10nF ceramic capacitor.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage of any pin with respect to V_{SS} pin 3 (except $V_{REF.1}$, $V_{REF.2}$, V_{DD} and V_B) ..... -0.3 to +20V
Voltage on $V_{REF.1}$, $V_{REF.2}$, V_{DD} with respect to V_{SS} pin ..... V_{GG} to +36V
Voltage on V_B with respect to V_{SS} pin ..... -4 to +0.3V
Storage Temperature Range ..... -40°C to +100°C
Ambient Operating Temperature Range ..... 0°C to +70°C

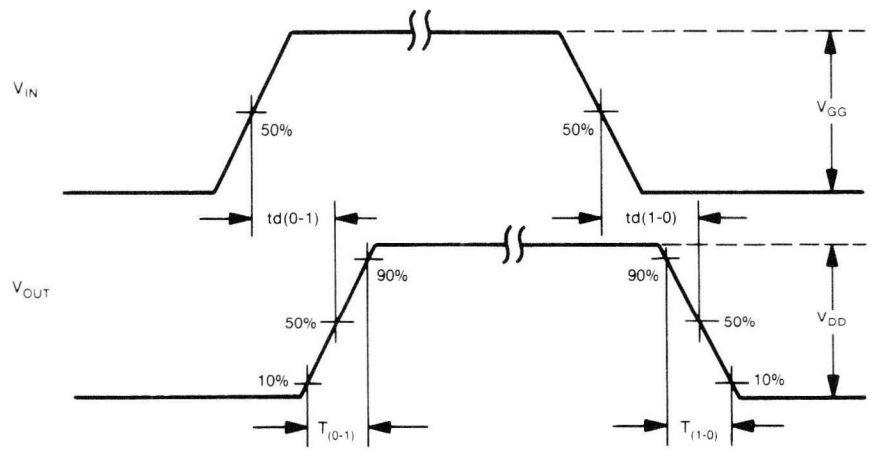
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{GG} = +12V ± 10%
$V_{DD} = V_{REF.1} = V_{REF.2}$ = +28 to +30V
V_B = −2.25V ± 10%
T_A = +25°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Input					
Logic '0'	-0.2	—	+0.3	Volts	
Logic '1'	10	—	V_{GG}	Volts	
Fine Tune Output on Resistance					
Logic '0'	—	70	200	Ω	
Logic '1'	—	100	300	Ω	
Tuning Voltage Output on Resistance					
Logic '0'	—	200	500	Ω	Pin 4 connected to Pin 11
Logic '1'	—	300	700	Ω	R1 = 10K
Output Propagation Delay					
Logic '0' to Logic '1'	—	90	—	ns	C1 = 100pF
Logic '1' to Logic '0'	—	80	—	ns	C1 = 100pF
Output Switching Time					
Logic '0' to Logic '1'	—	80	—	ns	
Logic '1' to Logic '0'	—	70	—	ns	
Supply Current					
V_{GG}	—	75	—	μA	$V_{DD} = V_{REF.1} = V_{REF.2}$ = +28V
V_B	—	75	—	μA	V_{GG} = +12V
V_{DD}, V_{REF1}, V_{REF2} (Total)	—	1.2	—	mA	V_B = −2.25V

TIMING DIAGRAM



ENTER-TAINMENT

ECONOMEGA / 16 Channel Digital Tuning System

FEATURES

- 8/12/16 Programs
- 3/4 Bands
- 10 bit Coarse-Tune
- 4 bit Fine-Tune
- Non-Volatile Memory without battery
- Auto or Manual Tuning
- Auto or Manual Band switching

DESCRIPTION

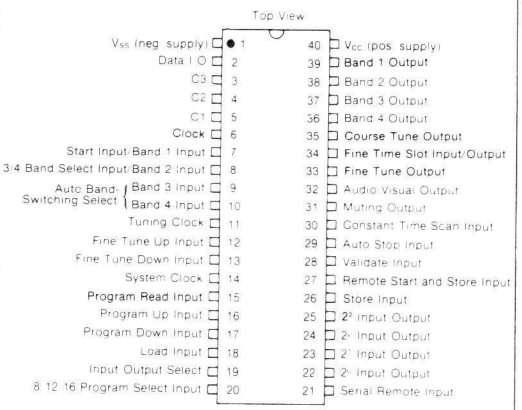
The ECONOMEGA Digital Tuning system is a three chip voltage synthesizer. The first chip (AY-5-8203) is an n-channel control chip which interfaces the remote control system, memory and D/A converter. The second chip (ER1400) is a non-volatile EAROM memory which stores the tuning and band information for 16 programs. The third chip is a CMOS Buffer amplifier/switch. This amplifies the converter output from the control chip to a fixed reference voltage and also contains the switch circuitry for the fine time slot. For details on the MEM4956 D/A converter circuit and the ER1400 EAROM, refer to the separate data sheet in this section.

NOTE: 10 bits of coarse time and 4 bits of fine tune does not mean the resolution is 14 bits (described later). The overall resolution is:

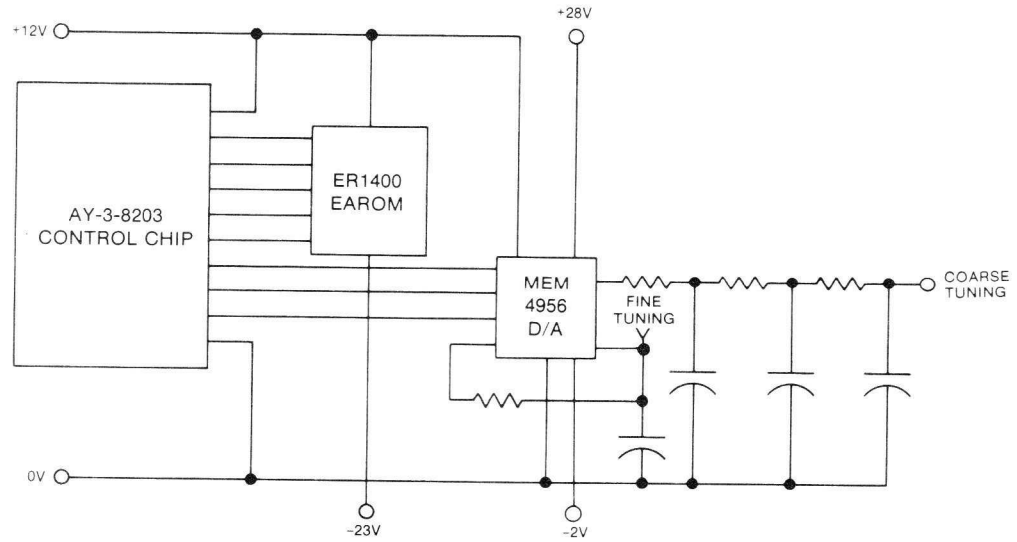
Band 3 — 11 bits
Bands 1, 2, & 4 — 10 bits

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8203



SYSTEM BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Ground
2	Data I/O	To ER1400 EAROM
3	C3	To ER1400 EAROM
4	C2	To ER1400 EAROM
5	C1	To ER1400 EAROM
6	15.6kHz	Control Chip Clock +128
7	Band 1 Input (Start Input)	When connected to V_{SS} selects Band 1 and initiates scan. (Connect to V_{SS} to start scan).
8	Band 2 Input (3/4 Band Select Input)	When connected to V_{SS} selects Band 2 and initiates scan. (Connect to V_{SS} for Bands 1, 2, 3. Leave open for Bands 1, 2, 3, 4).
9	Band 3 Input } Auto Bandswitch Select Input	When connected to V_{SS} selects Band 3 and initiates scan. } Connect to V_{SS} for Auto Bandswitching.
10	Band 4 Input } Auto Bandswitch Select Input	When connected to V_{SS} selects Band 4 and initiates scan. } Connect to V_{SS} for Auto Bandswitching.
11	Tuning Clock	Controls speed of coarse and fine tuning, set by external R-C network. 1.28kHz nominal. Runs only while scanning.
12	Fine Tune Up Input	When connected to V_{SS} causes FT to increment automatically.
13	Fine Tune Down Input	When connected to V_{SS} causes FT to decrement automatically.
14	System Clock	System clock 2.0 MHz nominal set by external R-C network.
15	Program Read Input	When connected to V_{SS} reads EAROM (includes 20ms antibounce delay).
16	Program Up Input	When connected to V_{SS} increments program number by 1. There is a 20msec antibounce delay on this input.
17	Program Down Input	When connected to V_{SS} decrements program number by 1. There is a 20msec antibounce delay on this input.
18	Load Input	When connected to V_{SS} new data is loaded into program number register from the program number inputs and the EAROM data is read. When left open the program number inputs are inhibited.
19	Input/Output Select	When connected to V_{SS} selects input mode for 2^0, 2^1, 2^2, 2^3 pins.
20	8/12/16 Program Select Input	Fixes the number of programs that can be selected using the Program UP and DOWN inputs. Open circuit =12, V_{SS}=16, V_{CC}=8.
21	Serial Remote Input	Accepts a train of 0.5msec negative pulses, the number of pulses determines the program number to be selected.
22	2^0 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
23	2^1 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
24	2^2 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
25	2^3 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
26	Store Input	When connected to V_{SS} stores Tuning and Band information in EAROM.
27	Remote Start and Store Input	A short positive pulse (<1msec) initiates scanning. A long positive pulse (>3msec) stores the tuning and band information in the EAROM.
28	Validate Input	Confirms valid stop command. Positive for a valid TV signal.
29	Auto Stop Input	Initiates Autostop sequence on a positive going edge (except in constant time scan mode when a negative edge is used).
30	Constant Time Scan Input	When connected to V_{SS} a constant scan rate of 8 sec. per Band is selected. In addition on Band 3 stop is executed on a negative edge rather than a positive edge and the Muting output is active low with the same output specification as Band.
31	Muting Output	Active high during scan and program change (active low in constant time scan mode and Auto Band Switching mode).
32	Audio Visual Output	Goes to logic '0' when the last program is selected (8, 12 or 16) and is on Band 3.
33	Fine Tune Output	Fine Tuning Information, 4 bits resolution.
34	Fine Time Slot Input/Output	Used by MEM4956 CMOS D/A to combine Coarse and Fine data when separate FT is not required. Connect to V_{SS} when MEM4956 is not used to invert CT and FT Outputs. The Fine Tune slot is a 2μsec pulse repeated every 250μsec on Band 3, a 10μsec pulse on Bands 2 and 4 and a 30μsec pulse on Band 1.
35	Coarse Tune Output	Coarse Tuning Information, 10 bits resolution.
36	Band 4 Output	This output goes to logic '0' when Band 4 is selected.
37	Band 3 Output	This output goes to logic '0' when Band 3 is selected.
38	Band 2 Output	This output goes to logic '0' when Band 2 is selected.
39	Band 1 Output	This output goes to logic '0' when Band 1 is selected.
40	V_{CC}	Positive power supply, +12V ± 10%.

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... −0.3V to +20 Volts
Storage Temperature Range ..... −65°C to +150°C
Ambient Operating Temperature Range ..... 0°C to +70°C
Package Thermal Resistance ..... 63°C/Watt

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = OV
V_{CC} = +12V ± 10%
System Clock = 1.44 to 2.15MHz (2.0MHz nominal)

Parameter	Min	Typ**	Max	Units	Conditions
Control Inputs					
Logic '0' Level	—	—	1.0	Volts	
Logic '1' Level	8	—	V_{CC}	Volts	
Resistance	200	400	1200	kΩ	to V_{CC}
Program No Inputs					
Logic '0' Level	—	—	0.5	Volts	
Logic '1' Level	8	—	—	Volts	
Resistance	100	200	600	kΩ	to V_{CC}
8/12/16 Input					
Logic '0' Level	—	—	0.5	Volts	
Logic 0/1 Level	—	open	—		
Logic '1' Level	10	—	—	Volts	
Input Resistance	30	100	300	kΩ	
Band, AV, Outputs					
Logic '0' Level	—	—	2	Volts	I_{sink} = 5mA
Off Leakage	—	—	10	μA	V_{out} = V_{CC}
Muting Output					
Logic '1' Level	6	—	—	Volts	Isource = 2mA
Off Leakage	—	—	10	μA	Note 1.
Program Outputs					
Logic '0' Level	—	—	0.4	Volts	Isink = 1.6mA
Logic '1' Level	8	—	—	Volts	Isource = 10μA
Supply Current					
V_{CC} (+12)	—	51.8	—	mA	at +25°C
	—	—	60	mA	at 13V and +70°C

**Typical values are at +25°C and nominal voltages.
NOTE: 1. In the constant time scan mode, the Muting Output has the same specification as the Band and AV outputs.

OPERATION

1. Coarse Tune
The coarse tune resolution is 10 bits with a predominant output ripple at 3.9kHz.

2. Fine Tune
The fine tune resolution is 4 bits with an output ripple at 15.6kHz. The fine tune steps twice per second related to system clock; it does not wrap around or overflow into coarse tune. During scanning it is reset to mid range.

3. Scanning
The actual tuning rates are fixed by the Tuning Clock and may be adjusted over wide limits. Typical figures are shown below.

(a) Normal Mode

Operation of a band button initiates scanning on the selected band, typical scan rates are as follows:

Band	Scan Time
1	0.8 sec.
2	1.6 sec.
3	8.0 sec.
4	1.6 sec.

(b) Constant Time Scan Mode

Operation of a band button initiates scanning on the selected band. The scan rate is a constant 8 seconds for each band.

(c) Auto Band Switching Mode

At the end of each scan the band is automatically changed in the sequence 1, 2, 3, 4. In the 3 band mode, band 4 is omitted.

4. Auto Stop and Validate
In the Normal Mode a stop is executed immediately on a positive going input transition. If validate goes positive within 256msec the system stops, if not the scan will restart (See Fig. 1 for a suggested validate circuit).

At the end of a band the tuning voltage goes back to zero and after a delay of 256msec scanning restarts. In the Constant Time Scan mode in Band 3, the stop is executed on a negative going transition.

5. Manual Operation
In the Normal Mode Stop and Validate can be linked to the Band Inputs to give full manual control of the tuning operation.

6. Muting
The Muting output is active from the time that a Scan is initiated until the Validate input goes positive after a Stop command. When a program change is made the Muting output is activated for 256msec.

7. Tuning Procedure

(a) 1. Select required program number (1 to 16).
2. Press required band button, scanning commences from the station currently tuned, scanning stops at the next station.
3. Fine tune if required.
4. Store Data.

(b) Alternatively using the circuitry shown in Fig. 2, the following procedure is available:
1. Press Band or Start.
2. Press Store.
3. Press required program.

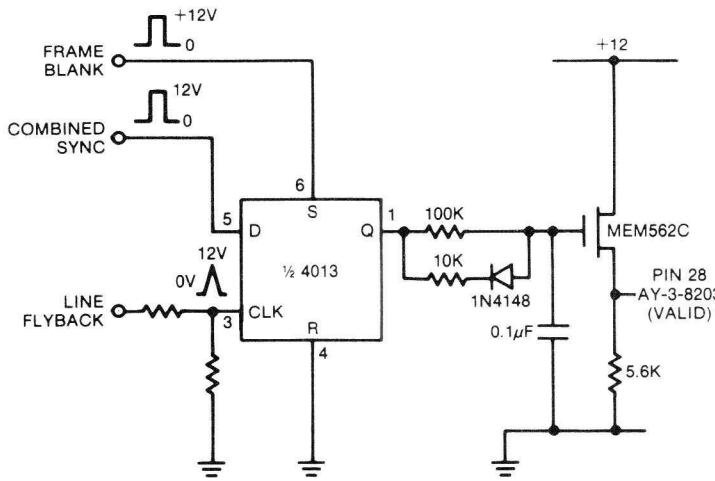


Fig.1 "VALID" CIRCUIT

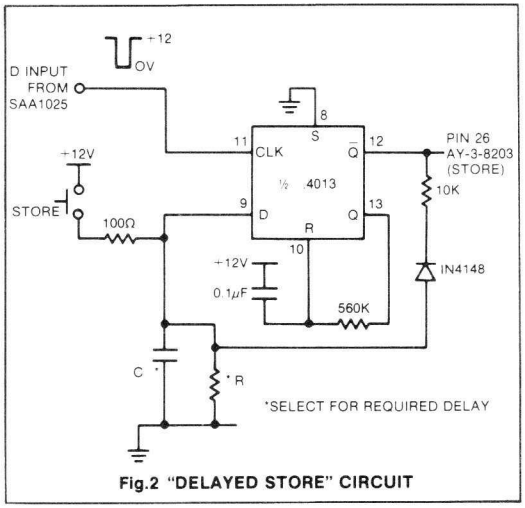


Fig.2 "DELAYED STORE" CIRCUIT

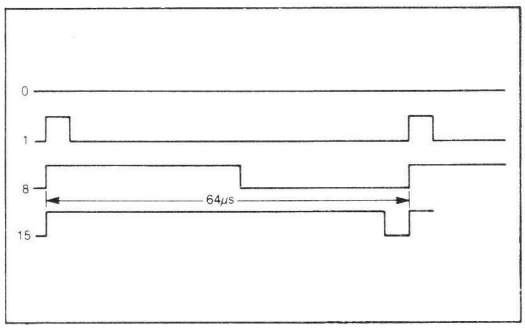
8. Fine Tune Resolution

When the MEM4956 D/A is used to combine the Coarse and Fine Data the relationship between Coarse Tune and Fine Tune is as follows:

Band 1	1 FT step = 7.5 CT steps
Band 2, 4	1 FT step = 2.5 CT steps
Band 3	1 FT step = 0.5 CT steps

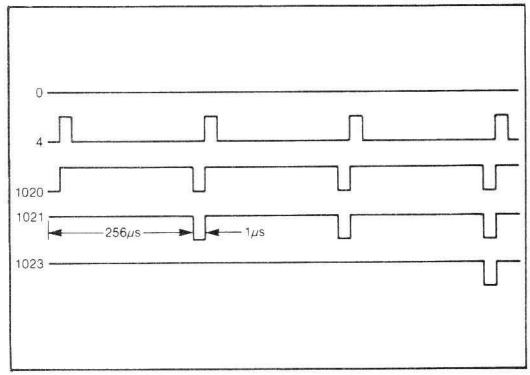
9. Additional Fine Tune Information

The fine tune output is a rectangular waveform with a frequency of 15.6kHz (system clock +128). The mark/space ratio defines the fine tune level, 16 steps being possible. The following diagram relates the binary number within the fine tune store to the output waveform. Bit width is approximately 3.8μs for a 15.6kHz output waveform.



10. Additional Coarse Tune Information

The Coarse tune output is a rectangular waveform with a predominant ripple frequency of 3.9kHz (system clock +512). The mark/space ratio indicates the coarse tune level. The addition of a coarse tune bit increases the mark period by approx. 1.0μs for a 2.0MHz clock. There are thus 256 bits within the 3.9kHz period. This accounts for 8 of the 10 coarse tune bits. The information from the remaining 2 bits (LS Bits) is used to add 0, 1, 2, or 3 extra bit periods (1.0μs) over 4 periods of the basic waveform. The complete coarse tune waveform repeats every 1ms.

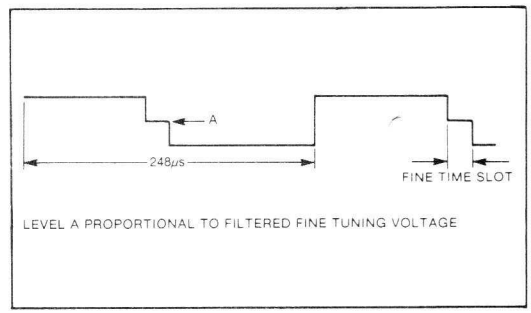


11. MEM4956 Buffer

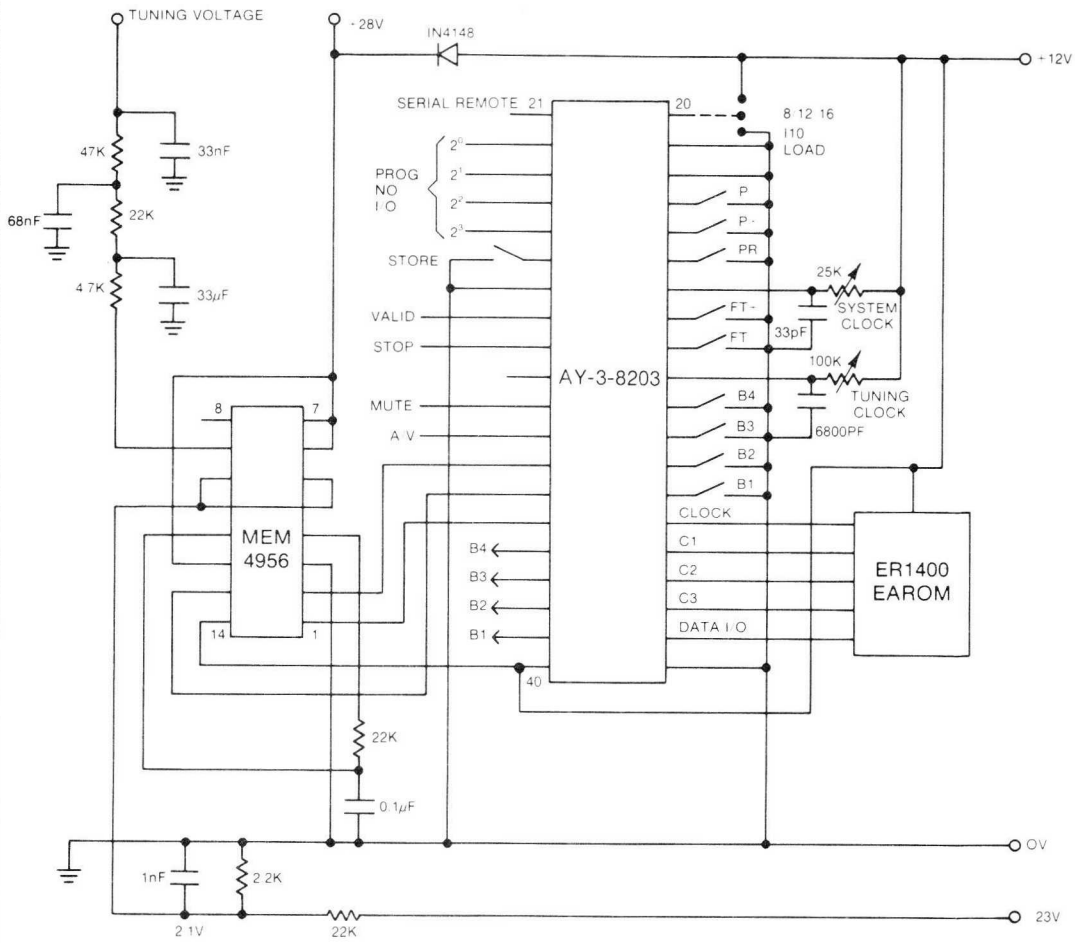
This buffer combines coarse and fine data under the control of the Fine Time slot output from the control chip.

The fine time slot controls the CMOS switch and hence the times the coarse tune or fine tune information are routed to the output filter. Note the fine tune waveform is filtered before being routed to the switch.

A typical output waveform of pin 9 of the device is shown below.



SYSTEM DIAGRAM



ENTER-TAINMENT

TV Time/Channel Display Circuits

FEATURES

- Channel Display 0 to 15 or 1 to 16 or 00 to 99.
- 4 Digit Clock Display option.
- Color character on black background or color character on color background.
- 14 or 24 DIL package.

OPTIONS

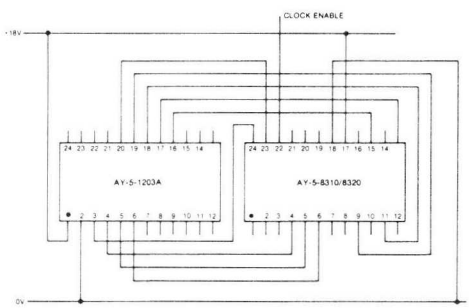
Part Number	Channel	Time
AY-5-8300	0-15	No
AY-5-8301	1-16	No
AY-5-8310/11	0-15 or 00-99	Yes
AY-5-8320/21/22/24	1-16	Yes*

*The AY-5-8320/21/22/24 are capable of either simultaneous or separate time and channel display and have automatic display enable.

DESCRIPTION

The AY-5-8300 series is a family of MOS circuits designed to display channel and time information on the screen of a TV set. The information is displayed as color characters on a black or color background. Channel information is displayed either as a single character 0 to 15 or 1 to 16 or as a dual character 00 to 99. Time is provided as a 4 digit hours and minutes display. The display is positioned at the top right hand corner or at the bottom center of the screen; the display may be permanent or momentary. Any of the AY-5-8300 series except the AY-5-8324 may be used for either 525 or 625 line systems; the AY-5-8324 is for use with 625 line systems only.

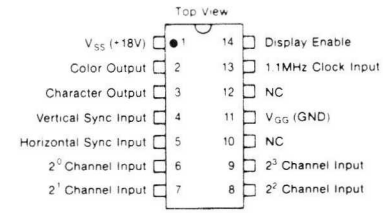
INTERCONNECT DIAGRAM FOR TV TIME DISPLAY



PIN CONFIGURATION

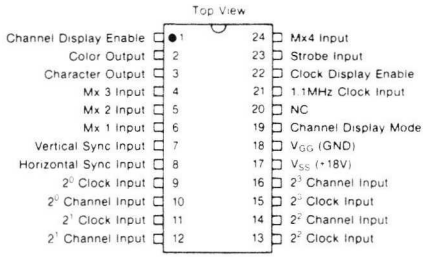
14 LEAD DUAL IN LINE

AY-5-8300/01

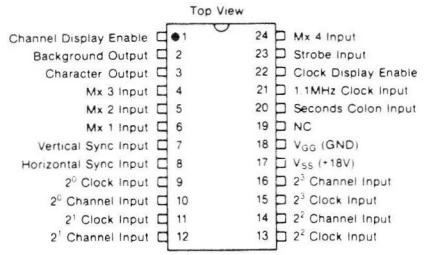


24 LEAD DUAL IN LINE

AY-5-8310/11



AY-5-8320/21/22/24



PIN FUNCTIONS

Name	Function
ALL TYPES:	
Vertical Sync Input	Resets the circuit at the end of each frame. At logic '0' during vertical flyback.
Horizontal Sync Input	Activates the line counter. At logic '0' during horizontal flyback.
1.1 MHz Clock Input	Determines character position and width. Must be synchronized by horizontal sync pulse to prevent ragged edges on character.
Channel Inputs 2^0-2^3	See table below.
AY-5-8300/01	
Display Enable	When taken to logic '0', the display is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
AY-5-8300/01/10/11	
Character Output	Defines the background border and the character.
Color Output	Determines the character color. Goes to logic '1' during a character block.
AY-5-8310/11	
Channel Display Enable	When taken to logic '0', the channel display is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
Clock Display Enable	When taken to logic '0', the clock display is enabled.
Channel Display Mode	When at logic "0", the 0-15 channel mode is selected: logic "1" for 00-99 channel mode.
AY-5-8310/11/20/21/22/24	
Clock Inputs 2^0-2^3	Multiplexed 4 digit BCD clock data inputs such as available from the AY-5-1203A clock circuit.
Mx1-Mx4	Multiplex inputs, at logic '1' during multiplex time slot. For the AY-5-8310/11, when operating in the 00-99 channel mode, Mx1 and Mx2 time slots are used.
Strobe Input	This input must go to a logic '1' during the middle of each Mx time slot to load the clock data into the chip.
AY-5-8320/21/22/24	
Character Output	Defines the character outlines. At logic '1' when displaying a character.
Background Output	Defines the background block. At logic '1' when outputting background.
Channel Display Enable	When taken to logic '1', the channel display is enabled. The display is automatically enabled when the channel is changed.
Clock Display Enable	When taken to logic '1', the clock display is enabled.
Seconds Colon Input	This input controls the colon between the hours and minutes display. When at logic '0', the colon is blanked. If connected to the DP output of the AY-5-1203A clock circuit, the colon will flash once per second.

Code 2^3 2^2 2^1 2^0	Display AY-5-8300	Display AY-5-8301/20/21/22/24	Display AY-3-8310/11
0 0 0 0	0	1	0 0*
0 0 0 1	1	2	1 1
0 0 1 0	2	3	2 2
0 0 1 1	3	4	3 3
0 1 0 0	4	5	4 4
0 1 0 1	5	6	5 5
0 1 1 0	6	7	6 6
0 1 1 1	7	8	7 7
1 0 0 0	8	9	8 8
1 0 0 1	9	10	9 9
1 0 1 0	10	11	10 —
1 0 1 1	11	12	11 —
1 1 0 0	12	13	12 —
1 1 0 1	13	14	13 —
1 1 1 0	14	15	14 —
1 1 1 1	15	16	15 —

*00-99 MODE.

ENTER-TAINMENT

OPERATION

The display is positioned digitally in both the vertical and horizontal directions. The vertical position is determined by counting horizontal sync pulses (the counting is initiated by the vertical sync pulse). The timing relationships are shown in Figs. 8a and 8b. Additionally, for the AY-5-8320/21/22/24, the time display is positioned 35 lines further down so that it appears immediately below the channel display.

In the horizontal direction the display is positioned by counting pulses from an external 1.1 MHz oscillator which is synchronized with the horizontal sync pulse to prevent ragged edges on each character.

Each character is made up of 15 dots in a 3×5 matrix. With a one dot border around each character a total matrix of 35 dots in a 5×7 format is utilized. Each dot lasts 0.9μsec in the horizontal direction and is 5 lines high. This gives a rectangular dot and characters as shown in Figs. 1a and 1b.

The various channel/time display formats are illustrated in Figs. 4, 6 and 7. The display positioning on the TV screen is shown in Figs. 6a and 6b.

In the AY-5-8300/01/10/11, the character display is controlled by two outputs. Character and Color. The video channels are controlled in the following manner:

(a) Black/white display

Character	Color	
0	0	Normal picture
1	0	Black (luminance channel full off)
1	1	Black
0	1	White

(b) Black/Yellow display

Character	Color	Normal picture
1	0	Black (luminance full off)
1	1	Black (luminance full off and blue suppressed)
0	1	Yellow (luminance full on and blue suppressed)

Other color displays are generated by suppressing one or two chrominance channels.

In the AY-5-8320/21/22/24, one video output defines the characters and the other a background block. Using these outputs, a display of any color character on a background of any color may be obtained.

The channel data is input on four lines; in the 0—15 or 1—16 channel mode, this information is applied in binary from a diode encoder attached to the varactor tuning drivers. Binary numbers greater than 9 are detected and displayed as a two digit character.

In the clock mode, data is entered on a 4 line BCD bus multiplexed into 4 time slots. A strobe signal occurring in the middle of each time slot is used to read the data into the chip. When the AY-5-1203A clock is used it can be directly connected to the AY-5-8310/11/20/21/22/24 with no external components. The AY-5-8310/11 displays the time with hours and minutes (Fig. 4); the AY-5-8320/21/22/24 displays the time with hours, minutes and a flashing colon for seconds (Fig. 5).

In the 00-99 channel mode the data is entered as a two digit BCD number in Multiplex time slots 1 and 2 in the same manner as the clock formation.

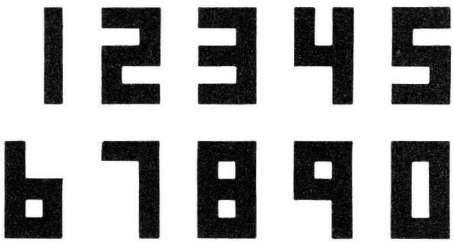


Fig. 1a CHARACTER SET (AY-5-8300/10)

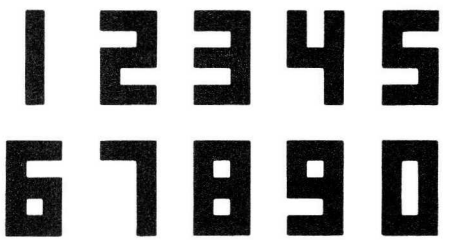


Fig. 1b CHARACTER SET (AY-5-8301/11/20/21/22/24)

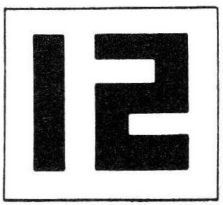


Fig. 2 CHANNEL DISPLAY

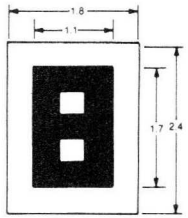


Fig. 3 CHARACTER SIZE (25/26 INCH SCREEN)

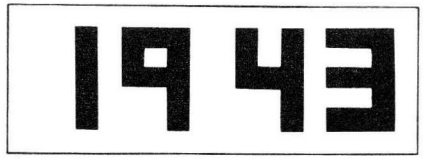


Fig.4 TIME DISPLAY (AY-5-8310/11)

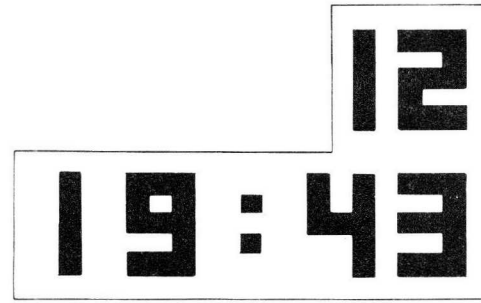


Fig.5 TIME AND CHANNEL DISPLAY (AY-5-8320/21/22/24)

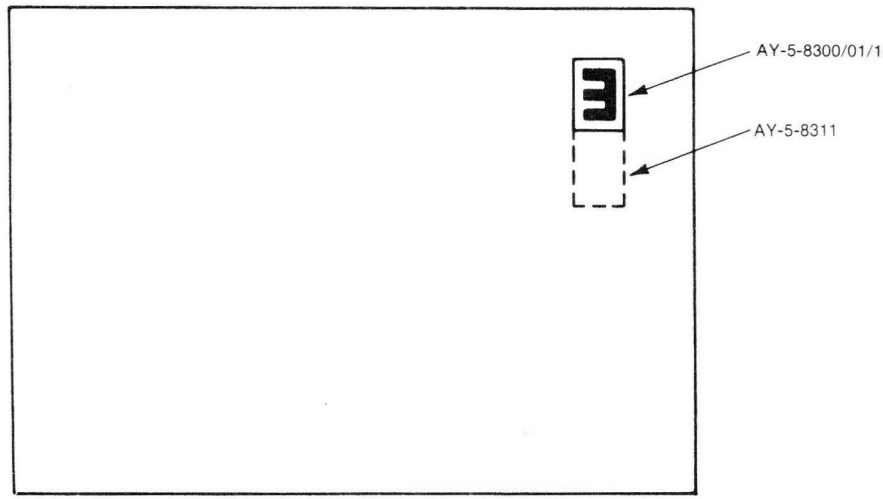


Fig.6a DISPLAY POSITION-CHANNEL (AY-5-8300/01/10/11) OR TIME (AY-5-8310/11)

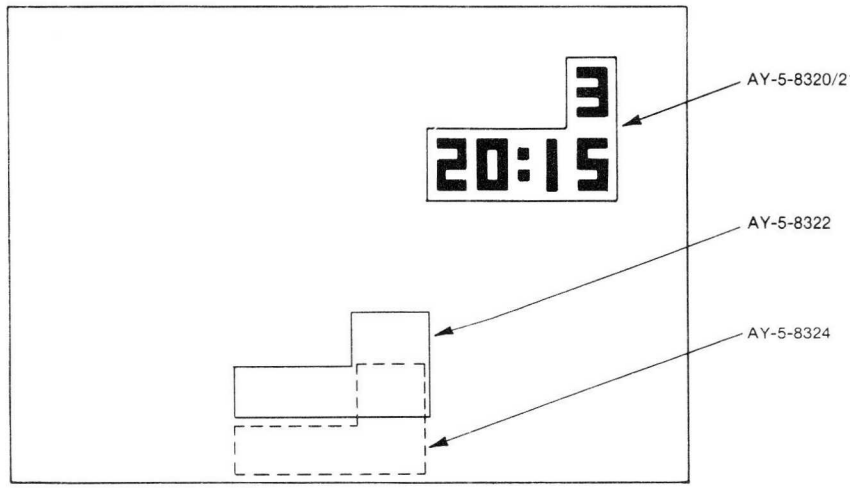


Fig.6b DISPLAY POSITION-CHANNEL (AY-5-8300/01/10/11)

ENTER-TAINMENT

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . . 0°C to +85°C
Storage temperature range. . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +17V to +19V
Operating Temperature (T_A) = 0°C to +85°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	Volts	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −1.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	1.0	1.1	1.15	MHz	
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	300	ns	10% to 90%
Pulse width	250	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	Volts	
Leakage	—	—	10	μA	V_{IN} = (V_{SS}−19) Volts
Display Enable Inputs					
Switch point positive edge	V_{SS} −8	—	V_{SS} −5	Volts	
Outputs					
On resistance	—	—	1.5	kΩ	V_{OUT} = V_{SS} −2V
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power: AY-5-8300/01/10	—	—	400	mW	V_{SS} = +19V
AY-5-8320	—	—	750	mW	V_{SS} = +19V

**Typical values are at +25°C and nominal voltages.
NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 50μA.

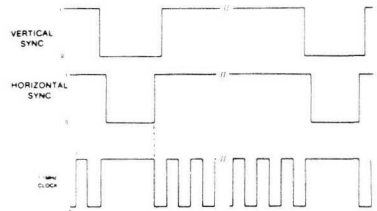


Fig. 7 INPUT WAVEFORMS

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +11.4V to +12.6V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.5	Volts	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS}−1.0	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	1.0	1.1	1.15	MHz	
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time		—	100	ns	10% to 90%
Pulse width	300	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.5	Volts	
Clock Inputs, Multiplex, Strobe Inputs					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS}−0.3	—	V_{SS} +0.3	Volts	
Input Resistance	—	20	—	kΩ	To V_{GG}
Display Enable Inputs					
Switch point positive edge	V_{SS}−5.5	—	V_{SS} −3.5	Volts	
Outputs					
On resistance	—	—	1	kΩ	$V_{OUT} = V_{SS}$ −2V
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power	—	150	—	mW	V_{SS} = +12V

**Typical values are at +25°C and nominal voltages.
NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 0.5mA.

ENTER-TAINMENT

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . 0°C to +70°C
Storage temperature range . . . . . −65°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +11.4V to +12.6V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	1.0	1.1	1.15	MHz	
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	100	ns	10% to 90%
Pulse width	300	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	Volts	
Clock Inputs, Multiplex, Strobe Inputs					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} − 0.5	—	V_{SS} +0.3	Volts	
Input Resistance	—	20	—	kΩ	To V_{GG}
Display Enable Inputs					
Switch point negative edge	V_{SS} −5.5	—	V_{SS} −3.5	Volts	
Outputs					
On resistance	—	—	1	kΩ	V_{OUT} = V_{SS} −2V
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power	—	150	—	mW	V_{SS} = +12V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 0.5mA.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +12.35V to +14.0V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.8	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.8	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	0.8	1.173	1.25	MHz	
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.8	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	100	ns	10% to 90%
Pulse width	280	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −3.8	—	V_{SS} +0.3	Volts	
Clock Inputs, Multiplex, Strobe Inputs					
Logic '0'	0	—	3	Volts	
Logic '1'	V_{SS} −0.5	—	V_{SS} +0.3	Volts	
Input Resistance	—	35	—	kΩ	To V_{GG}
Display Enable Inputs					
Switch point negative edge	V_{SS}-6	—	V_{SS} −3.8	Volts	
Outputs					
On resistance	—	—	1.5	kΩ	$V_{OUT} = V_{SS}$ −2V (Note 2)
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power	—	300	—	mW	V_{SS} = +13V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 0.5mA.
2. The output current must be limited to 5mA.

ENTER-TAINMENT

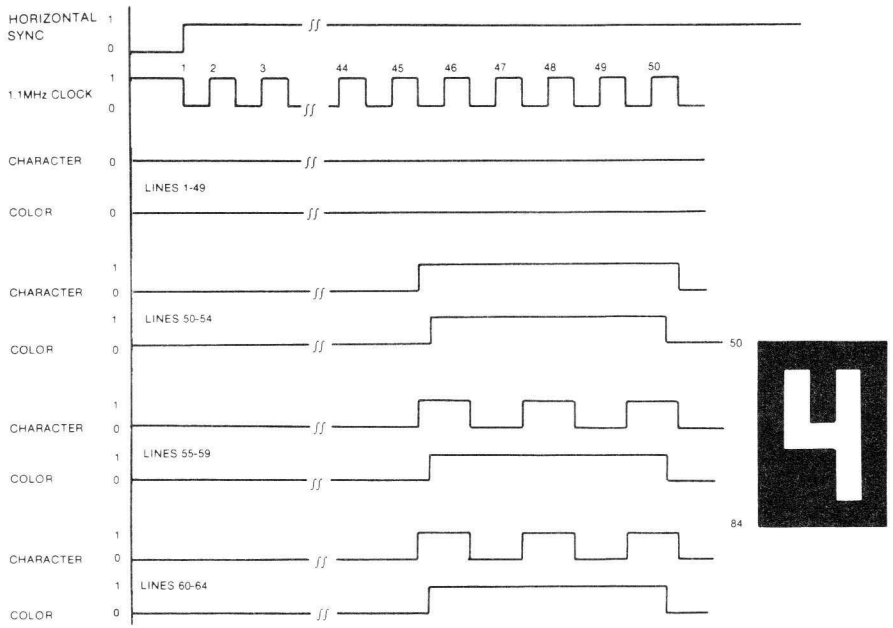


Fig. 8a OUTPUT WAVEFORMS (AY-5-8300/01/10)
(AY-5-8311 AS ABOVE BUT DISPLAY STARTS AT LINE 85.)

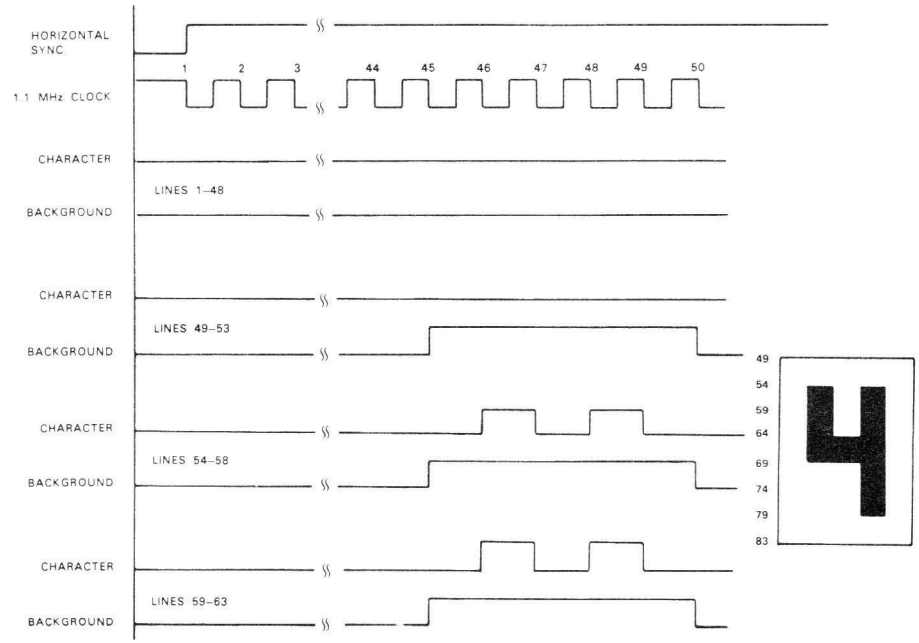


Fig. 8b OUTPUT WAVEFORMS (AY-5-8320/21)
(AY-5-8322 AS ABOVE BUT DISPLAY STARTS AT LINE 165.
AY-5-8324 AS ABOVE BUT DISPLAY STARTS AT LINE 220.)

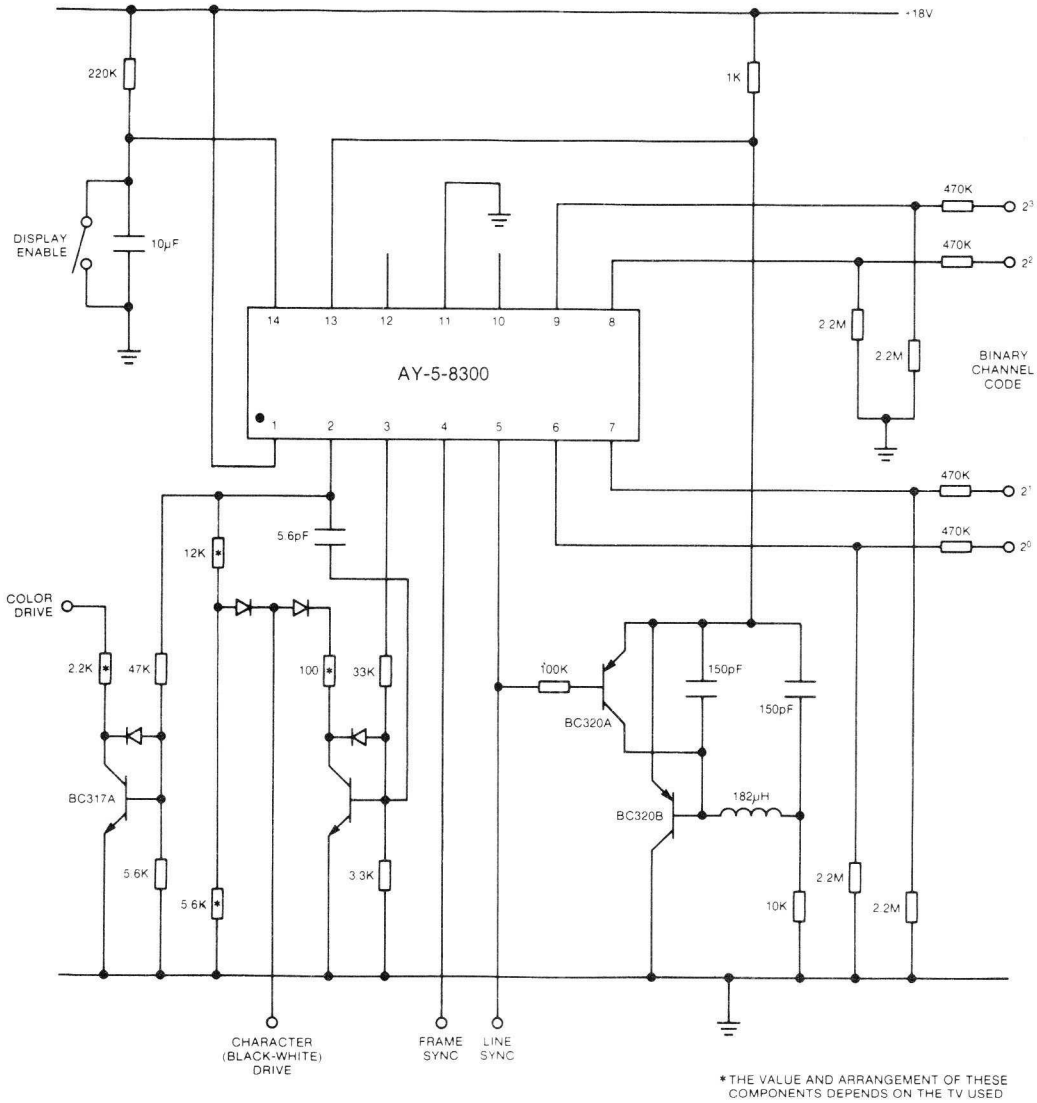


Fig.9

ENTER-TAINMENT

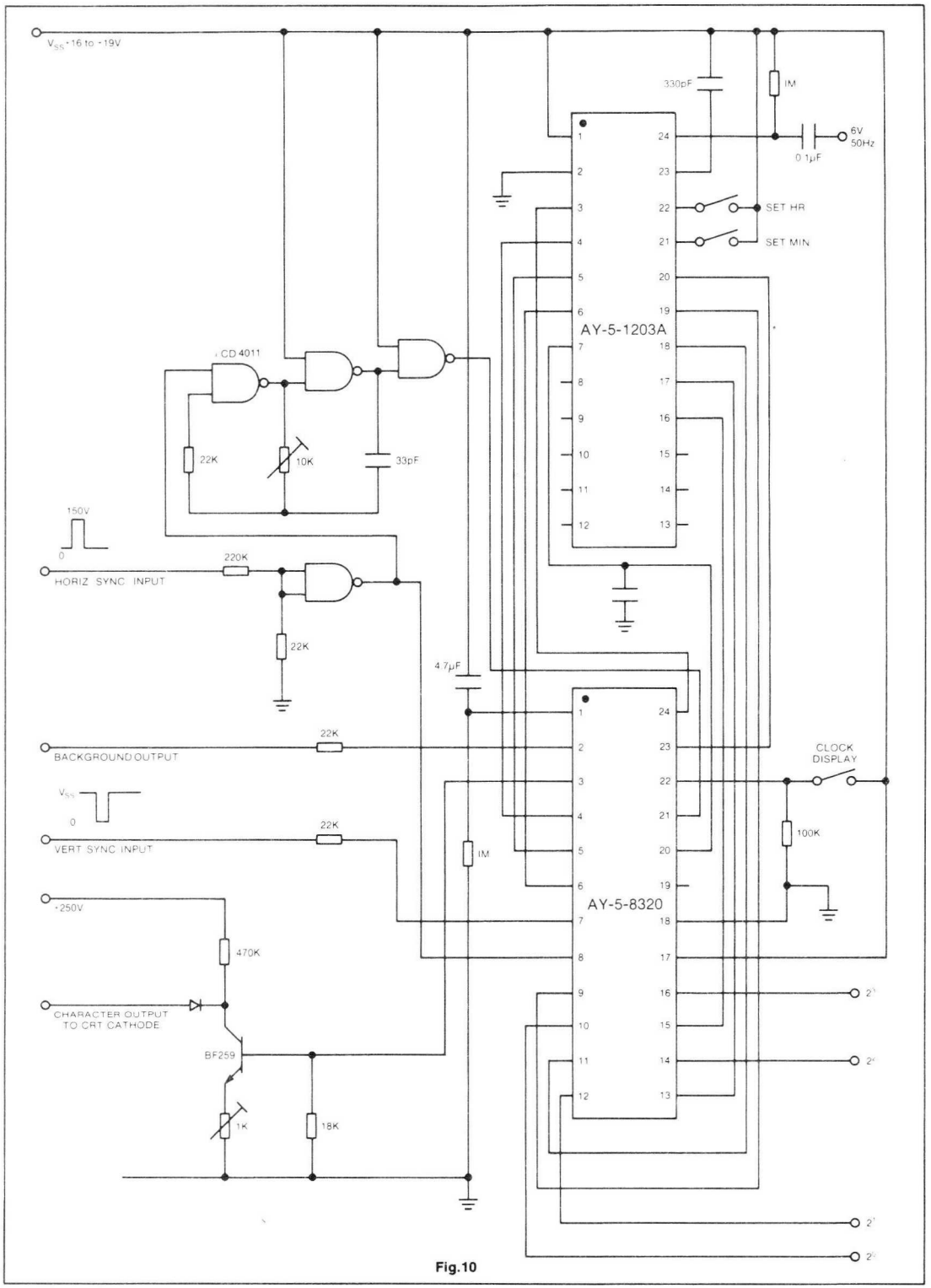

V_{SS} +16 to +19V
330pF
1M
6V
50Hz
0.1μF
SET HR
SET MIN
AY-5-1203A
CD 4011
22K
10K
33pF
150V
0
HORIZ SYNC INPUT
220K
22K
4.7μF
22K
BACKGROUND OUTPUT
V_{SS}
0
22K
VERT SYNC INPUT
1M
CLOCK
DISPLAY
100K
AY-5-8320
+250V
470K
CHARACTER OUTPUT
TO CRT CATHODE
BF259
1K
18K

Fig.10

Electronic On-Screen TV Tuning Scales

FEATURES

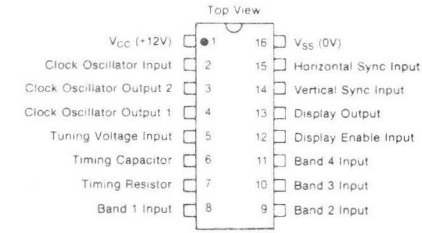
- Electronic tuning scale for 4 bands.
- Mask programmable for Band or Channel number display.
- Mask programmable for display position.
- 12V operation compatible with G.I. digital tuning systems.

DESCRIPTION

The AY-3-8330A/8331/8335 are designed to provide an electronic on-screen tuning scale for varactor tuned TV sets. A horizontal line of variable length shows the tuning voltage and a scale is provided to aid tuning. Four bands are provided, band number or optional channel number being displayed. The band or channel number display may be mask programmed as desired within the limitation of 2 blocks of 5x7 dots (see Fig. 3). The graticule may also be programmed as required.

PIN CONFIGURATION

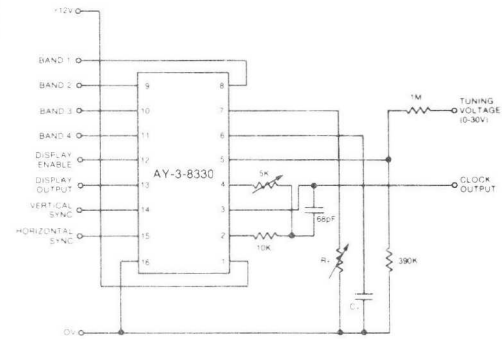
16 LEAD DUAL IN LINE



PIN FUNCTIONS

Name	Function
V_{CC}	Positive supply (+12V ± 10%)
V_{SS}	Ground
Horizontal Sync Input	Negative sync pulse from TV set
Vertical Sync Input	Negative sync pulse from TV set
Clock Input	1.1 MHz master clock which fixes display horizontal position.
Clock Output 1	Intermediate clock output
Clock Output 2	Output of on-chip oscillator synchronized by Horizontal Sync. May be used to drive AY-5-8320 Display Circuit.
Tuning Voltage Input	Tuning voltage from Varactor diodes. Length of tuning bar is proportional to this voltage.
Timing Capacitor	Connect timing capacitor from this pin to V_{SS}.
Timing Resistor	Connect adjustable timing resistor from this pin to V_{SS}.
Band 1 Select Input	Connect to V_{SS} to select required band, either channel number or band number information will be displayed.
Band 2 Select Input	
Band 3 Select Input	
Band 4 Select Input	
Display Output	Positive going output of video information.
Display Enable Input	Connect to V_{SS} to enable display

SYSTEM DIAGRAM



ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin ..... -0.3 to +20V
Storage temperature range ..... -65° C to +150° C
Ambient operating temperature range ..... 0° C to +70° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges ,are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +12V ± 10%
T_A = 0° C to +70° C
Clock frequency = 1.1 MHz

Parameter	Min	Typ**	Max	Units	Conditions
Inputs					
Logic '0'	0	—	+4	Volts	
Logic '1'	+8	—	Vcc	Volts	
Analog Input	0	—	+9	Volts	
Display Output					
Logic '0'	—	—	0.5	Volts	I sink = 1mA
Logic '1'	V_{CC} -1	—	—	Volts	I source = 1mA
Ton, Toff	—	—	200	nsec	
Power Supply Current	—	10	—	mA	

**Typical values are at +25° C and nominal voltages.

AY-3-8330A/8335 DISPLAY DIAGRAMS

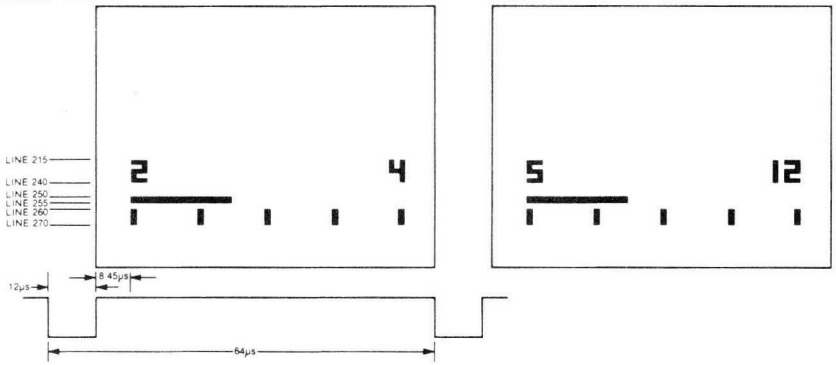


Fig. 1a BAND 1 DISPLAY

Fig. 1b BAND 2 DISPLAY

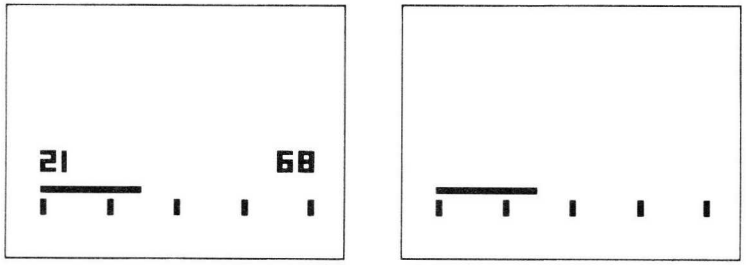


Fig.1c BAND 3 DISPLAY
(AY-3-8335 displays 69 instead of 68)

Fig. 1d BAND 4 DISPLAY

AY-3-8331 DISPLAY DIAGRAMS

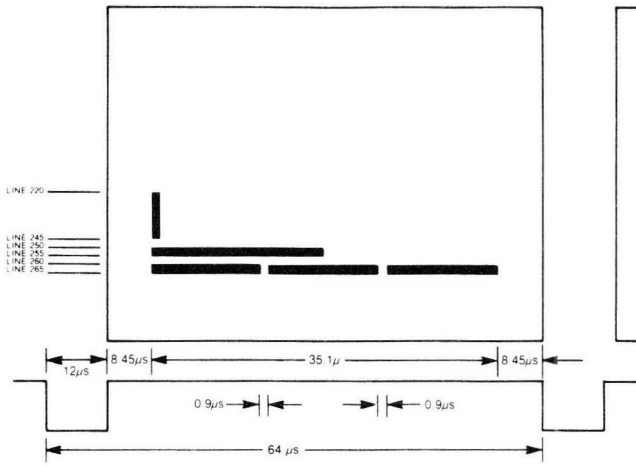


Fig. 2a BAND 1 DISPLAY

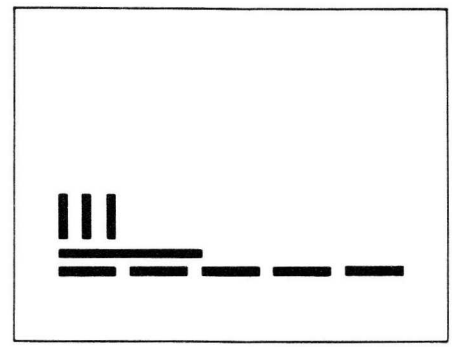


Fig. 2b BAND 2 DISPLAY

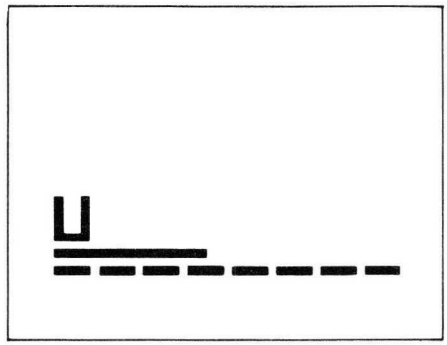


Fig. 2c BAND 3 DISPLAY

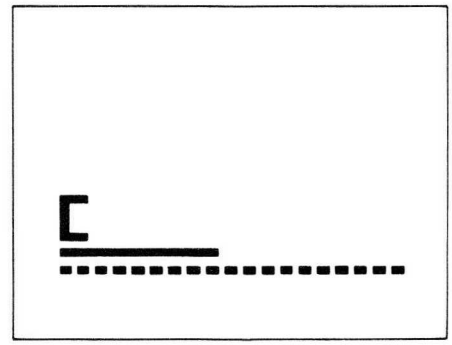


Fig. 2d BAND 4 DISPLAY

Fig. 3 TYPICAL CHARACTER FORMATS

ENTER-TAINMENT

REMOTE CONTROL

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
R/C SYSTEM I	30 channel discrete frequency ultrasonic transmitter.	SAA 1024	6-62
	30 channel discrete frequency ultrasonic receiver.	SAA 1025	6-64
R/C SYSTEM II	23 channel PCM ultrasonic or infrared transmitters.	AY-5-8410	6-68
		AY-5-8411	6-68
	31/63 channel PCM ultrasonic or infrared receiver.	AY-5-8420	6-70
R/C SYSTEM III	30 channel discrete frequency ultrasonic transmitter.	AY-5-8450	6-72
	16 channel discrete frequency ultrasonic receivers.	AY-5-8460	6-74
		AY-5-8461	6-74
R/C SYSTEM IV	264 command PCM infrared transmitter.	AY-3-8470	6-78
	264 command PCM infrared receiver.	AY-3-8475	6-81

30 Channel Remote Control Transmitter

DESCRIPTION

- 30 channels, 346.4Hz spacing in the range 34-44kHz.
- P-channel 9V battery operation.
- 4.4336MHz TV crystal master oscillator.
- Touch or mechanical keyboard, 1 of 5 and 1 of 6 coding.
- Low standby current drain (15 μA max.)
- Compatible with SAA1025, SAA1130, AY-5-8460, and AY-5-8461 receivers.

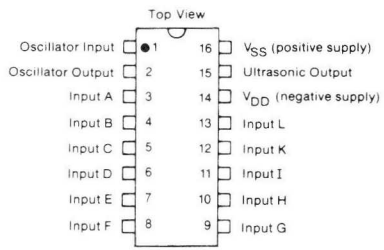
FEATURES

The SAA1024 allows the transmission of 30 commands using 30 different ultrasonic frequencies in the range 33.945 to 43.990 kHz. It is designed for battery operation and uses a low cost TV crystal as the master oscillator. When inactive the circuit is in a standby mode having a current drain of less than 15μA. As soon as a valid input code is applied the main circuit is powered up and transmission commences.

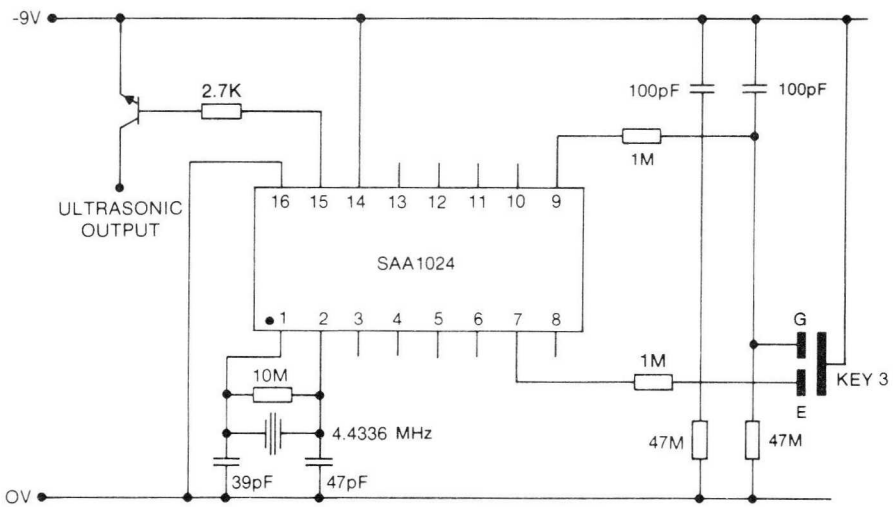
The code input can be generated by either a mechanical keyboard or a touch plate.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



TRANSMITTER WITH TOUCHPLATE INPUT



OUTPUT FREQUENCIES

Crystal = 4.4336 MHz

Key	Inputs (Logic 1)	Frequency
1	EH	33,945 Hz
2	EL	34,291 Hz
3	EG	34,638 Hz
4	EK	34,984 Hz
5	EF	35,330 Hz
6	EI	35,677 Hz
7	AF	36,023 Hz
8	AI	36,370 Hz
9	BF	36,716 Hz
10	BI	37,062 Hz

Key	Inputs (Logic 1)	Frequency
11	CF	37,409 Hz
12	CI	37,755 Hz
13	DF	38,101 Hz
14	DI	38,448 Hz
15	AG	38,794 Hz
16	AK	39,141 Hz
17	BG	39,487 Hz
18	BK	39,833 Hz
19	CG	40,180 Hz
20	CK	40,526 Hz

Key	Inputs (Logic 1)	Frequency
21	DG	40,872 Hz
22	DK	41,219 Hz
23	AH	41,565 Hz
24	AL	41,912 Hz
25	BH	42,258 Hz
26	BL	42,604 Hz
27	CH	42,951 Hz
28	CL	43,297 Hz
29	DH	43,643 Hz
30	DL	43,990 Hz

NOTE: The full key configuration/frequencies above are compatible with 30 channel receivers such as the GI SAA1025. For operation with 16 channel receivers, such as the GI AY-5-8460/8461, only keys 10 to 25 are required.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . . +0.3 to −12 Volts
Output current 10mA
Storage temperature range . . . . . −65°C to +150°C
Ambient operating temperature range . . . . . −10°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = −7 to −10V
Operating Temperature (T_A) = −10°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	—	4.4336	—	MHz	See diagram for external components.
Output Frequencies	—	See Table	—		
Input logic '0'	—	—	−0.5	V	
Input logic '1'	-4	—	—	V	
Input leakage	—	—	200	nA	at 70°C, Vin = −4V
Output On Resistance	—	500	—	Ω	to V_{SS}, V_{OUT} = −1V
Output Off Resistance	—	1.5	—	kΩ	to V_{DD}, V_{OUT} = V_{DD}+0.5V
Standby current drain	—	—	15	μA	
Operating current drain	—	8.0	—	mA	

**Typical values are at +25°C and nominal voltages.

ENTER-TAINMENT

30 Channel Remote Control Receiver

FEATURES

- 30 Control Channels, including 21 independent codes (e.g. for TV channel selection), an on/off signal, and 8 codes for the control of 3 analog outputs.
- Capability for direct interface to a local keyboard.
- Uses a 4.4336MHz TV crystal.

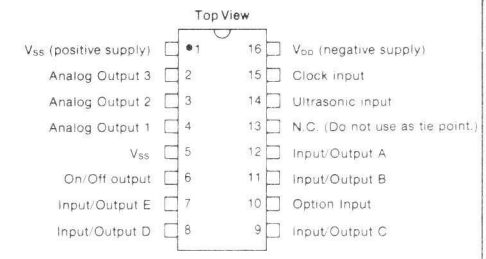
DESCRIPTION

The Receiver has 30 control channels, each channel being allocated a separate ultrasonic frequency. Twenty-one of the channels are independent (e.g. may be allocated to selection of TV programs), six are used to control three analog outputs; one for On/Off, one for Normalizing and one for Muting. All channels are output on a 5 line binary bus. The bus is also used as an input for local control from a keyboard.

The analog channels have a pulse width modulated output with 30 possible values, the time taken to go from maximum to minimum being 5.5 seconds. The Normalize signal sets Analog Outputs 1 and 2 to approximately their mid-point. The Mute signal alternately reduces Analog Output 3 to an "off" level, or returns it to its previously set level.

The ON/OFF channel toggles every time it is activated, there is a delay of approximately 0.7 seconds to prevent accidental operation.

PIN CONFIGURATION
16 LEAD DUAL IN LINE



To prevent false operation the frequency of the ultrasonic input is measured in the following manner. As soon as the signal appears a 23msec. timer is started, at the end of this period the room reflections will have died away.

The frequency is then measured for 23msec. and the appropriate output activated. If at any time a signal is received with a period shorter than 18μsec. or longer than 36μsec. the receiver is reset. Out of band and noisy signals are therefore rejected.

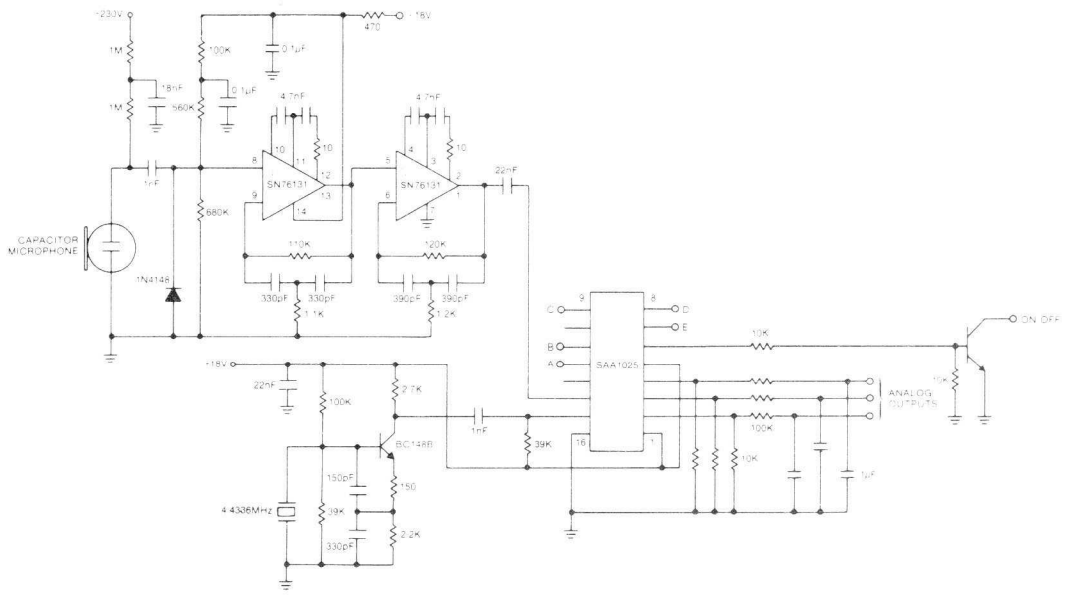


Fig. 1. ULTRASONIC PREAMP AND CRYSTAL OSCILLATOR

PIN FUNCTIONS

Pin No.	Name	Function
1,5	V_{SS}	Positive supply.
16	V_{DD}	Negative supply 18V nominal.
13	N.C.	Do not connect anything to this pin.
10	Option Input	Connect to V_{SS} for turn ON by channel select; leave open for turn ON and OFF by command 1 only.
15	Clock Input	This pin is driven by a 4.4336HMz crystal oscillator. The input signal should be a minimum of 4V peak to peak capacitively coupled.
14	Ultrasonic Input	The ultrasonic signal should be capacitively coupled and be at least 300 mV peak to peak. The first incoming pulse triggers a 23.1ms timer and after a delay of this period, two measurements of the ultrasonic signal are made over the following two 23.1ms periods. If the measurements produce a comparison, an output pulse 23.1ms long is generated after a further pause of 46.2ms. With continuous input signals an output pulse is generated every 184.8ms. During the complete receiving time the period of the ultrasonic signal is measured. If it is less than 18μsec or greater than 36μsec the signal is rejected and the receiver is set back to the start conditions and a new measuring cycle commences. The input signals need not be completely accurate for satisfactory reception. At the lowest frequency an error of $\pm$0.51% can be tolerated and at the highest $\pm$0.39%.
2, 3, 4	Analog Outputs	These outputs are in the form of a pulse, the mark to space ratio of which can be changed in 30 steps from 1:30 to 30:1, the repetition frequency being 8.99kHz. The mark space ratio is incremented by one step about 115msec after the start of an ultrasonic command, thereafter it is incremented every 184.8msec. The output state is an open drain MOS transistor which appears as a 1kOhm (Max.) resistor connected to V_{SS} when ON and an open circuit when OFF. At power ON the outputs are normalized to the following mark space ratios: Analog Output 1 18:13 Analog Output 2 16:15 Analog Output 3 10:21 When command 4 (Normalize) is received, Analog Outputs 1 and 2 are reset to their normalized values. Analog Output 3 is unchanged. When command 2 (Mute) is received, Analog Output 3 is turned OFF, a further command re-enables the output. A delay of approximately 0.7 seconds is built in to this control to prevent false operation. When Analog Output 3 is muted, the corresponding Up and Down commands are blocked. The Muting is cancelled if either the Mute command is repeated or an ON command is received.
6	ON/OFF Output	This output is toggled ON and OFF by the reception of command 1. The command must be present for 0.7 sec. At power ON the output is set to the OFF condition. When in the OFF condition the Analog outputs are prevented from changing. Also, when OFF, any one of the 16 F codes, if present for 0.7 seconds, will change this output to the ON condition. However, these signals will not switch the output to OFF. The output can also be switched ON by connecting pin 6 to V_{SS} for 10 microseconds.
7, 8, 9, 11, 12	Input/Output A, B, C, D, E	These pins have the dual function of receiving input commands from a local keyboard or touch plate and for providing output control signals in response to commands from the transmitter or the keyboard. When the receiver is inactive the pins are held to within 1 Volt of V_{SS} by R1 (Fig. 1). If a touch contact is activated current flows through R3 and R2 (Safety Isolating resistors) into R1 driving the input negative. When the input voltage exceeds 4 Volts for at least 10μsec the command is accepted and after a processing time of 46.2msec an output pulse 23.1msec long is generated. During the output pulse the output pin is driven negative by the output transistor. The output current is sufficient to drive TTL. When commands are received from both the remote transmitter and the local keyboard the local command takes precedence.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . . +0.3 to -20V
Output Current 10mA
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature Range . . . . . -20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = OV
V_{DD} = -16.5 to -19.5V
(T_A) = -20°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input	4	8	—	V_{P-P}	capacitively coupled
Clock Frequency	—	4.4336	—	MHz	
Ultrasonic Input	0.5	—	V_{DD}	V_{P-P}	capacitively coupled
Inputs A-E					
Logic '0'	+0.3	—	−1	Volts	
Logic '1'	-4	—	−19.5	Volts	
Outputs A—E					
Logic '0'	—	—	−0.5	Volts	RL = 4.7M to V_{SS}
Logic '1'	−5.5	—	—	Volts	Iout = 1.6mA (Fig. 2)
On/Off Output					
Off leakage	—	—	10	μA	Vout = −19.5 Volts
On resistance	—	—	1	kΩ	Vout = −1V (resistance to V_{SS})
Analog Outputs					
Off leakage	—	—	10	μA	Vout = −19.5 Volts
On resistance	—	—	1	kΩ	Vout = −1V (resistance to V_{SS})
Output frequency	—	8.99	—	kHz	
Increment time per stop	—	184.8	—	msec	
Chip Supply Current	—	25	—	mA	

**Typical values are at +25°C and nominal voltages.

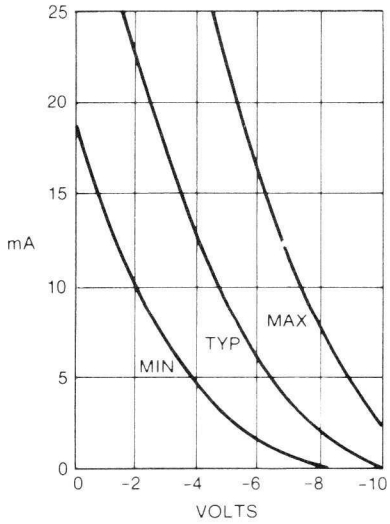


Fig.2 OUTPUT CHARACTERISTICS

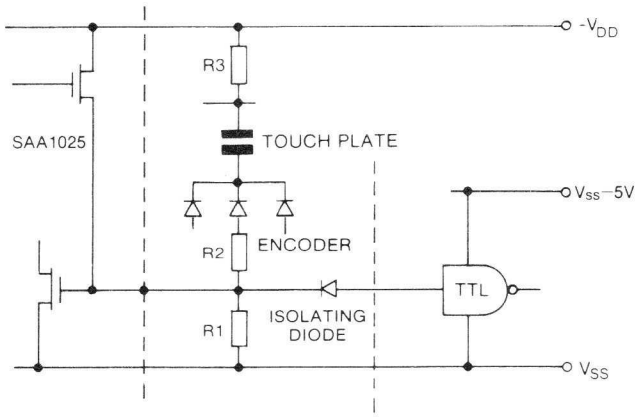


Fig.3 INPUT/OUTPUT CIRCUIT

Table 1: FREQUENCY ALLOCATIONS
Clock frequency 4.4336 MHz, Output in Negative logic

CH	Frequency Hz	Function	Output Code A	B	C	D	E
1	33,944.89	ON/OFF	1	0	0	0	0
2	34,291.21	Mute	1	0	0	0	1
3	34,637.65	Analog Output 1—Up	0	1	0	0	0
4	34,984.02	Normalize	0	1	0	0	1
5	35,330.40	Analog Output 1—Down	1	1	0	0	0
6	35,676.78	Z1	1	1	0	0	1
7	36,023.15	Analog Output 2—Up	0	0	1	0	0
8	36,369.53	Z2	0	0	1	0	1
9	36,715.91	Analog Output 2—Down	1	0	1	0	0
10	37,062.28	Z3	1	0	1	0	1
11	37,408.66	Analog Output 3—Up	0	1	1	0	0
12	37,755.03	Z4	0	1	1	0	1
13	38,101.41	Analog Output 3—Down	1	1	1	0	0
14	38,447.79	Z5	1	1	1	0	1
15	38,794.16	F1	0	0	0	1	0
16	39,140.54	F2	0	0	0	1	1
17	39,486.92	F3	1	0	0	1	0
18	39,833.29	F4	1	0	0	1	1
19	40,179.67	F5	0	1	0	1	0
20	40,526.05	F6	0	1	0	1	1
21	40,872.42	F7	1	1	0	1	0
22	41,218.80	F8	1	1	0	1	1
23	41,565.18	F9	0	0	1	1	0
24	41,911.55	F10	0	0	1	1	1
25	42,257.93	F11	1	0	1	1	0
26	42,604.31	F12	1	0	1	1	1
27	42,950.68	F13	0	1	1	1	0
28	43,297.06	F14	0	1	1	1	1
29	43,643.43	F15	1	1	1	1	0
30	43,989.81	F16	1	1	1	1	1

These functions also give an ON command

Table 2
The table below illustrates the use of the SAA 1025 R/C receiver with either the SAA 1024 or AY-5-8450 R/C transmitters for the GI Economega TV and Stereomega Hi-Fi digital tuning systems.

R/C Transmitters			R/C Receiver		
SAA1024 Key/Inputs	AY-5-8450 Key/Matrix	Frequency (Hz)	SAA1025 Function	Economega Function	Stereomega Function (Suggested Only)
1/EH	1/X1 Y1	33,945	On/Off	On/Off or Off	On/Off or Off
2/EL	6/X2 Y1	34,291	Mute	Mute	Mute
3/EG	11/X3 Y1	34,638	Analog Output 1-Up	Color Up	—
4/EK	16/X4 Y1	34,984	Normalize	Normalize	Normalize
5/EF	21/X5 Y1	35,330	analog Output 1-Down	Color Down	—
6/EI	22/X5 Y2	35,677	Z1	—	—
7/AF	23/X5 Y3	36,023	Analog Output 2-Up	Brightness Up	Balance Left
8/AI	26/X6 Y1	36,370	Z2	—	—
9/BF	27/X6 Y2	36,716	Analog Output 2-Down	Brightness Down	Balance Right
10/BI	2/X1 Y2	37,062	Z3	—	—
11/CF	3/X1 Y3	37,409	Analog Output 3-Up	Volume Up	Volume Up
12/CI	4/X1 Y4	37,755	Z4	—	—
13/DF	5/X1 Y5	38,101	Analog Output 3-Down	Volume Down	Volume Down
14/DI	7/X2 Y2	38,448	Z5	—	—
15/AG	8/X2 Y3	38,794	F1	Program 1	Scan
16/AK	9/X2 Y4	39,141	F2	Program 2	Search AM/FM
17/BG	10/X2 Y5	39,487	F3	Program 3	Search Stereo
18/BK	12/X3 Y2	39,833	F4	Program 4	Station #1
19/CG	13/X3 Y3	40,180	F5	Program 5	Station #2
20/CK	14/X3 Y4	40,526	F6	Program 6	Station #3
21/DG	15/X3 Y5	40,872	F7	Program 7	Station #4
22/DK	17/X4 Y2	41,219	F8	Program 8	Station #5
23/AH	18/X4 Y3	41,565	F9	Program 9	Program
24/AL	19/X4 Y4	41,912	F10	Program 10	Tune Up
25/BH	20/X4 Y5	42,258	F11	Program 11	Tune Down
26/BL	24/X5 Y4	42,604	F12	Program 12	AM/FM Bandswitch
27/CH	25/X5 Y5	42,951	F13	Program 13	—
28/CL	28/X6 Y3	43,297	F14	Program 14	—
29/DH	29/X6 Y4	43,643	F15	Program 15	—
30/DL	30/X6 Y5	43,990	F16	Program 16	—

23 Channel Remote Control Transmitters

FEATURES

- Ultrasonic or Infrared transmission
- 23 Direct channels of information
- Direct drive for 40kHz transducer
- Power consumption only during keying of information.
- AY-5-8410 — local control at receiver
  AY-5-8411 — remote control operates on 9V battery
- Keyboard bounce protection built in.
- No external oscillator is required.
- Local transmitter wire-OR'ed to receiver

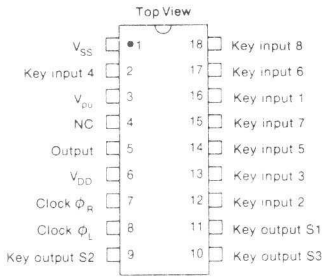
DESCRIPTION

The AY-5-8410/8411 transmitter provides the electronics to transmit 23 channels of information. The transmission is in pulse code modulated form suitable for either ultrasonic or infrared transmission. The transmitter will drive a 40kHz transducer either directly or via a step-up transformer. When any key is depressed, battery power is applied to the chip; power is removed at the end of the code sequence following the release of the key. The requirement for a separate on/off switch is avoided. The keyboard is an 8 × 3 matrix as shown on the next page. Key bounce protection is incorporated. A stable on-chip oscillator is also provided.

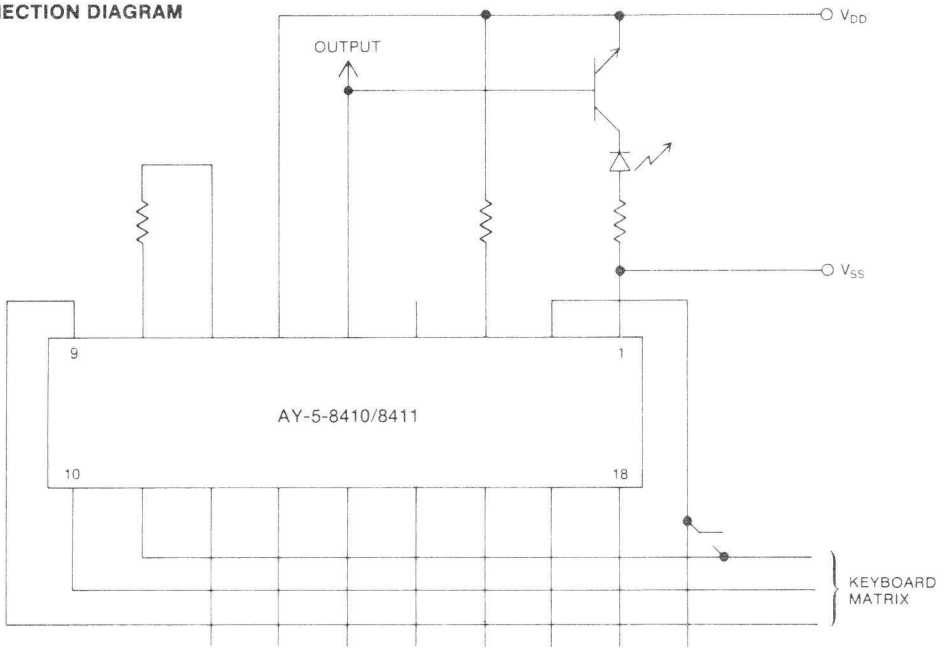
If a local keyboard is required, an additional transmitter chip can be used to encode the local keyboard and the chip output can be wire-OR'ed with the output from the receive transducer amplifier before being fed to the receiver chip.

PIN CONFIGURATION

18 LEAD DUAL IN LINE



CONNECTION DIAGRAM



PIN FUNCTIONS

Key Lines S1, S2, S3

These key lines form part of the key matrix as shown above and are strobe signals which each go to logic '0' in sequence.

Key Inputs K1-K8

Those key lines form part of the key matrix as shown above and they are connected to strobe lines S1, S2 or S3 when appropriate keys are depressed.

Ultrasonic Output

The ultrasonic output is a three state push pull output which goes to logic 1 between trains of pulse in a data block.

A transducer or step up transformer can be connected between the ultrasonic output and V_{DD}.

ϕR and ϕL

These are the oscillator input pins. The chip frequency is not critical except in so far as is necessary to satisfy the requirements of the ultrasonic transducers.

The chip may be driven from an external clock by connecting the clock to both ϕR and ϕL linked together.

V_{SS}

0V or positive supply.

V_{DD}

Negative supply (nominally 9 volts for the AY-5-8411).

V_{pu}

This pin is concerned with automatic circuit start up and should be connected to V_{DD} by a 2.2 Meg resistor.

TRANSMITTER KEY MATRIX

Key Strobe / Input Line	S 2	S 3	S 1
1	Ch 24	16	16
2	9	17	25
3	10	18	26
4	11	19	27
5	12	20	28
6	13	21	29
7	14	22	30
8	15	23	31

NOTE:
Channels are the codes that are output by the AY-5-8420 receiver.

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage Temperature range ..... -65°C to +150°C
Ambient Operating Temperature range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at the conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted

V_{SS} = 0V
V_{DD} = -9V Nominal (AY-5-8411)
-15V Nominal (AY-5-8410)
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min.	Typ*	Max.	Units	Conditions
Inputs					
Clocks, Key lines 1-8					
Logic 0	+0.3	—	-1	Volts	
Logic 1	-3	—	V_{DD}	Volts	
Outputs					
Strobes S1, S2, S3	—	2.5	—	kΩ	Output at -7V
Ultrasonic output	—	100	—	Ω	
Supply Current:					
Standby Mode	—	6	—	μA	
Transmitting Mode	—	2	—	mA	Chip alone

*Typical values are at +25°C and nominal voltages.

31-63 Channel Remote Control Receiver

FEATURES

- Ultrasonic or Infrared reception.
- Up to 31 or 63 channels of information
- On board oscillator — external oscillator optional
- Automatic power on clear
- Local control from wire-OR of transmitter
- Error detection is contained
- Output provided to show information being received

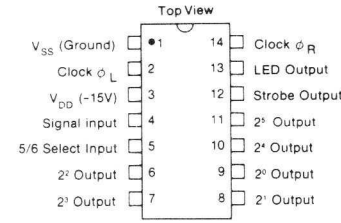
DESCRIPTION

The AY-5-8420 provides the electronics to produce an ultrasonic or infrared remote control receiver which, with an appropriate transmitter, can accept up to 63 channels of information. An on chip oscillator is provided, the frequency of which is non critical (≈66kHz). The oscillator frequency is set by one external resistor; an external oscillator can be used if required. Two outputs are provided to indicate that data has been received and is ready for use. Automatic internal power-on-clear is provided.

Error checking bits are transmitted with the code, these are interrogated by the receiver and prevent it from accepting incorrect data caused by attenuation, reflection or multiple path propagation effects. If the first received block of data is not accepted due to introduced errors, the receiver logic resets and attempts to accept the next block. Data blocks are repeatedly transmitted whenever the transmitter is keyed.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



PIN FUNCTIONS

V_{SS}
0 Volts or positive supply.

V_{DD}
Negative supply (15V nominal).

Clock inputs ϕR, ϕL

The clock frequency is determined by the value of a resistor connected between ϕR and L.

ϕR and ϕL may be connected together and overdriven by an external clock input.

Signal Input

The input should be driven from an amplifier output stage. The receiver is insensitive to input frequency except in so far as is necessary to satisfy the requirements of the transducers.

A local keyboard input can be wire-OR'ed. The frequency is set to approximately 66kHz with a single resistor.

5/6 Select Input

This pin alters the function of the receiver to enable it to accept data from either a 5 bit (31 channel) or 6 bit (63 channel) transmitter. With the pin not connected the receiver functions in the 5 bit mode. With the pin connected to V_{SS} the receiver functions in 6 bit mode.

Outputs 2^0, 2^1, 2^2, 2^3, 2^4, 2^5

The six outputs are latching outputs which retain the data until it is replaced by new input data. The outputs are open ended and clamp to 0 Volts with no output data present.

The output codes change state midway through the end code following correct reception of a data block.

Power-on-clear sets the outputs to an all ones state when power is first applied.

LED

This signal can be used to drive an indicator to show that new data has been received.

The LED output is normally at 0 Volts and goes open circuit simultaneous with the outputs changing. The signal remains in this state during the time that the transmitter is keyed and the receiver is receiving input signals. The signal goes to 0 volts 32ms after the input signals cease.

By gating the LED output with a discrete decode of the outputs 1,2,4,8,16,32 a signal is obtained to drive an analog function i.e. volume up. Such a signal would be present only during the time that the transmitter was keyed.

Strobe

The strobe output is open ended and clamps to 0 Volts.

The clamp is released 60 sec after the data on outputs 1,2,4,8,16,32 has changed and is re-applied 60μsec later.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -15V nominal
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min.	Typ*	Max	Units	Conditions
Inputs					
Clock, Signal, 5/6 Select:					
Logic 0	+0.3	—	-1	Volts	
Logic 1	-3	—	V_{DD}	Volts	
Outputs					
A-F, LED, STROBE:					
Logic 0 sink current	—	2	—	mA	2V drop
Oscillator frequency	—	66	—	kHz	

*Typical values are at +25°C and nominal voltages.

ENTER-TAINMENT

30 Channel Remote Control Transmitter

FEATURES

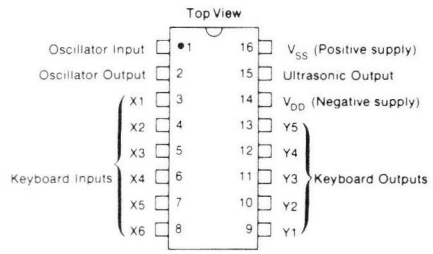
- 30 channels 346.4Hz spacing in the range 34-44kHz.
- P-channel 9V battery operation.
- 4.4336MHz TV crystal master oscillator.
- 5 × 6 matrix keyboard input.
- Low standby current drain (10μA max.).
- Compatible with SAA1025, SAA1130, AY-5-8460 and AY-5-8461 receivers.

DESCRIPTION

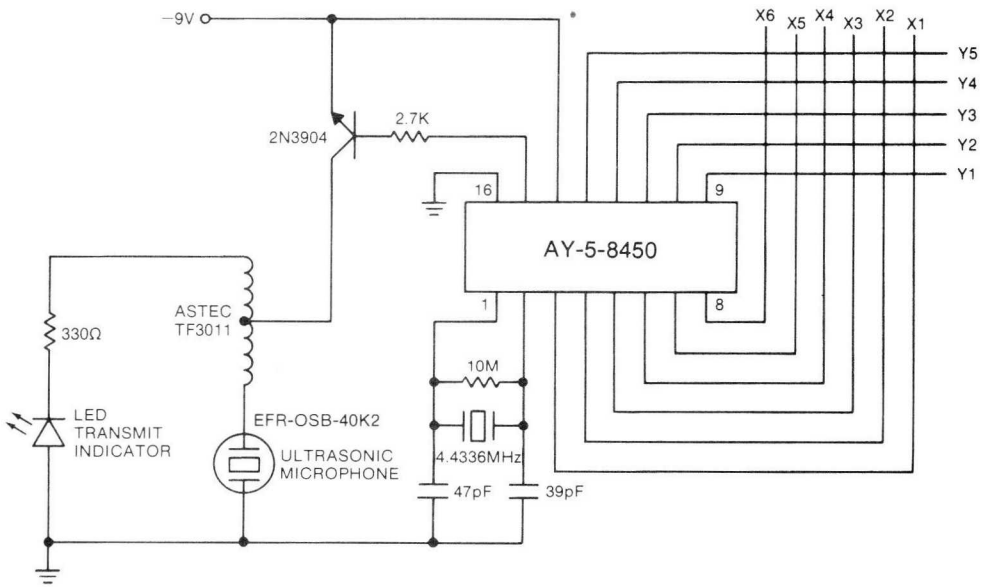
The AY-5-8450 allows the transmission of 30 commands using 30 different ultrasonic frequencies in the range 33.945 to 43.990kHz. It is designed for battery operation and uses a low cost TV crystal as the master oscillator. When inactive the circuit is in a standby mode having a current drain of less than 10μA. As soon as a key is depressed the main circuit is powered up and transmission commences.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



SYSTEM DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1.	Oscillator Input	The Quartz crystal network is connected to these pins.
2.	Oscillator Output	
3.	X1	The keys are in the form of an XY matrix. As soon as a key closure is detected the chip is powered up and the keyboard is scanned at 3kHz. When it has been determined what key has been pressed the appropriate frequency is transmitted. If more than one key is pressed the chip ceases to transmit.
4.	X2	
5.	X3	
6.	X4	
7.	X5	
8.	X6	
	Keyboard Inputs	
9.	Y1	
10.	Y2	
11.	Y3	
12.	Y4	
13.	Y5	
	Keyboard Outputs	
14.	V_{DD}	Negative supply (-9V nom)
15.	Ultrasonic output	Off until key pressed
16.	V_{SS}	Positive supply (ground)

OUTPUT FREQUENCIES

Crystal = 4.4336 MHz

Key	Matrix	Frequency (Hz)
1	X1 Y1	33944.89
2	X1 Y2	37062.28
3	X1 Y3	37408.66
4	X1 Y4	37755.03
5	X1 Y5	38101.41
6	X2 Y1	34291.21
7	X2 Y2	38447.97
8	X2 Y3	38794.16
9	X2 Y4	39140.54
10	X2 Y5	39486.92

Key	Matrix	Frequency (Hz)
11	X3 Y1	34637.65
12	X3 Y2	39833.29
13	X3 Y3	40179.67
14	X3 Y4	40526.05
15	X3 Y5	40872.42
16	X4 Y1	34984.02
17	X4 Y2	41218.80
18	X4 Y3	41565.18
19	X4 Y4	41911.55
20	X4 Y5	42257.93

Key	Matrix	Frequency (Hz)
21	X5 Y1	35330.40
22	X5 Y2	35676.78
23	X5 Y3	36023.15
24	X5 Y4	42604.31
25	X5 Y5	42950.68
26	X6 Y1	36369.53
27	X6 Y2	36715.91
28	X6 Y3	43297.06
29	X6 Y4	43643.43
30	X6 Y5	43989.81

NOTE: The full key configuration/frequencies abqve are compatible with 30 channel receivers such as the GI SAA 1025. For operation with 16 channel receivers, such as the GI AY-5-8460/8461, only keyboard inputs X1 to X4 and keyboard outputs Y2 to Y5 are required.

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -12 Volts
Output current 10mA
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... -10°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = 0V
V_{DD} = -7 to -10V
T_A = −10°C to 70°C

Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Frequency	—	4.4336	—	MHz	See the Connection Diagram for external components
Key Contact Resistance:					
ON	—	—	100	Ω	
OFF	1	—	—	MΩ	
Key Capacitance	—	—	20	pF	
Output:					
On Resistance	—	—	600	Ω	To V_{SS}, V_{OUT} = -1V
Off Resistance	—	—	3	kΩ	To V_{DD}, V_{OUT} = V_{DD} +0.5V
Standby Current Drain	—	5	10	μA	
Operating Current Drain	—	12	—	mA	

16 Channel Remote Control Receivers

FEATURES

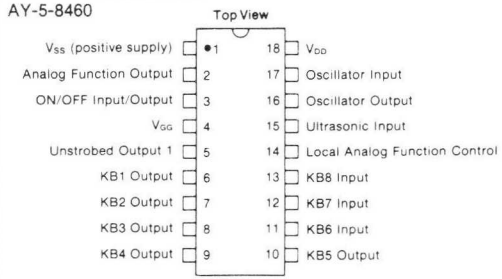
- 16 channels including 12 strobed (KB outputs), an on/off signal, and for the AY-5-8460, one unstrobed output and 2 signals (up/down) for control of an analog function; for the AY-5-8461, three unstrobed outputs.
- The 12 strobed outputs are in a 3×5 matrix format for direct parallel connection to a local keyboard.
- On-chip oscillator using a 4.4336 MHz TV crystal.
- Compatible with AY-5-8450 or SAA1024 transmitters.

PIN CONFIGURATIONS

18 LEAD DUAL IN LINE

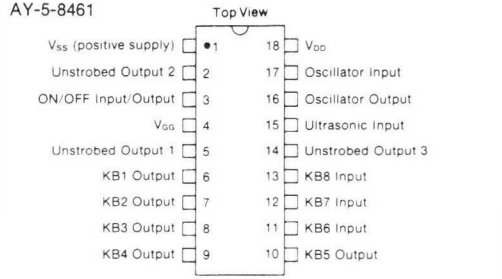
AY-5-8460

Top View



AY-5-8461

Top View



DESCRIPTION

The AY-5-8460/8461 is a 16 channel ultrasonic remote control receiver designed to be compatible with the GI Omega TV and Stereomega Hi-Fi digital tuning systems, or any system which requires the use of a local keyboard in parallel with a remote control receiver. 12 of the received signals are output in a 1 of 5 code on lines KB1-5 upon application of the corresponding strobe on input lines KB6-8. This operation simulates the function of a mechanical 3×5 matrix keyboard. Additionally for other requirements, an on/off control and one (AY-5-8460) or three (AY-5-8461) unstrobed outputs are provided. The AY-5-8460 also recognizes two analog function controls to vary the mark/space ratio of an analog function output.

Either the AY-5-8460 or 8461 can be operated by the AY-5-8450 or SAA1024 remote control transmitters.

SYSTEM DIAGRAM

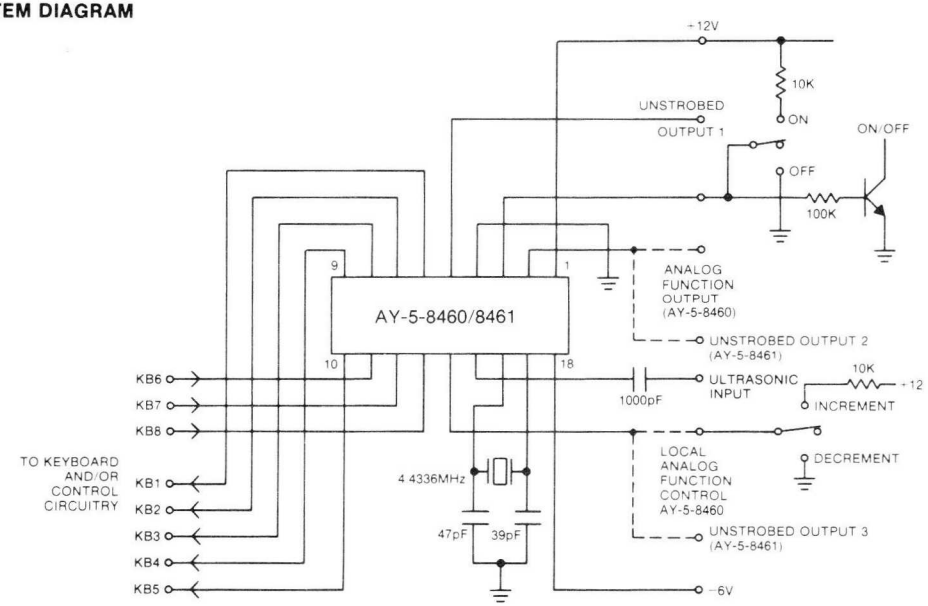


Table 1 FREQUENCY ALLOCATIONS

Frequency Hz	Output Code
37,062	KB1/KB6
37,409	Unstrobed Output
37,755	On/Off Output
38,101	KB4/KB8
38,448	KB2/KB6
38,794	KB3/KB6
39,141	KB4/KB6
38,487	KB5/KB8
39,833	KB5/KB6
40,180	KB1/KB7
40,526	KB2/KB7
40,872	Analog Function Down (AY-5-8460) or Unstrobed Output 2 (AY-5-8461)
41,219	KB3/KB7
41,565	KB4/KB7
41,912	KB5/KB7
42,258	Analog Function Up (AY-5-8460) or Unstrobed Output 3 (AY-5-8461)

PIN FUNCTIONS

Pin No.	Name	Functions
1	V_{SS}	Positive power supply.
2	Analog Function Output (AY-5-8460)	This output is in the form of a pulse, the mark to space ratio of which can be changed in 125 steps from 1:126 to 126:1, the repetition frequency being 8.73kHz. The mark space ratio is incremented by one step about 115msec. after the start of an ultrasonic command, thereafter it is incremented every 46.2msec. At power ON the output is normalized to a mark space ratio of 63:64. The output is also controlled by pin 14.
2	Unstrobed Output 2 (AY-5-8461)	This output is unstrobed and is at logic '1' for the duration of the corresponding ultrasonic command.
3	ON/OFF Output/Input	This output is toggled ON and OFF by reception of the corresponding ultrasonic command. At power up the output is set to the OFF state. When in the OFF state the Analog Function output is prevented from changing and the KB outputs are at logic '1'. The output may be turned ON by connecting it to V_{SS} via a 10kOhm resistor for 10μs, it may be turned OFF by connecting it to V_{GG}. The Ultrasonic command must be present for at least 0.7 sec. to activate the output.
4	V_{GG}	This pin is externally maintained at $V_{DD}+(6V \pm 5\%)$, to serve as a ground reference for logic signals.
5	Unstrobed Output 1	This output is unstrobed and is at logic '0' for the duration of the corresponding ultrasonic command.
6	KB1 Output	A 3×5 matrix keyboard may be connected to the same pins. Maximum capacitance between intersecting matrix lines is 20pF.
7	KB2 Output	
8	KB3 Output	
9	KB4 Output	
10	KB5 Output	
11	KB6 Input	
12	KB7 Input	
13	KB8 Input	
14	Local Analog Function Control (AY-5-8460)	This is a tristate input which provides local control of the Analog Function Output, pin 2. Connecting this pin to V_{SS} (V_{DD}) via a 10kOhm resistor causes the mark space ratio to increment (decrement). The input must be activated for 23msec. before the Output begins to change. This input has priority over the ultrasonic command for Analog Function Up/Down.
14	Unstrobed Output 3 (AY-5-8461)	This output is unstrobed and is at logic '1' for the duration of the corresponding ultrasonic command.
15	Ultrasonic Input	The ultrasonic signal should be capacitively coupled and be at least 500mV peak to peak. The first incoming pulse triggers a 23.1ms timer and after a delay of this period, two measurements of the ultrasonic signal are made over the following two 23.1ms periods. If the measurements produce a comparison an output is generated after a further pause of 46.2ms. The outputs are present for the duration of the ultrasonic command. During the complete receiving time the period of the ultrasonic signal is measured. If it is less than 18μsec or greater than 36μsec the signal is rejected and the receiver is set back to the start condition and a new measuring cycle commences. The input signals need not be completely accurate for satisfactory reception. At the lowest frequency an error of ±0.51% can be tolerated and at the highest ± 0.39%.
16	Oscillator Output	This is the output of the clock oscillator. One side of the crystal is connected to this pin.
17	Oscillator Input	This is the input of the clock oscillator. The other side of the crystal is connected to this pin.
18	V_{DD}	Negative power supply.

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -20 Volts
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +12V ± 10%
V_{GG} = 0V
$V_{DD} = V_{GG}$ — (6V ± 5%)
T_{amb} = 0°/C to +70°C

Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Oscillator Frequency	—	4.4336	—	MHz	
Ultrasonic Input					
Sensitivity	500	—	25	mVp-p	
Impedance	10	—	—	kΩ	
Inputs KB6-8					
Pull up resistance	—	—	200	kΩ	to V_{SS}
Logic '0'	—	—	V_{SS} -8	Volts	
Logic '1'	V_{SS} -1.5	—	—	Volts	
Analog Function Control Input (AY-5-8460)					
Increment Up	V_{SS}—1	—	V_{SS}	Volts	10K to V_{SS}
Increment Down	V_{GG}	—	V_{GG} +0.5	Volts	Short to V_{GG}
No Movement	—	—	—	—	Open Circuit
ON/OFF Input					
ON	V_{SS} -1	—	V_{SS}	Volts	Load 10K to V_{SS} & 100K to V_{GG}
OFF	V_{GG}	—	V_{GG} +0.5	Volts	Short to V_{GG}
Outputs KB1-5					
Logic '0'	V_{GG}	—	V_{GG} +0.5	Volts	Load 100K to V_{SS}
Logic '1'	V_{SS} -1	—	V_{SS}	Volts	
Unstrobed Outputs					
Logic '0'	V_{GG}	—	V_{GG} +0.5	Volts	Load 100K to V_{SS}
Logic '1'	V_{SS} -1	—	V_{SS}	Volts	
Analog Function Output (AY-5-8460)					
On Level	V_{SS} -1	—	V_{SS}	Volts	Load 68K to V_{GG}
Off Level	V_{GG}	—	V_{GG} +0.5	Volts	
Pulse Frequency	—	8.73	—	kHz	
ON/OFF Output					
Off	V_{GG}	—	V_{GG} +0.5	Volts	Load 100K to V_{GG}
On	V_{SS} -1	—	V_{SS}	Volts	
Supply Current	—	30	40	mA	V_{SS}—V_{DD} = 18V

Table 2
The table below illustrates the use of the AY-5-8460 and AY-5-8461 R/C receivers with either the AY-5-8450 or SAA1024 R/C transmitters for the GI Omega TV and Stereomega Hi-Fi digital tuning systems.

R/C Transmitters		Frequency (Hz)	R/C Receiver	Omega Function	Stereomega Function (Suggested Only)
AY-5-8450 Key/Matrix	SAA1024 Key/Inputs		AY-5-8460/8461 Output		
2/X1 Y2	10/BI	37,062	KB1/KB6	0	—
3/X1 Y3	11/CF	37,409	Unstrobed Output 1	Recall	AM/FM Bandswitch
4/X1 Y4	12/CI	37,755	On/Off Output	On/Off	On/Off
5/X1 Y5	13/DF	38,101	KB4/KB8	Channel Down	Station #5
7/X2 Y2	14/DI	38,448	KB2/KB6	1	—
8/X2 Y3	15/AG	38,794	KB3/KB6	2	Search Stereo
9/X2 Y4	16/AK	39,141	KB4/KB6	3	Search AM/FM
10/X2 Y5	17/BG	39,487	KB5/KB8	Channel Up	Station #4
12/X3 Y2	18/BK	39,833	KB5/KB6	4	Scan
13/X3 Y3	19/CG	40,180	KB1/KB7	5	—
14/X3 Y4	20/CK	40,526	KB2/KB7	6	—
15/X3 Y5	21/DG	40,872	Analog Function Down (AY-5-8460) or Unstrobed Output 2 (AY-5-8461)	Volume Down Fine Tune Down	Volume Down —
17/X4 Y2	22/DK	41,219	KB3/KB7	7	Station #3
18/X4 Y3	23/AH	41,565	KB4/KB7	8	Station #2
19/X4 Y4	24/AL	41,912	KB5/KB7	9	Station #1
20/X4 Y5	25/BH	42,258	Analog Function Up (AY-5-8460) or Unstrobed Output 3 (AY-5-8461)	Volume Up Fine Tune Up	Volume Up —

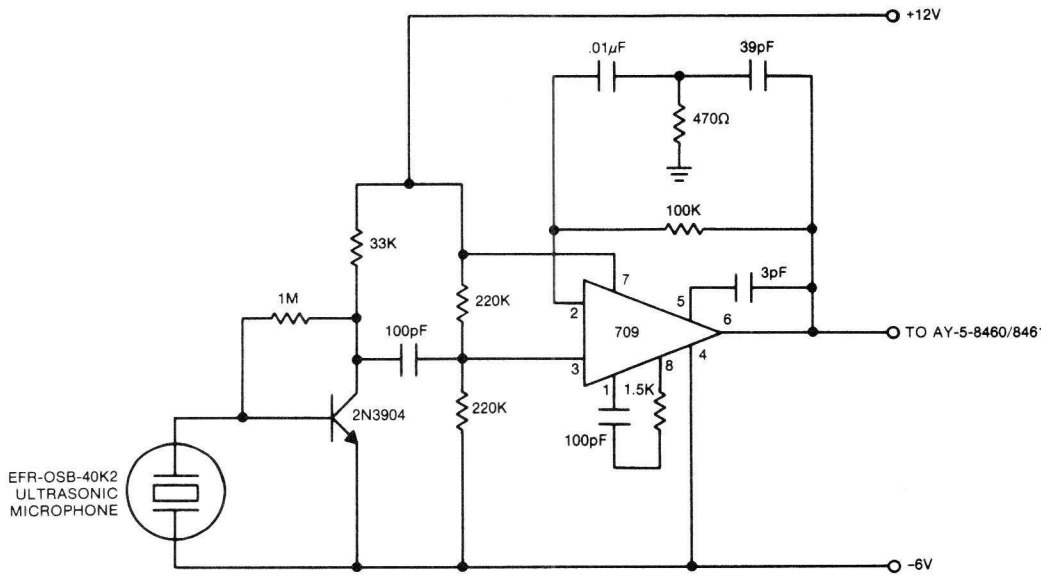


Fig.1 ULTRASONIC PREAMP

ENTER-TAINMENT

264 Command Infrared Remote Control Transmitter

FEATURES

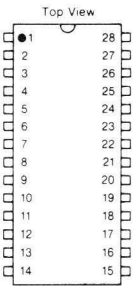
- 256 Digital Commands
- 8 optional analog commands for remote TV games
- 7.5/9V battery operation
- Low standby current (10μA)
- 4×8 keyboard matrix with optional shifts to increase matrix to 32×8

DESCRIPTION

The AY-3-8470 is designed to transmit 256 Digital and 8 Analog commands over an infrared link. For the digital commands, it uses a PCM system with an 8 bit code which is transmitted twice (the second time inverted) to prevent operation by false codes. For the analog commands it uses a pulse width modulation scheme.

PIN CONFIGURATION

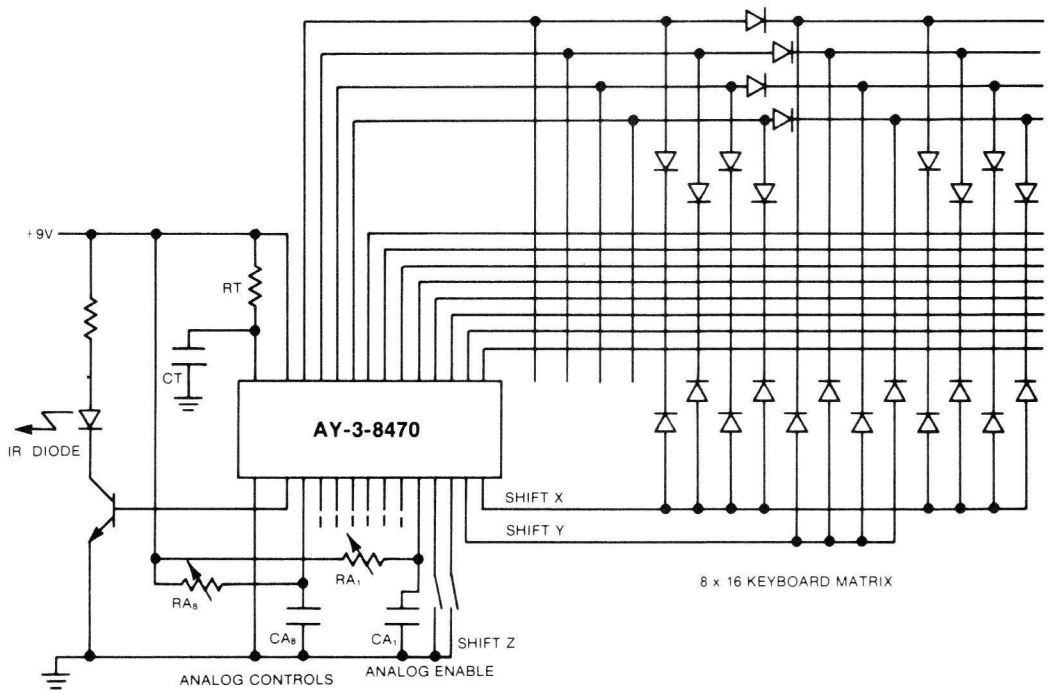
28 LEAD DUAL IN LINE



Not yet defined.

SYSTEM DIAGRAM

IR Transmitter with an 8×16 keyboard, a shift key, and 8 analog channels.



PIN FUNCTIONS

Pin	Function
V_{SS}	Negative supply
V_{DD}	Positive supply
Clock Input	A capacitor connected to V_{SS} and a resistor connected to V_{DD} determine the clock frequency.
Key Input 1 Key Input 2 Key Input 3 Key Input 4	These key lines form part of the key matrix and are connected to strobe lines A to K when the appropriate keys are depressed.
Key Output A Key Output B Key Output C Key Output D Key Output E Key Output F Key Output G Key Output H	These key lines form part of the key matrix and are strobe signals which go to logic '0' in sequence.
Shift Input X Shift Input Y Shift Input Z	These inputs control the first 3 bits of the code and are used to extend the keyboard up to a maximum of 256 commands.
Analog Channel Enable	When this input is connected to V_{DD} the analog channels are enabled and the transmitter operates continuously.
Analog Input 1 Analog Input 2 Analog Input 3 Analog Input 4 Analog Input 5 Analog Input 6 Analog Input 7 Analog Input 8	A capacitor connected to V_{SS} and a variable resistor connected to V_{DD} control the width of the analog command pulses and hence the analog function.

OPERATING NOTES

1. When transmitting a digital command the transmitter remains powered up repeating the command as long as the button is pressed. When the button is released the command is completed before the transmitter reverts to standby.
2. If more than one key is pressed the transmitter will power up but will not output data.
3. When the analog mode is selected the transmitter continuously sends the analog commands.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect of V_{SS} pin ..... −0.3 to +12V
Ambient operating temperature range ..... 0°C to +70°C
Storage temperature range ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +10V
T_A = 0°C to +70°C

Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	—	1.0	2.0	MHz	
Transmission Frequency	—	500	1000	kHz	
Transmission Time	69	138	—	ms	
Duty Cycle (Digital Only)	—	1.0	—	%	
Duty Cycle (Analog & Digital)	—	7.0	13	%	
Key Contact Resistance					
Closed	—	—	100	Ω	
Open	1	—	—	MΩ	
Transmitter Output					
On	—	10	—	mA	V_{OUT} = +1V source
Off	—	10	—	μA	V_{OUT} = 0.5V sink
Standby Current	—	—	10	μA	
Operating Current	—	2	—	mA	

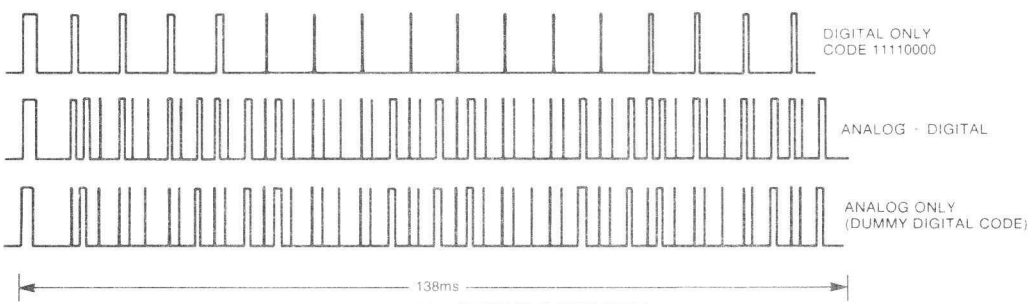


Fig.1 TYPICAL OUTPUT WAVEFORMS

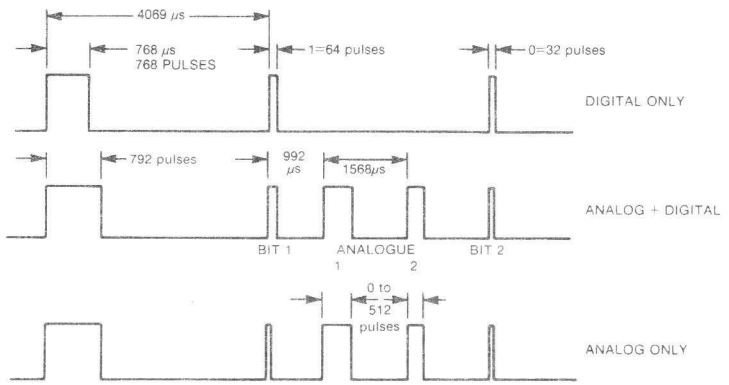


Fig.2 OUTPUT WAVEFORM DETAIL

264 Command Infrared Remote Control Receiver

FEATURES

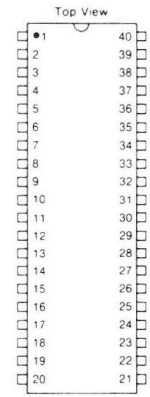
- 256 commands
- 5 bit binary program output (for up to 32 programs)
- Output strobe
- Output enable
- 4 analog channels with 62 steps
- Main power switching output
- Mute facility on volume output
- Normalize command on 3 analog outputs
- 2 auxiliary ON/OFF outputs
- CPU databus interface for 256 digital commands and 8 proportional analog commands

DESCRIPTION

The receiver is a 256 digital and 8 proportional analog command unit capable of interfacing directly to the GI Omega digital tuning systems and the Gimini TV games systems. An infrared transmission link is used to ensure security and accuracy of transmission together with a short response time.

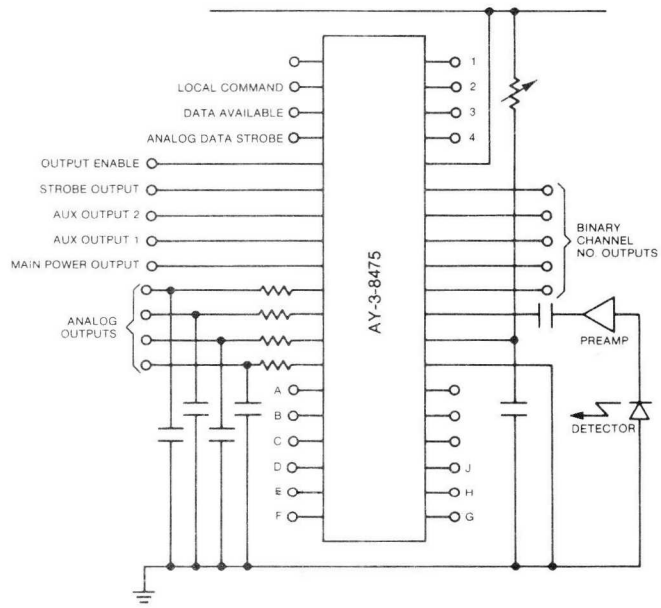
PIN CONFIGURATION

40 LEAD DUAL IN LINE



Not yet defined.

SYSTEM DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin	Function
Output 2^0 Output 2^1 Output 2^2 Output 2^3 Output 2^4	Binary program number outputs. Program 1 = 00000 (positive logic)
Analog Output 1 Analog Output 2 Analog Output 3 Analog Output 4	Open drain pulse width modulated outputs. The mark space ratio is variable from 1:62 to 62:1. When continuous command is received, the outputs increment or decrement once every 102 ms.
Main Power On/Off Output	Open drain transistor which is turned ON by any one of the 32 Program commands and OFF by the Main Power OFF command. If the output is shorted to V_{SS} for at least 9.5μs, it will also be turned on.
Signal Input	Capacitively coupled signal from preamplifier.
Spare Output 1 Spare Output 2	Open drain outputs which can be turned ON and OFF as desired. In addition, Spare 1 can be toggled.
Strobe Output	Strobe output goes to logic '0' as soon as new program data has been received. It remains at logic '1' for the duration of the transmitted signal.
Output Enable	When taken to logic '0', the program Number Outputs 2^0, 2^1, 2^2, 2^3, 2^4, are enabled.
V_{SS}	Ground
V_{CC}	Positive supply (+12V nom.)
Oscillator	An RC network connected to this pin determines the clock frequency and the system response time.
Analog Data Strobe Input	When taken to a logic '1' it gates the 9 outputs A-J on to the external bus. When at logic '0', the outputs A-J are at a high impedance.
Output A/Input A Output B/Input B Output C/Input C Output D/Input D Output E/Input E Output F/ F Output G/ G Output H/ H Output J/ J	Tri-state outputs indicating the value of the data stored in one of the eight internal storage registers. The output is Binary coded with output A being the L.S.B. and output J the M.S.B. Local commands may be entered via Input A-E.
Control Input1 Control Input 2 Control Input 3	Binary control inputs to address any one of eight internal storage registers, i.e. 0-7.
Control Input 4	Selects the output of Digital Commands and resets Data Available.
Local Command Strobe	Enables A-E as inputs for local commands
Data Available	Signals the presence of a new digital command word.

OPERATION

Power Up

All power up the Main Power, Spare 1 and Spare 2 outputs are OFF. The analog outputs are all set to a mark space ratio of 32:31.

The program number store is set to 00000 (program 1).

Normalization

On reception of the Normalize Command the Analog outputs are set to a mark-space ratio of 32:31.

Muting

The volume output is turned OFF when the MUTE command is received. It is turned on again by:

a) A repeat of the Mute Command
b) Reception of any of the Program Commands
c) Switch on of the Main Power Output
d) Reception of either the Volume Up or volume down commands
e) Reception of Normalization command

Transmitter Command	Receiver Function	Transmitter Command	Receiver Function	Transmitter Command	Receiver Function
1	Program 1	19	Color Increase	37	Program 21
2	Program 2	20	Color Decrease	38	Program 22
3	Program 3	21	Brightness Increase	39	Program 23
4	Program 4	22	Brightness Decrease	40	Program 24
5	Program 5	23	Spare Increase	41	Program 25
6	Program 6	24	Spare Decrease	42	Program 26
7	Program 7	25	Normalize	43	Program 27
8	Program 8	26	Mute	44	Program 28
9	Program 9	27	Main Power Off	45	Program 29
10	Program 10	28	Spare 1 On	46	Program 30
11	Program 11	29	Spare 1 Off	47	Program 31
12	Program 12	30	Spare 1 Toggle	48	Program 32
13	Program 13	31	Spare 2 On	49—63	Spare
14	Program 14	32	Spare 2 Off	63	Used to initiate receiver
15	Program 15	33	Program 17	64	Self test sequence
16	Program 16	34	Program 18	65—256	Spare
17	Volume Increase	35	Program 19		
18	Volume Decrease	36	Program 20		

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . −0.3 to +15 volts
Ambient operating temperature range . . . . . 0°C to +70°C
Storage temperature range . . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Function operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{CC} = +12V ± 20%
V_{SS} = 0V

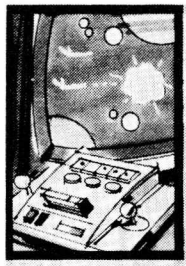
Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	—	2.52	—	MHz	
Command Response time	54	86	230	ms	Note 1
Signal Input Level	1.6	2	—	Vp-p	AC coupled
Signal Input Impedance	—	100	—	kΩ	
Analog Outputs					Gives 6.3 sec.
Increment time/step	82	102	136	ms	Typ. for 62 steps Note 1
Output frequency	—	20	—	kHz	
On Resistance	—	—	600	Ω	
Off Leakage	—	—	10	μA	
Output Enable input					
Logic '0' level	—	—	0.8	Volts	
Logic '1' level	2.4	—	—	Volts	
Leakage	—	—	10	μA	$V_{IN} = V_{CC}$
Digital Outputs					
Logic '0' level	—	—	0.4	Volts	I_{SINK} = 1.6mA
Logic '1' leakage	—	—	10	μA	$V_{OUT} = V_{CC}$
Current consumption	—	20	—	mA	
Main Power Switch Output					
Off leakage	—	—	10	μA	
On resistance	—	—	1	kΩ	

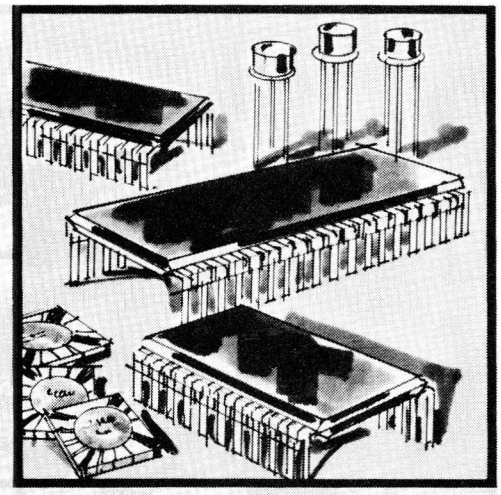
NOTE 1: The command response time is dependent upon the transmitter clock frequency.

ENTER-TAINMENT

TV GAMES 7

Dedicated TV Games 7- 3
Programmable TV Games 7-63





MICRO ELECTRONICS

DEDICATED TV GAMES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500	7-4
		AY-3-8500-1	7-4
BALL & PADDLE (TWO AXIS)	Six selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8550	7-16
		AY-3-8550-1	7-16
COLOR PROCESSOR	Adds color to the AY-3-8500-1 and AY-3-8550-1.	AY-3-8515	7-25
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603	7-26
		AY-3-8603-1	7-26
WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605	7-28
		AY-3-8605-1	7-28
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606	7-32
		AY-3-8606-1	7-32
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607	7-36
		AY-3-8607-1	7-36
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610	7-40
		AY-3-8610-1	7-40
COLOR PROCESSOR	Adds color to the "8600" series dedicated TV Game circuits.	AY-3-8615	7-51
BATTLE	A two player "tank battle" game where each player has a steerable tank and a fire control button.	AY-3-8710	7-52
		AY-3-8700-1	7-52
MOTORCYCLE	A one player game where the player controls the speed of a motorcycle on a three track course.	AY-3-8760	7-56

Ball & Paddle

FEATURES

- Full **COLOR** operation with AY-3-8515.
- 6 Selectable Games—Tennis, soccer, squash, practice and two rifle shooting games
- 625 Line (AY-3-8500) and 525 Line (AY-3-8500-1) versions
- Automatic Scoring
- Score display on T.V. Screen, 0 to 15
- Selectable Bat Size
- Selectable Rebound Angles
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Action Sounds
- Shooting Forwards in Soccer Game
- Visually defined area for all Ball Games.

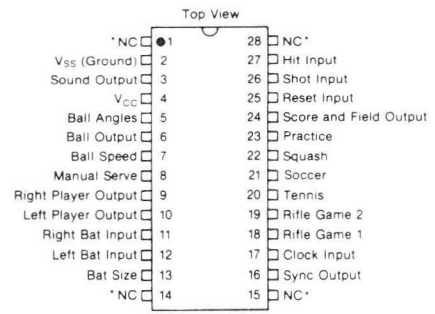
DESCRIPTION

The AY-3-8500 and AY-3-8500-1 circuits have been designed to provide a TV 'games' function which gives active entertainment using a standard domestic television receiver.

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

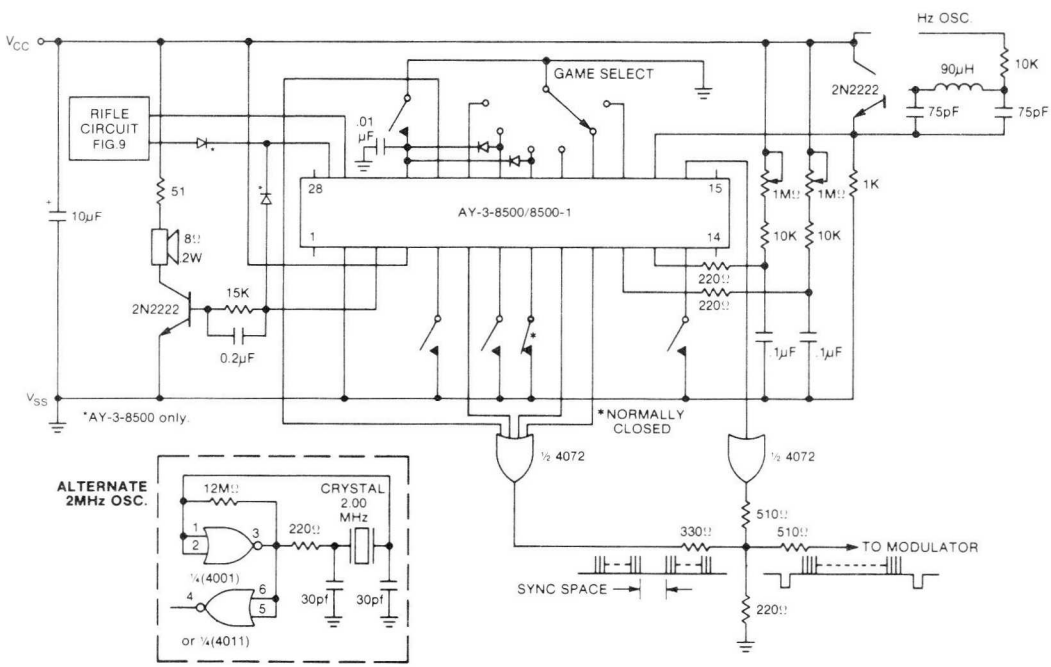
PIN CONFIGURATION

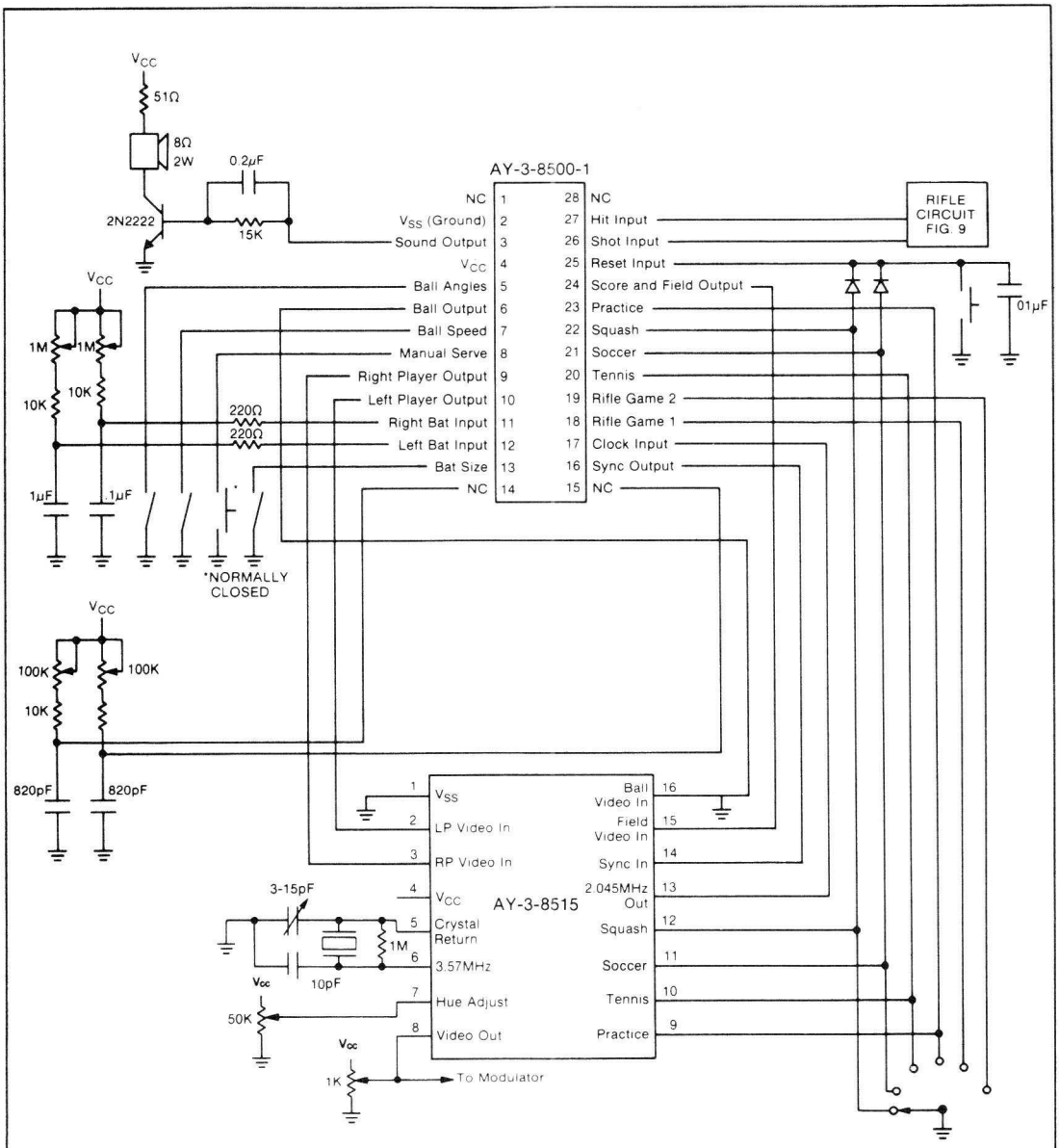
28 LEAD DUAL IN LINE



*Do not use as tie point.

SYSTEM DIAGRAM 1: BLACK AND WHITE IMPLEMENTATION





SYSTEM DIAGRAM 2: AY-3-8500-1 FULL COLOR IMPLEMENTATION USING AY-3-8515 COLOR CONVERTER CIRCUIT

TV GAMES

PIN FUNCTIONS (Pin numbers in parentheses)

Vss (2)
Negative supply input, nominally 0V(GND).

Sound Output (3)
The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (32ms pulse/1.95KHz tone) sounds are output on this pin.

Vcc (4)
Positive supply input.

Ball Angles (5)
This input is left open circuit (Logic '1') to select two rebound angles and connected to Vss (Logic '0') to select four rebound angles. When two angles are selected they are ± 20°, when four are selected they are ±20° and ±40°. See Fig. 11.

Ball Output (6)
The ball video signal is output on this pin.

Ball Speed (7)
When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to Vss (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Manual Serve (8)
This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting this input to V_{SS}.

Right Player Output/Left Player Output (9,10)
The video signals for the right and left players are output on separate pins.

Right Bat Input/Left Bat Input (11,12)
An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot.

Bat Size (13)
This input is left open circuit (Logic '1') to select large bats and connected to V_{SS} (Logic '0') to select small bats. For a 19" T.V. screen, large bats are 1.9" and small bats are 0.95" high.

Sync Output (16)
The T.V. vertical and horizontal sync signals are output on this pin. See Fig. 1.

Clock Input (17)
The 2MHz master timing clock is input to this pin. The exact frequency is 2.012160 ± 1%.

Rifle Game 1, Rifle Game 2, Tennis, Soccer, Squash, Practice (18 thru 23)
These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game.

Score and Field Output (24)
The score and field video signal is output on this pin.

Reset (25)
This input is connected momentarily to Vss (Logic '0') to reset the score counters and start a new game. Normally left open circuit.

Shot Input (26)
This input is driven by a positive pulse output of a monostable to indicate a "shot".

Hit Input (27)
This input is driven by a positive pulse output of a monostable which is triggered by the shot input if the target is on the sights of the rifle.

NOTE: The "Shot" and "Hit" inputs have on-chip pull-down resistors to Vss. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to Vcc.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

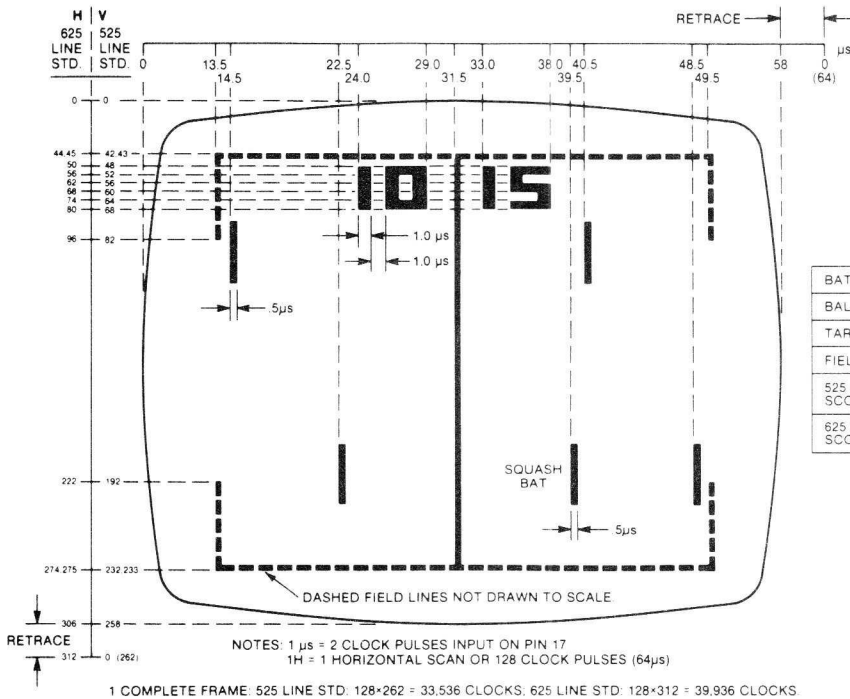
Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +12V
Storage Temperature Range ..... -20° C to +70° C
Ambient Operating Temperature Range ..... 0° C to +40° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V
Operating Temperature (T_A) = 0° C to +40° C

Characteristics at 25° C and Vcc = +6 Volts	Min	Typ	Max	Units	Conditions
Clock Input					Maximum clock source impedance
Frequency	1.99	2.01	2.03	MHz	of 1K to V_{CC} or V_{SS}.
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Pulse Width — Pos.	—	200	—	ns	
Pulse Width — Neg.	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = 0V, F = 1MHz
Leakage	—	100	—	μA	
Control Inputs					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Input Impedance	—	1.0	—	MΩ	Pull up to V_{CC}
Rifle Input	—	1.0	—	MΩ	Pull down to V_{SS}
Outputs					
Logic '0'	—	—	1.0	Volt	Iout = 0.5mA
Logic '1'	V_{CC}-2	—	—	Volts	Iout = 0.1mA
Power Supply Current	—	40	60	mA	at V_{CC} = +7V



	H	V
BAT	0.5μs	14/28 lines
BALL	1.0μs	5 lines
TARGET	2.5μs	14 lines
FIELD	0.5μs	2 lines
525 LINE SCORE	5.0μs	20 lines
625 LINE SCORE	5.0μs	30 lines

Fig.1 LOCATION OF DATA OUTPUT PULSES

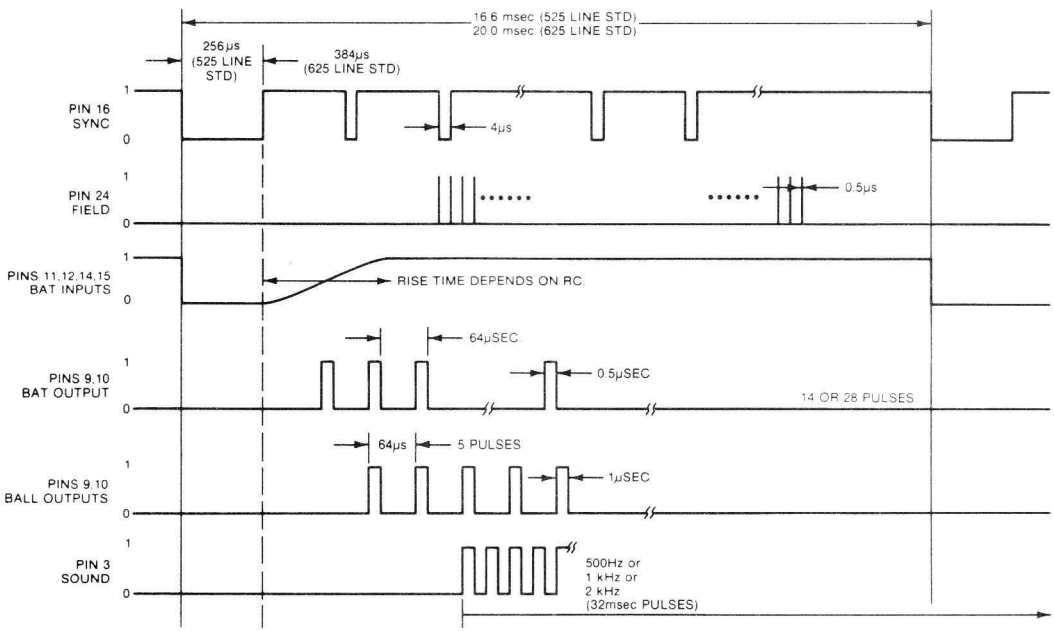


Fig.2 TIMING DIAGRAM

TV GAMES

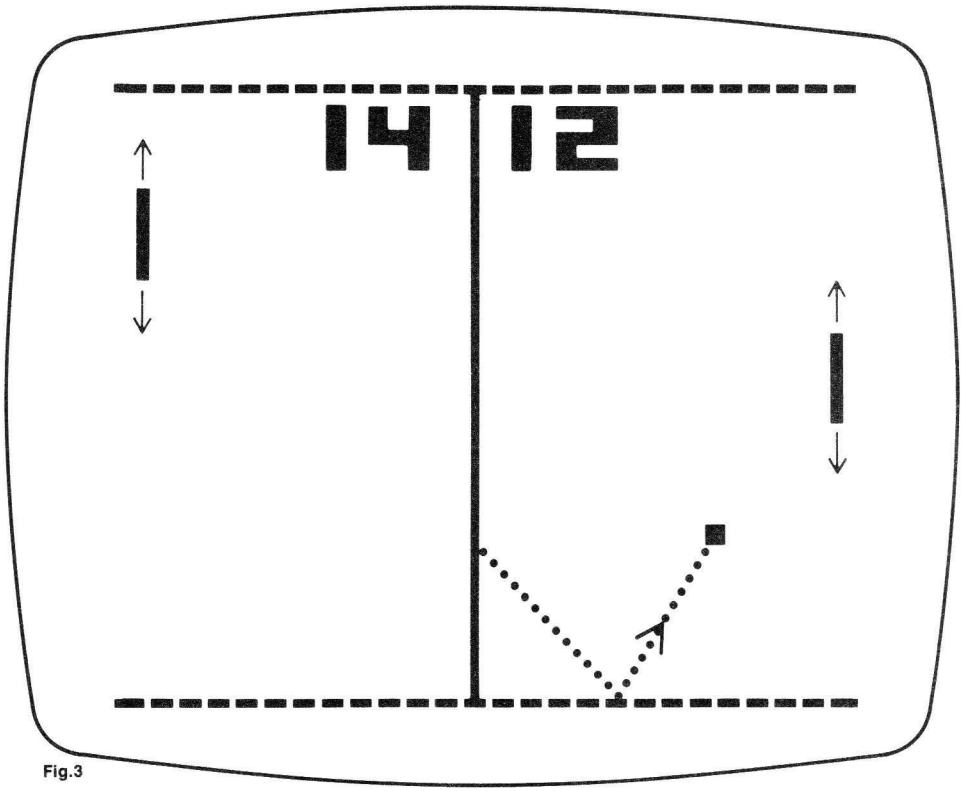


Fig.3

Tennis

With the tennis game the picture on the television screen would be similar to Figure 3 with one 'bat' per side, a top and bottom boundary and a center net. The individual scores are counted and displayed automatically in the position shown. The detail of the game will depend upon the selection of the options. Considering the situation where small bats are used and all angles, after the reset has been applied, the scores will be 0, 0 and the ball will serve arbitrarily to one side at one of the angles. If the ball hits the top or bottom boundary it will assume the angle of reflection and continue in play. The player being served must control his bat to intersect the path of the ball. When a 'hit' is detected by the logic, the section of the bat which made the hit is used to determine the new angle of the ball.

To expand on this, all 'bats' or 'players' are divided logically into four adjacent sections of equal length. When using the four angle option it is the quarter of bat which actually hits which defines the new direction for the ball.

The direction does not depend upon the previous angle of incidence. With the two angle option the top and bottom pairs of the bats are summed together and only the two shallower angles are used to program the new direction for the ball.

The ball will then traverse towards the other player, reflecting from the top or bottom as necessary until the other player makes his 'hit'. This action is repeated until one player misses the ball. The circuitry then detects a 'score' and automatically increments the correct score counter and updates the score display. The ball will then serve automatically towards the side which has just missed. This sequence is repeated until a score of 15 is reached by one side, whereupon the game is stopped. The ball will still bounce around but no further 'hits' or 'scores' can be made. While the game is in progress, three audio tones are output by the circuit to indicate top and bottom reflections, bat hits and scores.

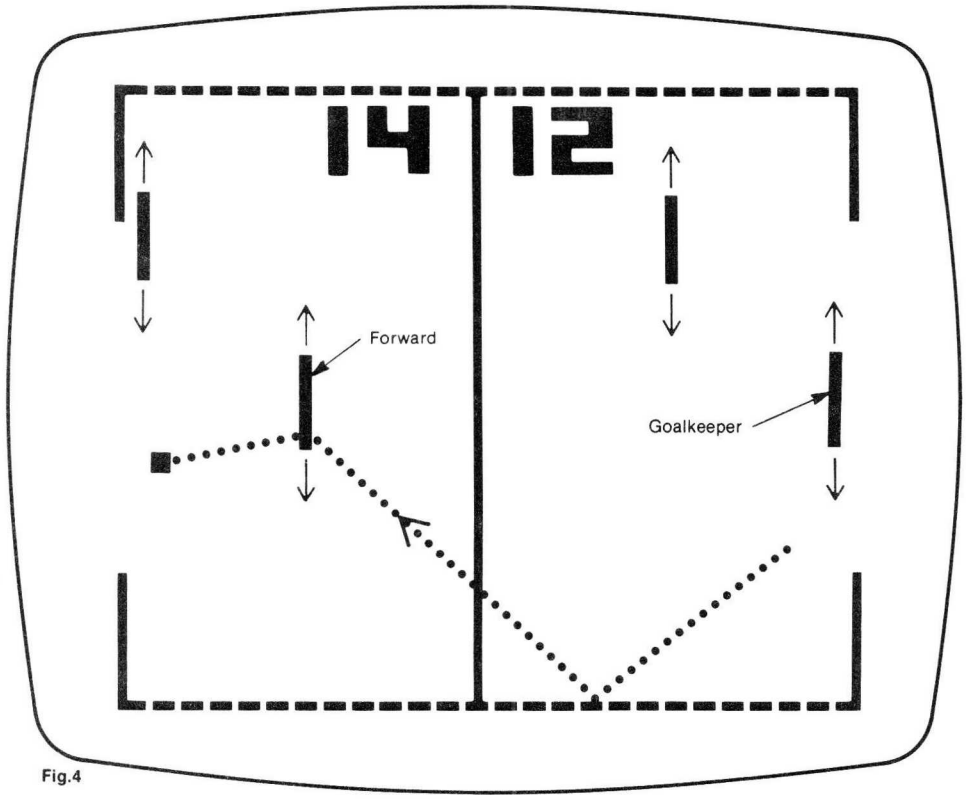


Fig.4

Soccer

The "soccer" type game is shown in Figure 4. With this game each participant has a 'goalkeeper' and a 'forward'. The layout is such that the 'goalkeeper' is in his normal position and the 'forward' is positioned in the opponent's half of the playing area.

When the game starts, the ball will appear travelling from one goal line towards the other side. If the opponent's forward can intercept the ball, (Figure 4a), he can 'shoot' it back towards the goal. If the ball is missed it will travel to the other half of the playing area and the first team's forward will have the opportunity of intercepting the ball and redirecting it forward at a new angle according to the 'player' section which is used (Figure 4b). If the ball is 'saved' by the 'goalkeeper' or it reflects back from the end boundary, the same forward will have the opportunity to intercept the outcoming ball and divert it back towards the 'goal'.

A 'score' is made in the "soccer" game by 'shooting' the ball through the defined goal area. The scoring and game control is done automatically as for the tennis game. The same audio signals are used to add atmosphere to the game.

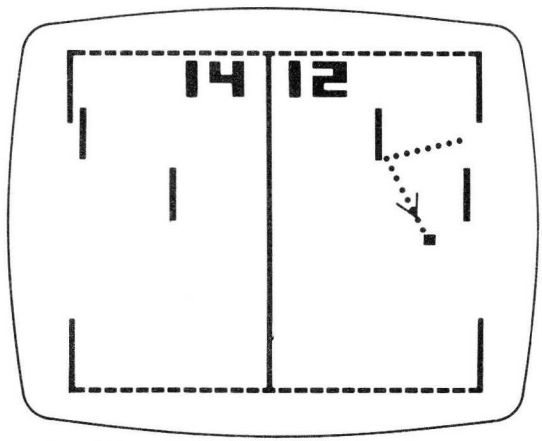


Fig.4a Return of "Goal Save"

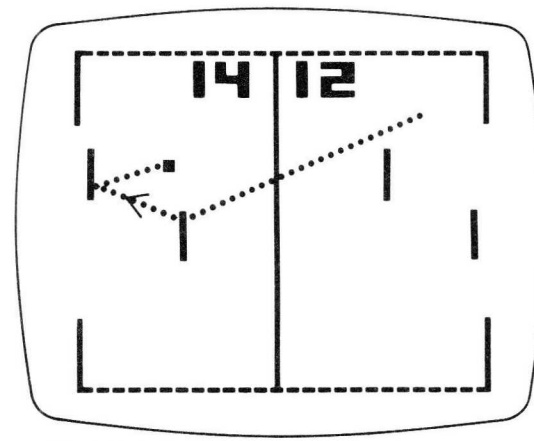


Fig.4b "Shooting" Forward

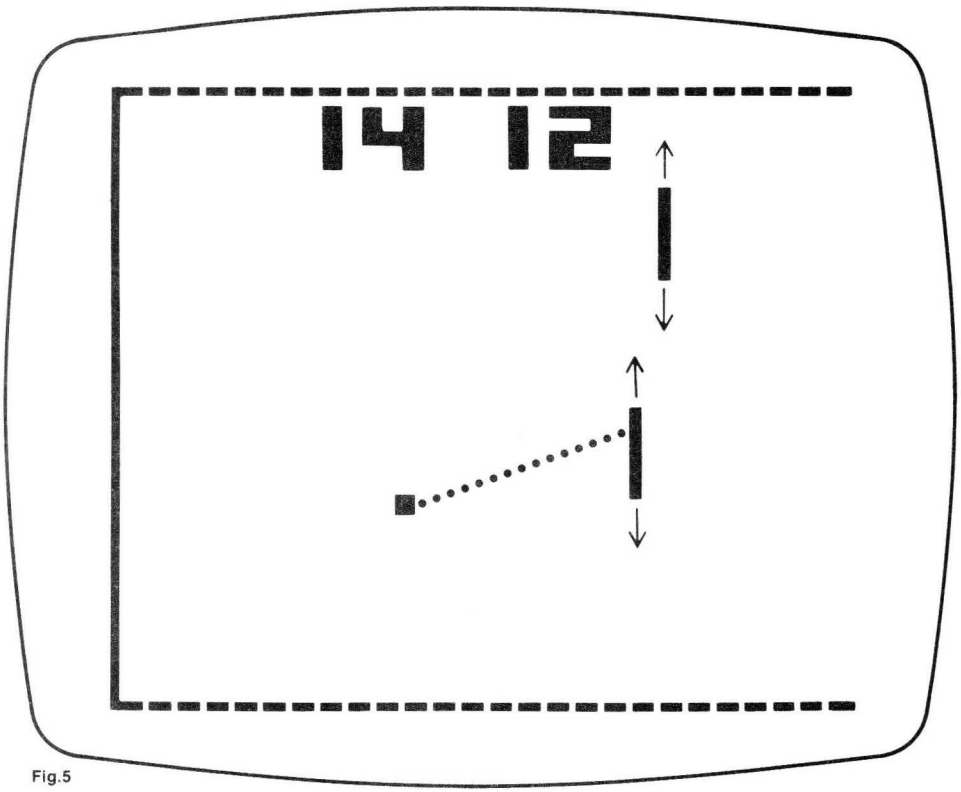


Fig.5

Squash

This game is illustrated in Fig. 5. There are two players who alternately hit the ball into the court. The right hand player is the one that hits first; it is then the left hand player's turn. Each player is enabled alternately to ensure that the proper sequence of play is followed.

Practice

This game is similar to squash except that there is only one player. See Fig. 6.

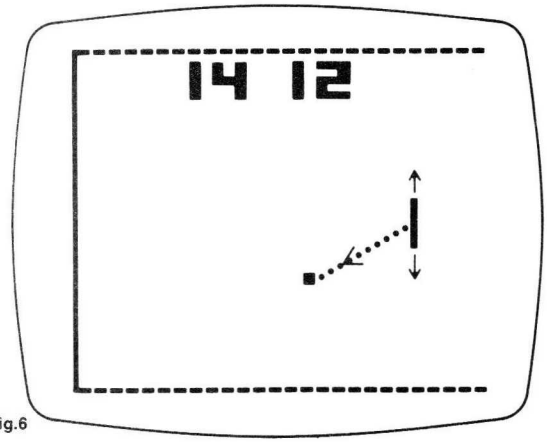


Fig.6

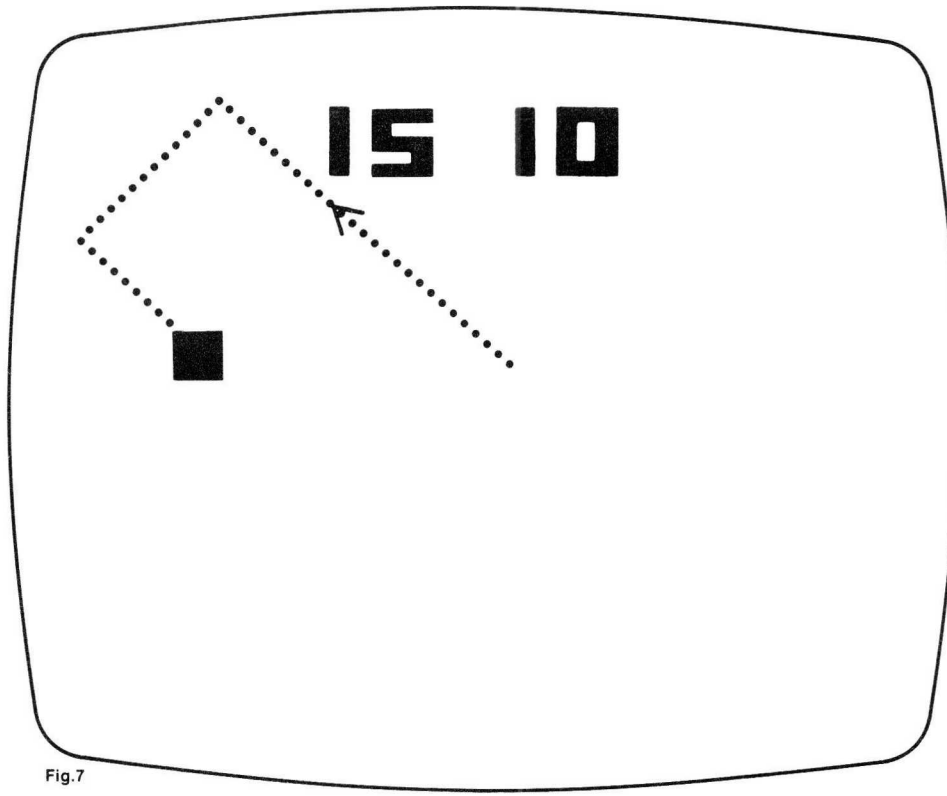


Fig.7

Rifle Game No. 1

This game is illustrated in Fig. 7. It has a large target which bounces randomly about the screen. A photocell in the rifle is aimed at the target. When the trigger is pulled, the shot counter is incremented and, if the rifle is on target, the hit counter is incremented, a hit noise is generated and the target is blanked for a short period. After 15 shots the score appears but the game can still continue without additional scoring.

Rifle Game No. 2

In this game illustrated in Fig. 8, the ball traverses the screen from left to right under control of the manual serve button. Otherwise the game is as described for Rifle Game No. 1.

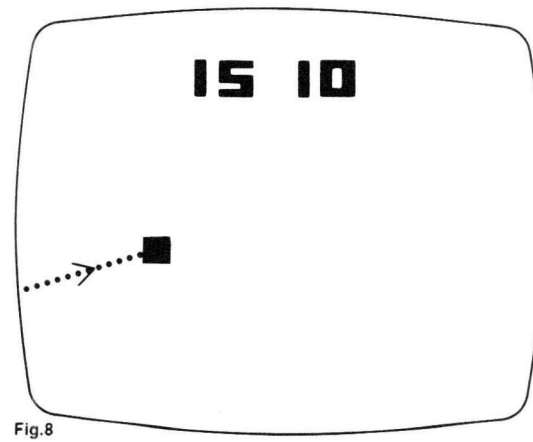


Fig.8

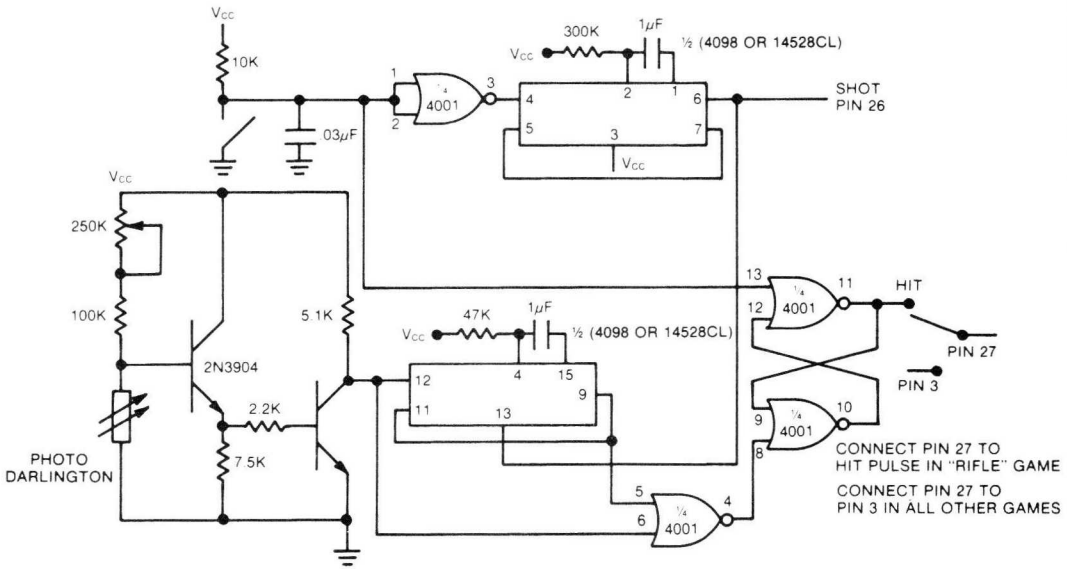


Fig.9 RIFLE INTERFACE

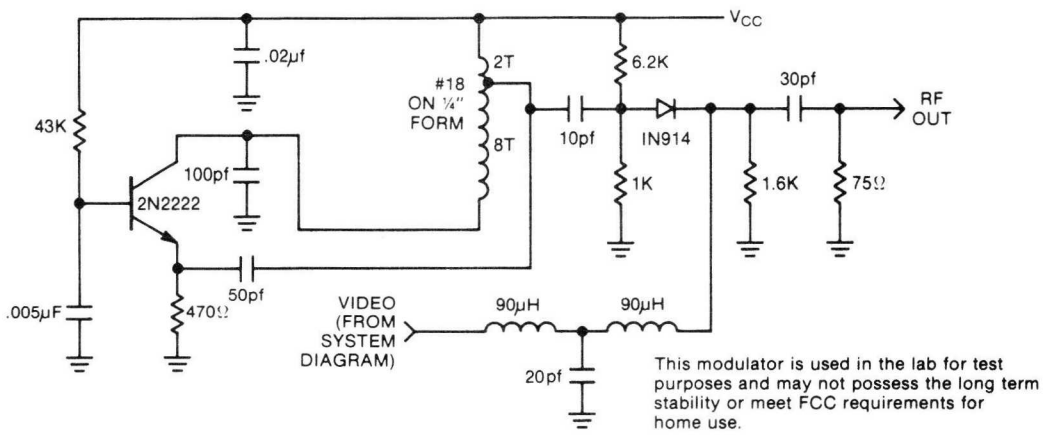


Fig.10 VHF MODULATOR

	Horizontal	Vertical
Slow	± .5μs	2 angles ± 1 line 4 angles ± 3 lines
Fast	± 1μs	2 angles ± 2 lines 4 angles ± 5 lines

Fig.11 ANGULAR MOTION

RANDOM BALL SPEED/RANDOM ANGLES

To enhance the excitement and challenge of the various games, this option provides random variations of the ball speed and random changes in the ball rebound angle as the games are being played.

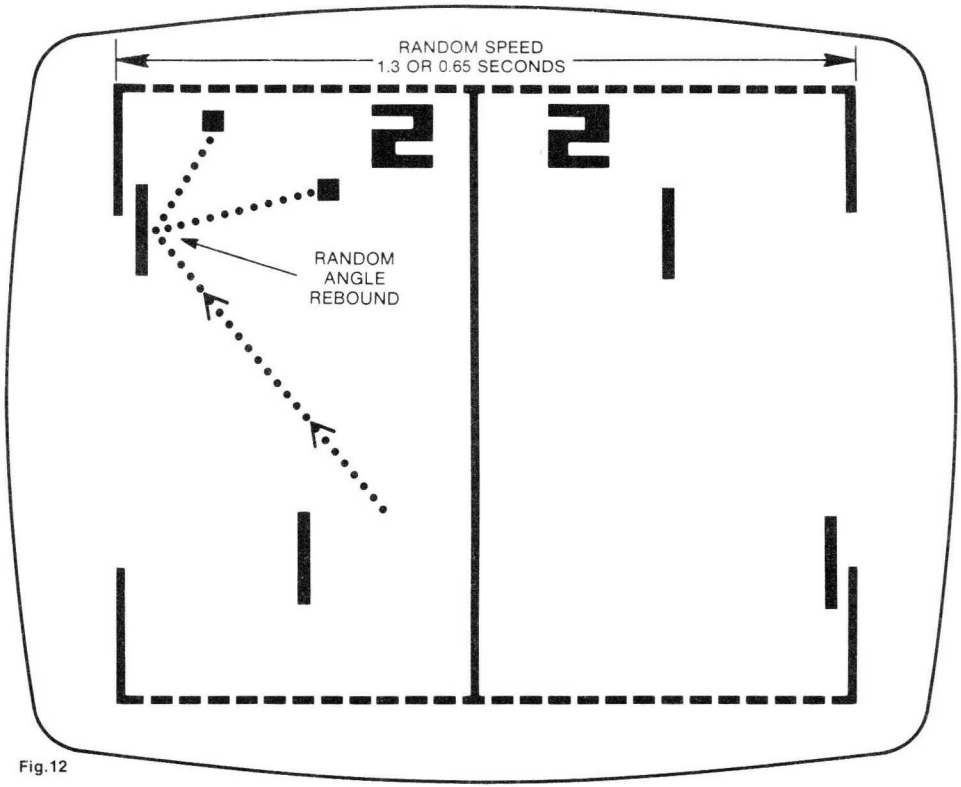


Fig.12

Soccer

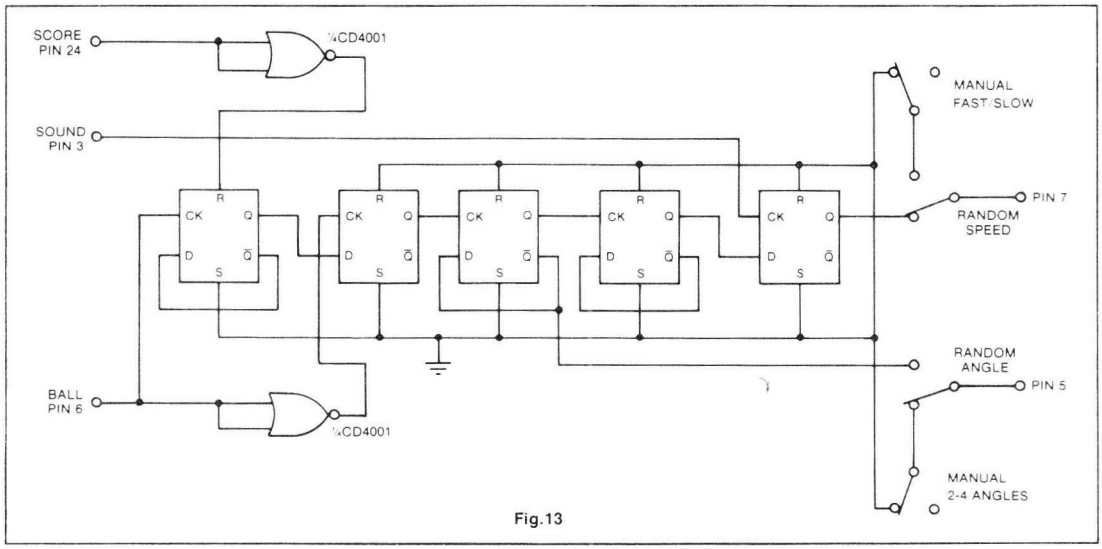


Fig.13

BLACK AND WHITE BATS/GRAY BACKGROUND

This option provides an added factor for player team recognition. The field or court is produced as a gray background with the bats in black and white. This option is particularly helpful for the squash game where the players are positioned close together.

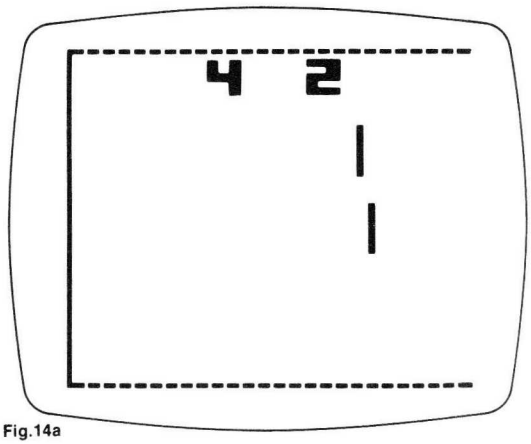


Fig.14a

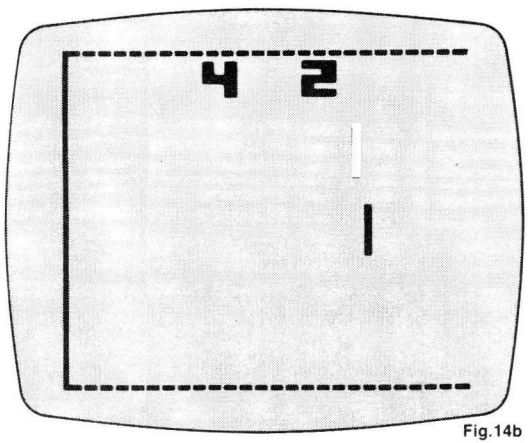


Fig.14b

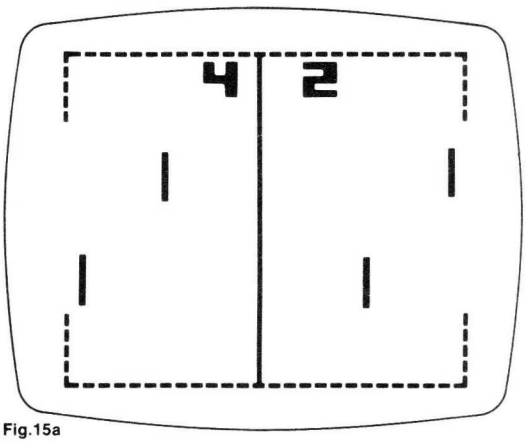


Fig.15a

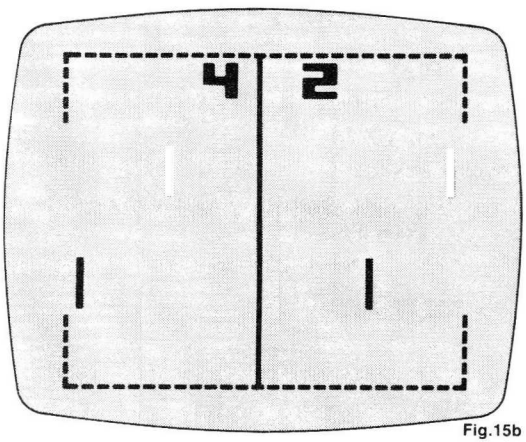
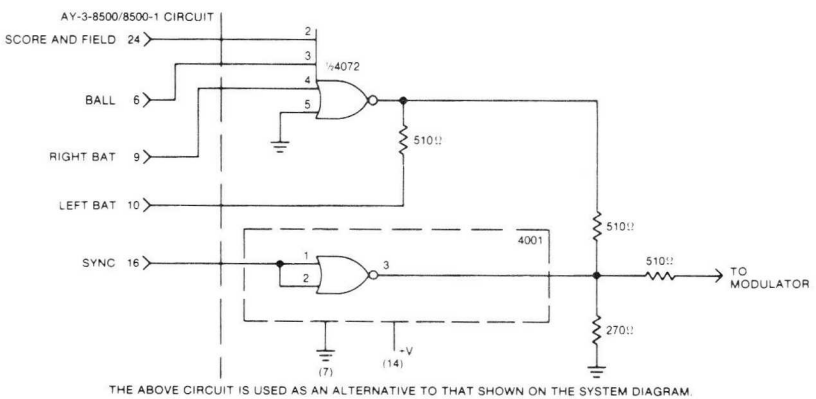


Fig.15b



THE ABOVE CIRCUIT IS USED AS AN ALTERNATIVE TO THAT SHOWN ON THE SYSTEM DIAGRAM.

Fig.16 GRAY BACKGROUND

FOUR PLAYER CONFIGURATION

With this option, the basic two player tennis game can be expanded to true four player doubles. Each player is capable of playing the full width of the court.

A variation of this option allows for a three player handicap game with two players against one.

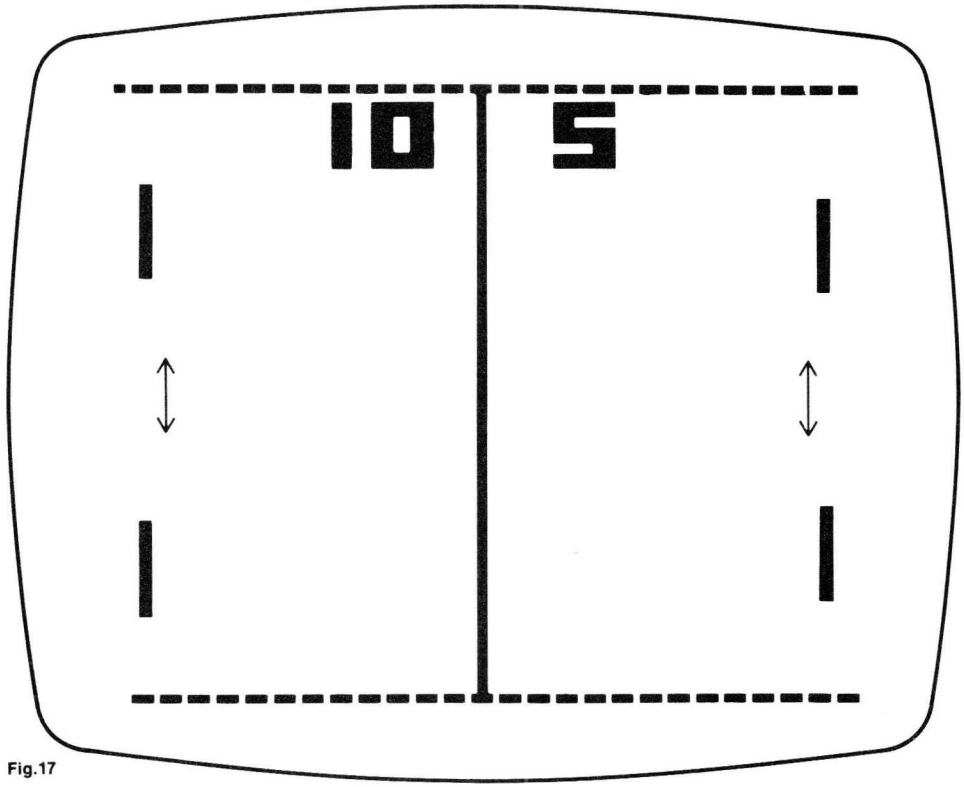


Fig.17

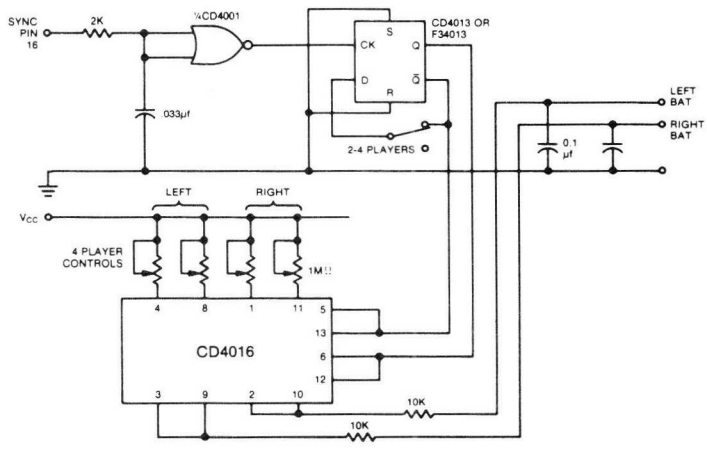


Fig.18

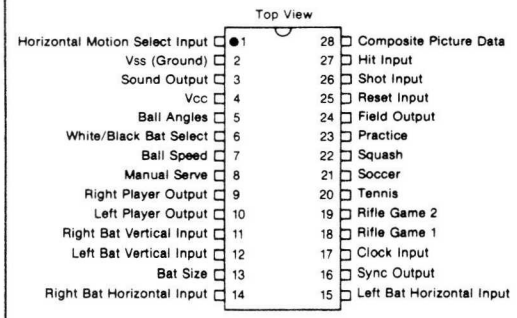
Ball & Paddle (Two Axis)

FEATURES

- Full **COLOR** Operation with AY-3-8515.
- 6 Selectable Games—Tennis, soccer, squash, practice and two rifle shooting games
- 625 Line (AY-3-8550) and 525 Line (AY-3-8550-1) versions
- Selectable horizontal motion
- Special Composite outputs for color coding, players and score, ball and boundaries
- Automatic Scoring
- Score display on T.V. Screen, 0 to 15
- Selectable Bat Size
- Selectable Rebound Angles
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Action Sounds
- Shooting Forwards in Soccer Game
- Visually defined area for all Ball Games
- Score color-coded to player
- Ball output coded to player in Squash
- Practice game scores both hits and misses
- Composite picture data on one pin, and individual video signals for color
- Pin compatible with AY-3-8500/8500-1.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

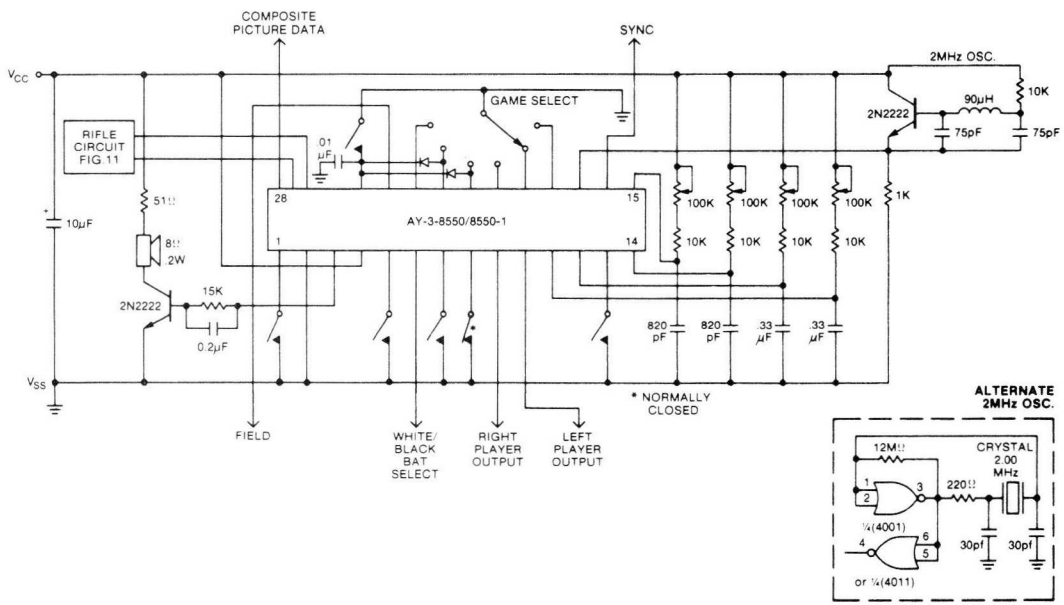


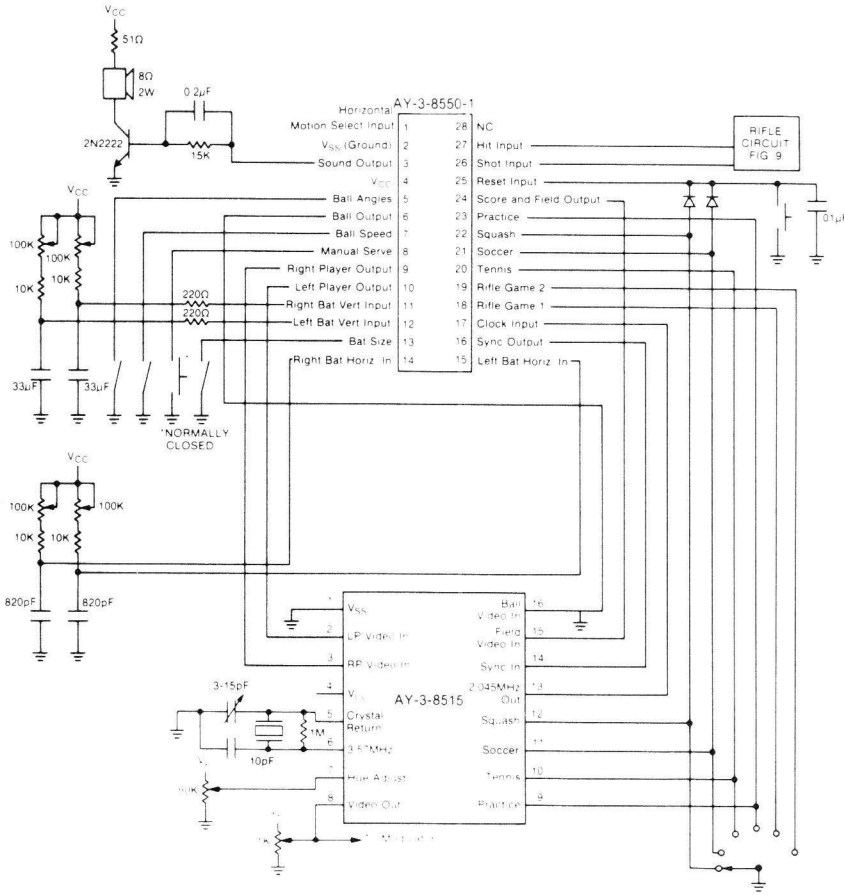
DESCRIPTION

The AY-3-8550 and AY-3-8550-1 circuits have been designed to provide a TV 'games' function which gives active entertainment using a standard domestic television receiver.

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

SYSTEM DIAGRAM 1: BLACK AND WHITE IMPLEMENTATION





SYSTEM DIAGRAM 2: AY-3-8550-1 FULL COLOR IMPLEMENTATION USING AY-3-8515 COLOR CONVERTER CIRCUIT

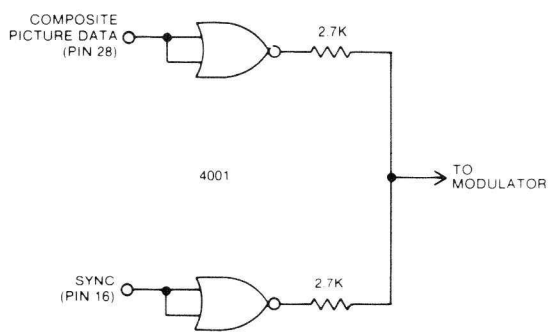


Fig.1 BLACK AND WHITE IMPLEMENTATION USING COMPOSITE PICTURE DATA SIGNAL (White Bats)

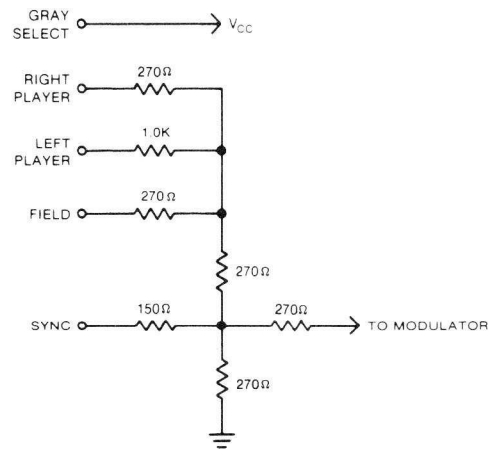


Fig.2 BLACK AND WHITE IMPLEMENTATION USING INDIVIDUAL PLAYER SIGNALS (Black and White Bats/Gray Background)

PIN FUNCTIONS

Horizontal Motion Select (1) When connected to V_{SS} (Logic '0'), the horizontal motion controls are enabled. Open circuit fixes paddles at baselines for vertical motion only.

Vss (2) Negative supply input, nominally 0V(GND).

Sound Output (3) The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (32ms pulse/1.95KHz tone) sounds are output on this pin.

Vcc (4) Positive supply input.

Ball Angles (5) This input is left open circuit (Logic '1') to select two rebound angles and connected to V_{SS} (Logic '0') to select four rebound angles. When two angles are selected they are $\pm$ 20°, when four are selected they are $\pm$ 20° and $\pm$ 40°. See Fig. 13.

White/Black Bat Select (6) Connection to Vcc (Logic '1') inverts the right player output for black right player. This input is pulled to Vss so this circuit may be used in AY-3-8500/8500-1 sockets.

Ball Speed (7) When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to V_{SS} (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Manual Serve (8) This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting the input to V_{SS}.

Right Player Output/Left Player Output (9,10) Normally positive going video signals representing the right hand player (paddle, score, and when playing Squash, the ball when it is the right hand player's turn to hit) and the left hand player (paddle, score, and ball — except that in Squash the ball is output only when it is the left hand player's turn to hit). When connected to V_{CC}, the output is negative going with the "off" state at V_{CC}.

Right bat Vertical Input/Left Bat Vertical Input (11,12) An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot.

Bat Size (13) This input is left open circuit (Logic '1') to select large bats and connected to V_{SS} (Logic '0') to select small bats. For a 19" T.V. screen, large bats are 1.9" and small bats are 0.95" high.

Right Bat Horizontal Input/Left Bat Horizontal Input (14,15) An R-C network connected to each of these inputs controls the horizontal position of the bats. Use a 10K resistor in series with each pot.

Sync Output (16) The T.V. vertical and horizontal sync signals are output on this pin. Sync must always be one of the signals included in the composite video to the modulator. See Fig. 3.

Clock Input (17) The 2MHz master timing clock is input to this pin. The exact frequency is 2.012160 $\pm$ 1%.

Rifle Game 1, Rifle Game 2. Tennis, Soccer, Squash, Practice (18 thru 23) These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game.

Field Output (24) The field video signal is output on this pin.

Reset (25) This input is connected momentarily to V_{SS} (Logic '0') to reset the score counters and start a new game. Normally left open circuit.

Shot Input (26) This input is driven by a positive pulse output by a monostable to indicate a "shot".

Hit Input (27) This input is driven by a positive pulse output of a monostable which is triggered by the shot input if the target is on the sights of the rifle.

Composite Picture Data (28) This positive going output is the sum of the picture data for the bats, ball, field and score and can be used in lieu of the data on pins 9, 10 and 24. This signal and Sync are the only signals required for black and white operation (see Fig. 1).

NOTE: The "Shot" and "Hit" inputs have on-chip pull-down resistors to V_{SS}. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to V_{CC}.

ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

Maximum Ratings*

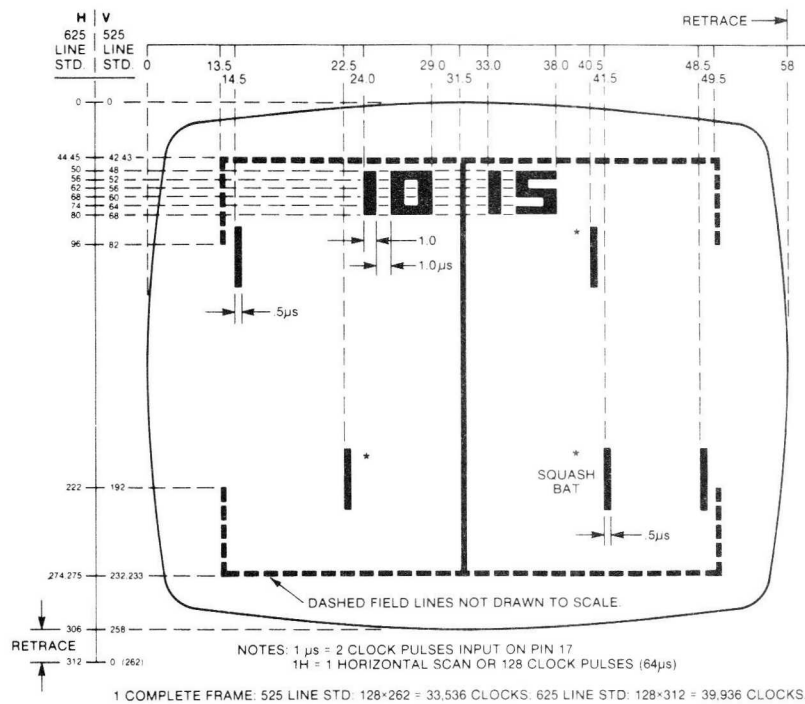
Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +12V
Storage Temperature Range ..... -20° C to +70° C
Ambient Operating Temperature Range ..... 0° C to +40° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V
Operating Temperature (T_A) = 0° C to +40° C

Characteristics at 25° C and Vcc = +6 Volts	Min	Typ	Max	Units	Conditions
Clock Input					Maximum clock source impedance
Frequency	1.99	2.01	2.03	MHz	of 1K to V_{CC} or V_{SS}.
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Pulse Width — Pos.	—	200	—	ns	
Pulse Width — Neg.	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = 0V, F = 1MHz
Leakage	—	100	—	μA	
Control Inputs					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Input Impedance	—	1.0	—	MΩ	Pull up to V_{CC}
Rifle Input	—	1.0	—	MΩ	Pull down to V_{SS}
Outputs					
Logic '0'	—	—	1.0	Volt	Iout = 0.5mA
Logic '1'	V_{CC}-2	—	—	Volts	Iout = 0.1mA
Power Supply Current	—	40	60	mA	at V_{CC} = +7V



	H	V
BAT	0.5μs	14/28 lines
BALL	1.0μs	5 lines
TARGET	2.5μs	14 lines
FIELD	0.5μs	2 lines
525 LINE SCORE	5.0μs	20 lines
625 LINE SCORE	5.0μs	30 lines

*Positions as shown when horizontal motion is not selected.

Fig.3 LOCATION OF DATA OUTPUT PULSES

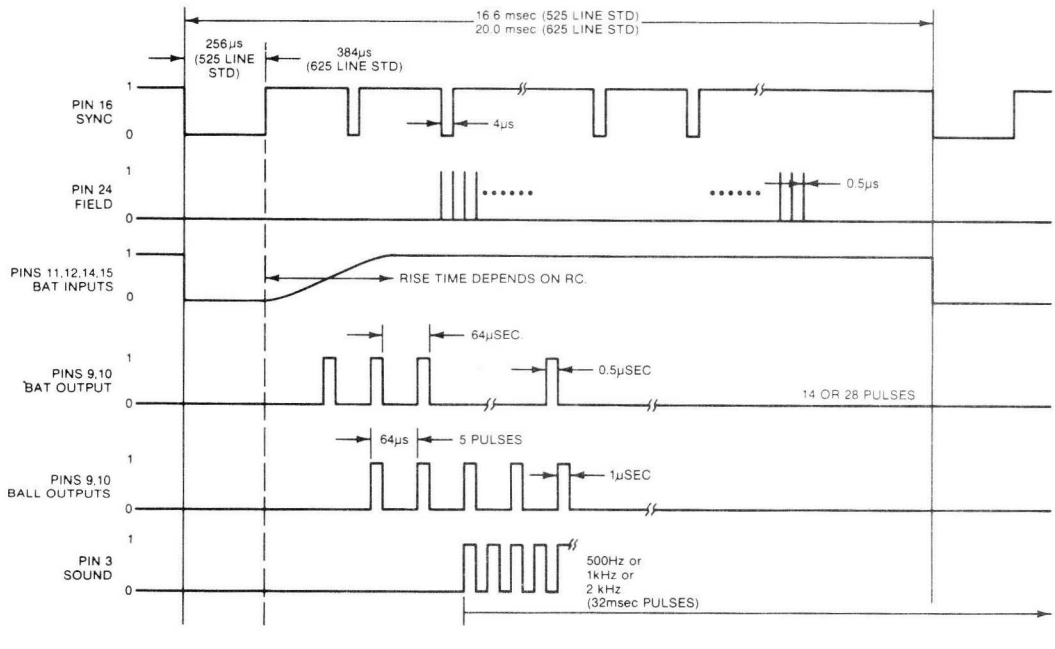


Fig.4 TIMING DIAGRAM

TV GAMES

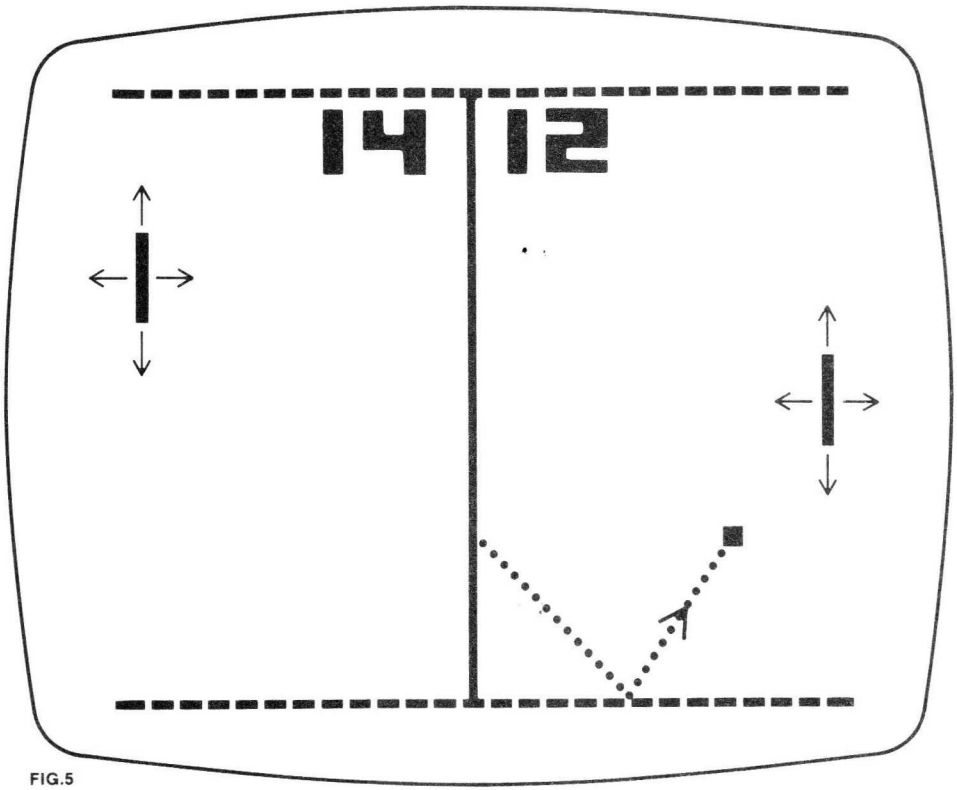


FIG.5

Tennis

With the tennis the picture on the television screen would be similar to Figure 5 with one 'bat' per side, a top and botton boundary and a center net. The individual scores are counted and displayed automatically in the position shown. The detail of the game will depend upon the selection of the options. Considering the situation where small bats are used and all angles, after the reset has been applied, the scores will be 0, 0 and the ball will serve arbitrarily to one side at one of the angles. If the ball hits the top or bottom boundary it will assume the angle of reflection and continue in play. The player being served must control his bat to intersect the path of the ball. When a 'hit' is detected by the logic, the section of the bat which made the hit is used to determine the new angle of the ball.

To expand on this, all 'bats' or 'players' are divided logically into four adjacent sections of equal length. When using the four angle option it is the quarter of bat which actually hits which defines the new direction for the ball.

The direction does not depend upon the previous angle of incidence. With the two angle option the top and bottom pairs of the bats are summed together and only the two shallower angles are used to program the new direction for the ball.

When horizontal motion is selected, the players are restricted to the proper side of the net.

The ball will then traverse towards the other player, reflecting from the top or bottom as necessary until the other player makes his 'hit'. This action is repeated until one player misses the ball. The circuitry then detects a 'score' and automatically increments the correct score counter and updates the score display. The ball will then serve automatically towards the side which has just missed. This sequence is repeated until a score of 15 is reached by one side, whereupon the game is stopped. The ball will still bounce around but no further 'hits' or 'scores' can be made. While the game is in progress, three audio tones are output by the circuit to indicate top and bottom reflections, bat hits and scores.

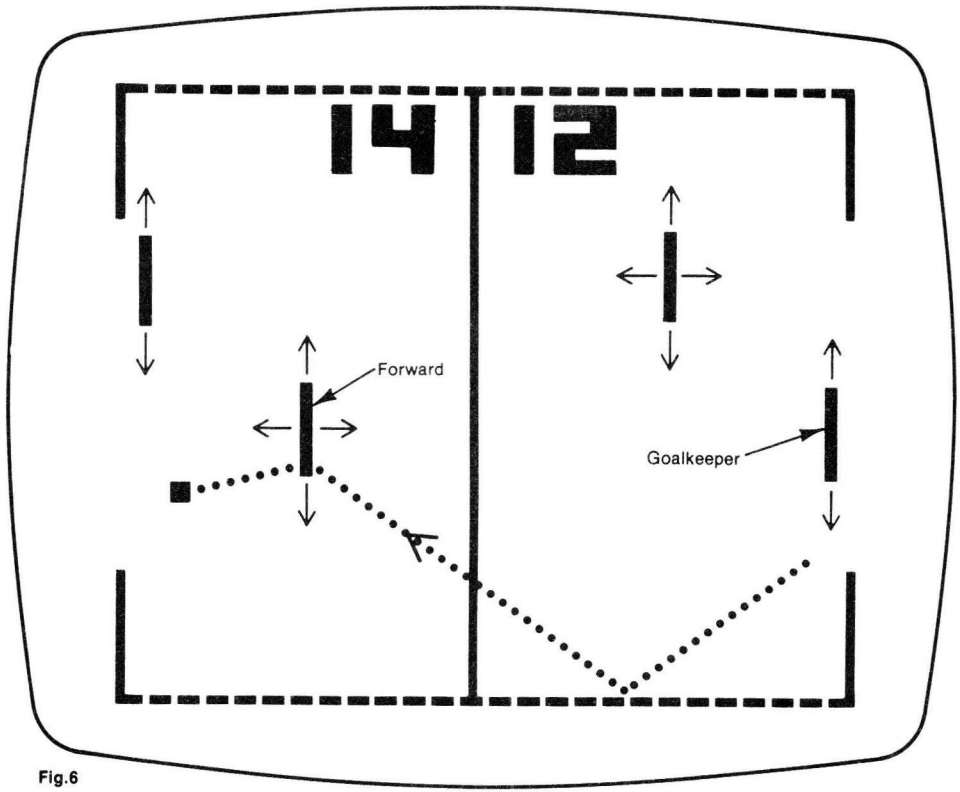


Fig.6

Soccer

The 'soccer' type game is shown in Figure 6. With this game each participant has a 'goalkeeper' and a 'forward'. The layout is such that the 'goalkeeper' is in his normal position and the 'forward' can be positioned in any part of the playing area.

When the game starts, the ball will appear travelling from one goal line towards the other side. If the opponent's forward can Intercept the ball, (Figure 6a), he can 'shoot' it back towards the goal. If the ball is missed it will travel to the other half of the playing area and the first team's forward will have the opportunity of intercepting the ball and redirecting it forward at a new angle according to the 'player' section which is used, (Figure 6b). If the ball is 'saved' by the 'goalkeeper' or it reflects back from the end boundary, the same forward will have the opportunity to intercept the outcoming ball and divert it back towards the 'goal'.

A 'score' is made in the 'soccer' game by 'shooting' the ball through the defined goal area. The scoring and game control is done automatically as for the tennis game. The same audio signals are used to add atmosphere to the game.

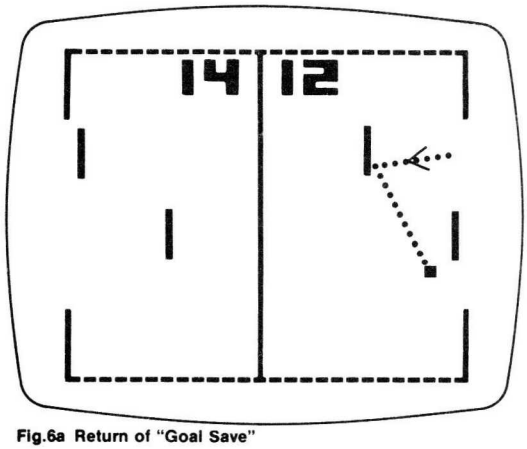


Fig.6a Return of "Goal Save"

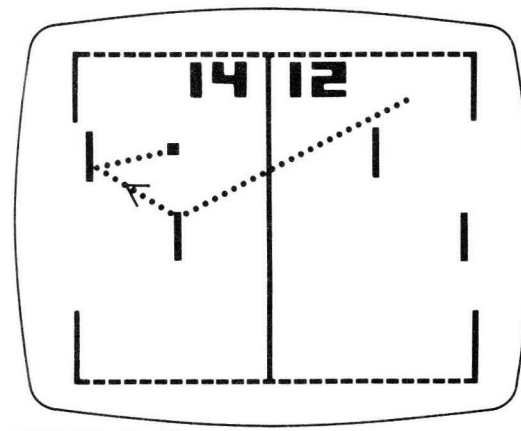


Fig.6b "Shooting" Forward

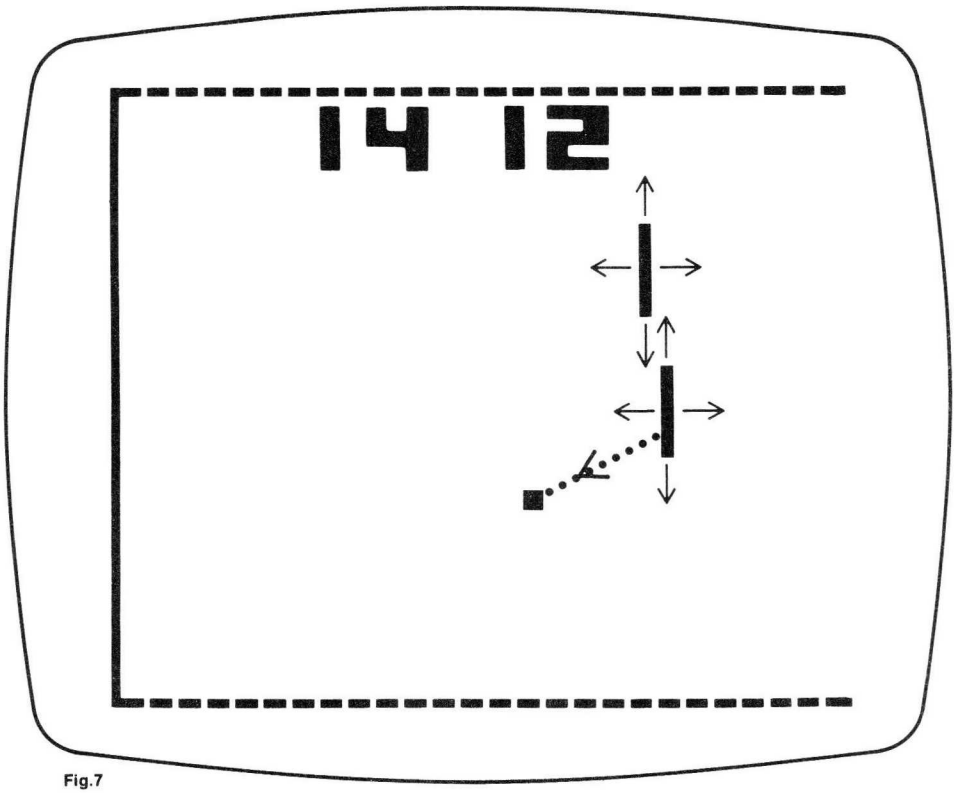


Fig.7

Squash

This game is illustrated in Fig. 7. There are two players who alternately hit the ball into the court. The right hand player is the one that hits first; it is then the left hand player's turn. Each player is enabled alternately to ensure that the proper sequence of play is followed. The ball is colored to the color of the bat of the next player who's to hit the ball.

Practice

This game is similar to squash except that there is only one player. See Fig. 8. The left score counts misses; the right score counts hits. The game ends when either 15 misses occur or when 15 consecutive hits are made without a miss. The right score is reset if it is not 15 and a miss occurs.

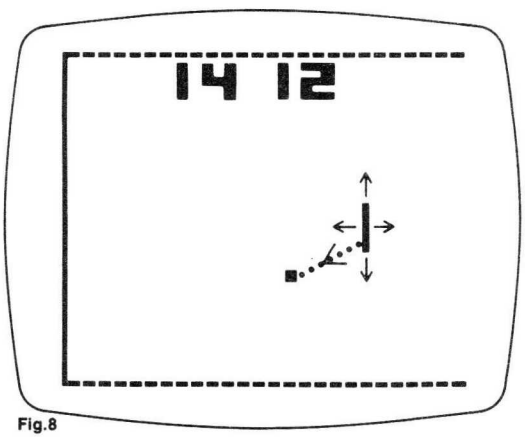


Fig.8

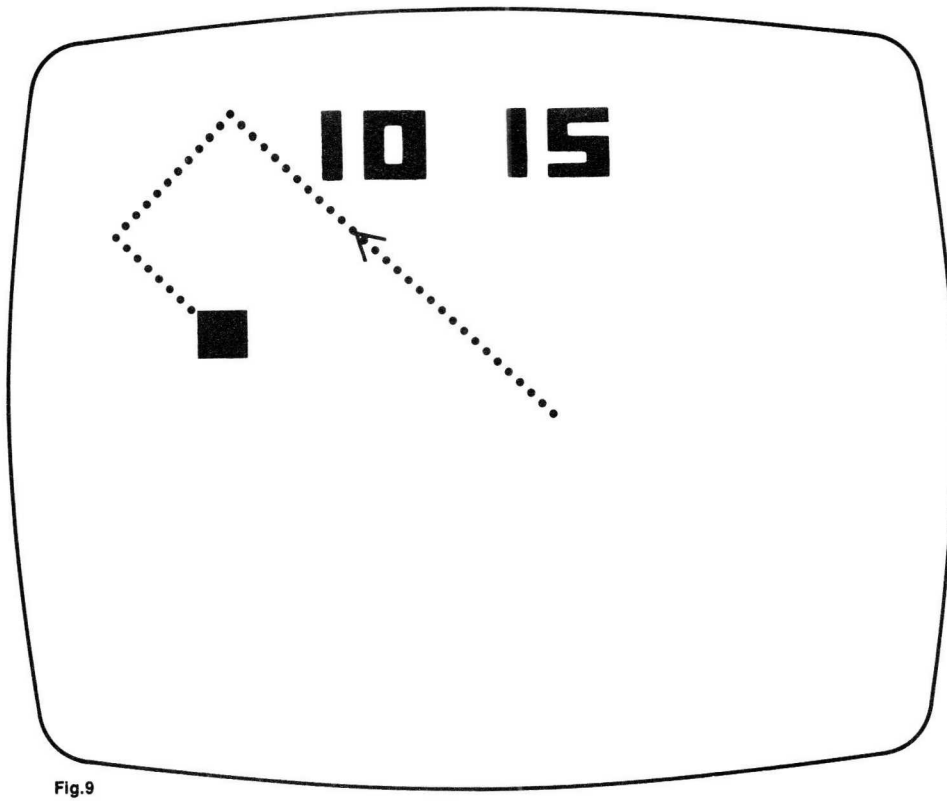


Fig.9

Rifle Game No. 1

This game is illustrated in Fig. 9. It has a large target which bounces randomly about the screen. A photocell in the rifle is aimed at the target. When the trigger is pulled, the shot counter is incremented and, if the rifle is on target, the hit counter is incremented, a hit noise is generated and the target is blanked for a short period. After 15 shots the score appears but the game can still continue without additional scoring.

Rifle Game No. 2

In this game, illustrated in Fig. 10, the ball traverses the screen from left to right under control of the manual serve button. Otherwise the game is as described for Rifle Game No. 1.

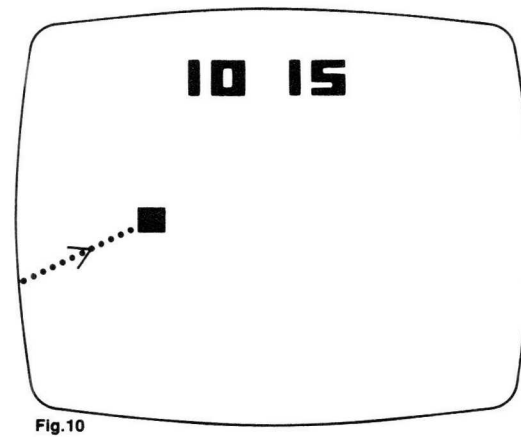


Fig.10

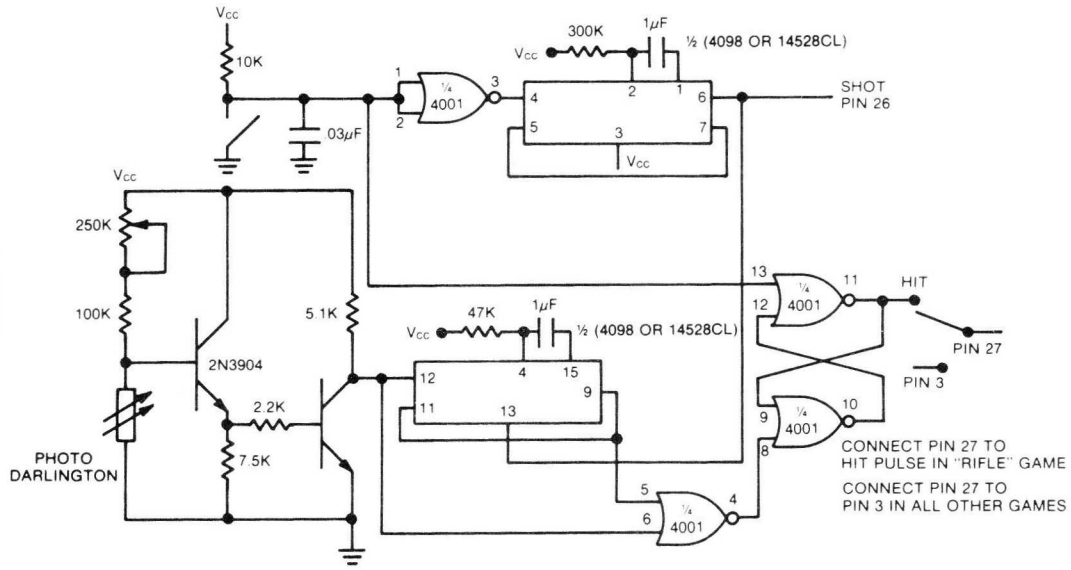


Fig.11 RIFLE INTERFACE

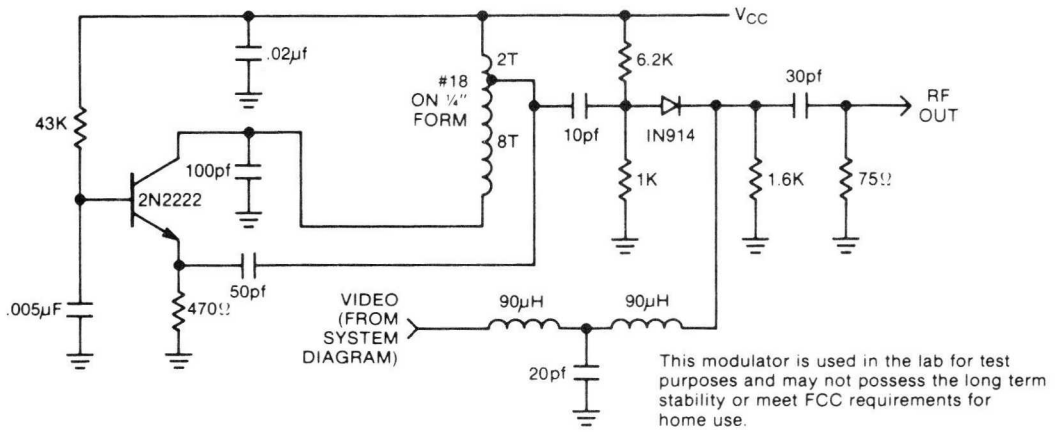


Fig.12 VHF MODULATOR

	Horizontal	Vertical
Slow	± .5μs	2 angles ± 1 line 4 angles + 3 lines
Fast	± 1μs	2 angles ± 2 lines 4 angles + 5 lines

Fig.13 ANGULAR MOTION

Color Processor

DESCRIPTION

The AY-3-8515 is a single N-Channel MOS circuit which accepts the video outputs of the AY-3-8500-1 and AY-3-8550-1 game circuits and converts the black and white signals to a single color composite video output. The colors of the background and paddle outputs are selectively changed directly by the game select inputs. The circuit also provides, as an output, a 2.045MHz clock for the game chip.

OPERATION

The AY-3-8515 provides a color composite video signal with color burst envelope and sync for input to the RF modulator of a TV game.

Sync: The sync input from the AY-3-8500-1 or AY-3-8550-1 is reconstructed in the color circuit and provides both front and back porches to insure correct operation in color TV circuits.

Color Burst: A color burst signal, containing ten cycles of the 3.579MHz color reference, is supplied after sync. The color phase of the burst is internally selected by the game select inputs with respect to the phases of the background, right player and left player so that different colors may be rendered for each game. This color change may be affected with no external components for ball and paddle games and only requires the addition of two diodes when target games are also selected.

The color burst is followed by an appropriate blanking interval so the TV set will not lock on to the background phase.

Video Inputs: Four video inputs are provided on the AY-3-8515. These are: field and score, left player, right player and ball. When operated with the AY-3-8550-1, the ball input should be grounded.

Video Output: After sync, color burst and blanking, the video consists of background, field and score, right player, left player and ball. The ball output is always white. In the absence of other signals, the background is output.

The color outputs are:

Grounded Select Input	Back-ground	Field	Right Player	Left Player
1 Tennis	Green	Yellow	Magenta	Blue
2 Soccer	Blue	Cyan	Dk Blue	Red
3 Squash	Magenta	Lt. Red	Blue	Yellow
4 Practice	Cyan	Green	Brown	Blue
	Green			

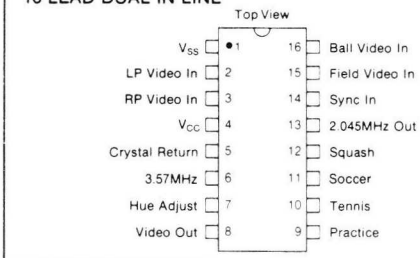
Colors may be adjusted for system variations by the chip hue control which varies the phase delay of the color outputs.

For games incorporating rifle, select input 3 may be connected by diodes to the squash select and practice select inputs of the game circuit, and select input 4 may be connected by diodes to the two rifle inputs.

Luminescense Levels: The luminescense levels of the various signals in the composite video output have been selected to provide black and white compatibility. The field and left player signals are set to near white levels, the right to near black, and the background is set at a mid level to show gray.

Figure 1 shows the typical composite video waveform from the circuit.

PIN CONFIGURATION
16 LEAD DUAL IN LINE



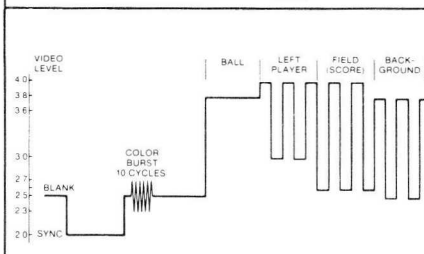


Fig. 1 COMPOSITE VIDEO OUTPUT

Characteristics at +25°C & V_{CC}= +6.0V	Min	Typ	Max	Units
Clock Input (Crystal)	—	3.579545	—	MHz
Video & Game Select Inputs				
Logic "0"	—	—	1.0	Volts
Logic "1"	V_{CC} −2	—	—	Volts
Hue Adjust (External)	2.0	—	V_{CC}	Volts
Video Output (bias to V_{CC})	—	1K	—	Ω
Clock Output Rise & Fall Time	—	100	—	ns

In order to assure the correct video levels, a 1K variable potentiometer should be used to adjust the output to a maximum of 4 volts and a minimum of 2 volts.

CLOCK INPUT

The AY-3-8515 is operated directly from a 3.579MHz crystal input. A variable capacitor with a range of 3 to 15 pF should be used to tune the crystal.

CLOCK OUTPUT

The AY-3-8515 generates a low impedance 2.045MHz clock to directly drive the game chip without external components.

Roadrace

FEATURES

- Two game selections—one and two player games
- T.V. raster generator
- All timing signals for color or black and white application
- Direct compatibility with Economy "8600" game console
- Automatic on-screen scoring
- Score color-keyed for each player
- Skill selection for difficult or easy driving conditions
- Realistic motor and crash sound generation with a minimum of external components

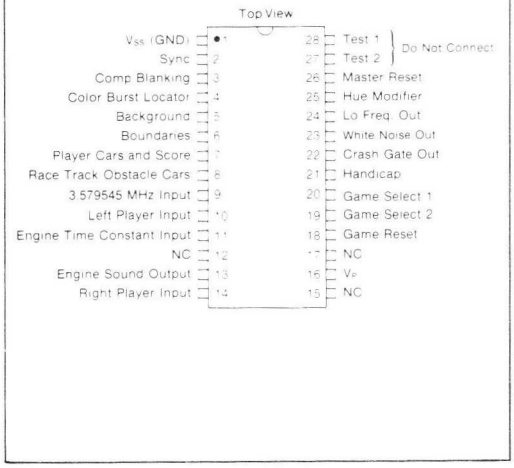
DESCRIPTION

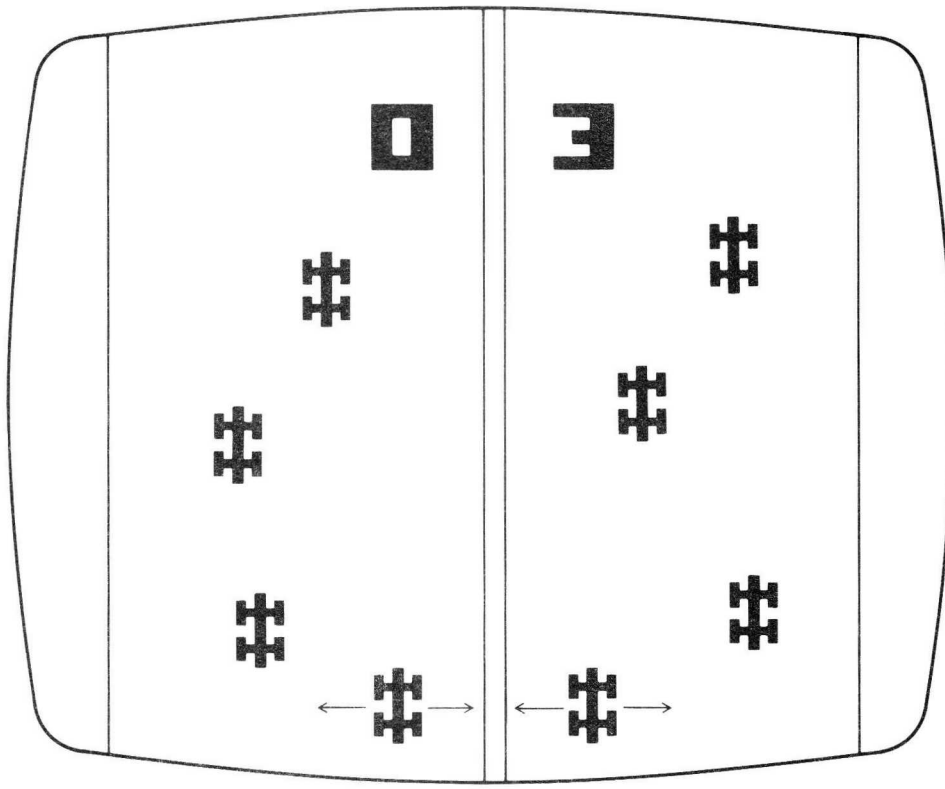
The AY-3-8603/8603-1 game circuit has been designed to provide a realistic roadrace game using a standard television receiver. The circuit is intended for color or black and white usage with a 525 (AY-3-8603-1) or 625 (AY-3-8603) line receiver. The circuit is designed to be either a stand-alone game or an add-on for the Gimini Economy "8600" game series.

OPERATION

The AY-3-8603/8603-1 utilizes two potentiometers to produce control voltages for the horizontal positioning of the race cars. Each player controls his own car. The circuit displays a score for each driver, processes the game logic and produces composite sync, color burst location and blanking signals for a 525 or 625 line T.V. receiver. Sound outputs are also included to produce simulated engine and crash sounds with a minimum of external components. The AY-3-8603/8603-1 are designed to be operated with the AY-3-8615 color circuit.

PIN CONFIGURATION
28 LEAD DUAL IN LINE





Roadrace (2 player)/ Qualify (1 player)

A typical T.V. screen display for the game is shown above. One driver for each car located at the bottom of each track controls his horizontal position only. After the game is reset the game starts as the picture produced simulates a race track in motion where each driver must maneuver his car around the other cars on the track. Both tracks have the same random obstacle car pattern with two visible per track, the pattern on the right is 24 lines ahead of the left pattern. This produces random cars on both tracks at one time with the same degree of difficulty for each driver. Video speeds increase every two seconds up to a maximum of seven speeds forward or until either player crashes his car into an obstacle car. Upon a crash, the video motion will stop and a crash sound will be generated. When the game restarts, the forward motion will start from slow and progress in speeds once again.

Simulated engine sound is produced during the game. The engine starts from low and increases in pitch at four second intervals during motion to simulate shift points during the game progress. Every crash scores one point for the opponent. Scores are shown over each track.

The one-player game selection removes the car image on the right track and left driver plays. A point is scored for the driver after passing every eight consecutive obstacle cars. Every crash gives the game, (right track) score one point. The first player or game to score 15 ends the game in either one or two player selection.

Warfare

FEATURES

- Outputs include NTSC (AY-3-8605-1) or CCIR (AY-3-8605) compatible composite sync, color burst location and blanking.
- Operation from a 3.579545 clock
- One or two player game
- Digital on-screen scoring
- Sound generation for engine, sonar, firing and explosions
- Designed for use with AY-3-8615.
- Outputs and power requirements compatible with the Gimini Economy "8600" game series.

DESCRIPTION

The AY-3-8605/8605-1 game circuit has been designed to provide realistic sea and space battle games using a standard television receiver. The circuit is intended for use with a 525 (AY-3-8605-1) or 625 (AY-3-8605) line receiver.

OPERATION

The AY-3-8605/8605-1 utilizes two potentiometers (one for each player) or one axis of two joysticks to produce control voltages for internal Schmitt triggers. These position the submarine, destroyer, and spaceships, via rate controllers in the horizontal axis only. The circuit displays an on-screen score for each player, processes the game logic and produces a composite sync, color burst location and blanking signals for a 525 or 625 line T.V. receiver. Sound outputs are also included to produce simulated engine, sonar, firing, and explosion sounds with a minimum of external components.

The AY-3-8605/8605-1 may be operated with the AY-3-8615 color processor circuit. The outputs are designed for compatibility within the Gimini Economy "8600" Game series. Game selection is made via a 2 strobe/3 select switch matrix with momentary contacts.

Two momentary switches that ground the "fire" input pins are used to activate the torpedoes, depth charges, and missiles.

SOUND OUTPUTS

Space background noise—7 Bit Polynomial Counter clocked at 2 kHz rate

Torpedo or Depth Charge fired—1 kHz signal for 2 frames then off for 4 frames.

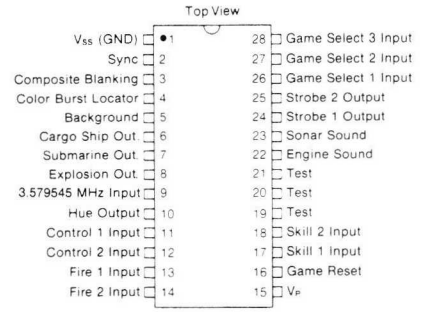
Explosion—$\sim$8 kHz signal for $\sim$ 3½ seconds

Destroyer engine—Fast sound is a 240 Hz clock into a 4 bit poly counter — Slow sound is a 120 Hz clock rate

Sonar for Submarine—Decaying 480 Hz signal for $\sim$ 2.9 seconds followed by a 2 kHz signal burst for $\sim$ 200 ms. This sound repeats every 3½ seconds.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



MOVEMENT

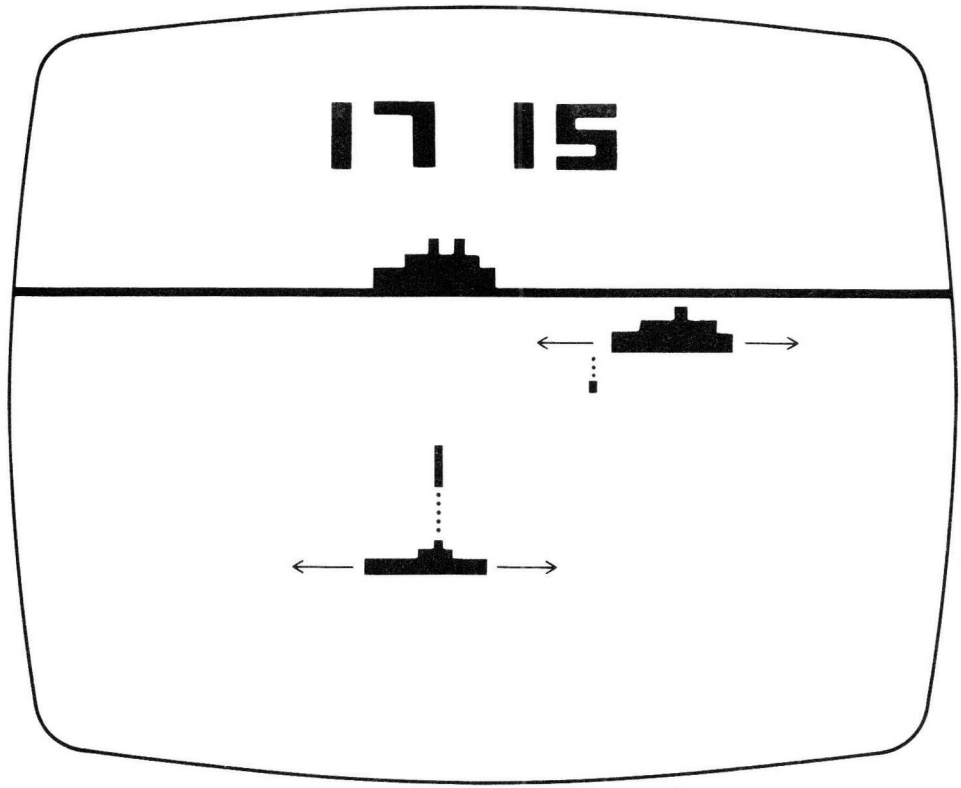
The cargo ship will traverse the screen in 16 seconds.

The destroyer ship will traverse the screen in 5.3 seconds.

The submarine moves across the screen in 8 seconds.

The torpedo rises at a rate of 1 line per frame. To move the 100 lines to hit the destroyer will take 1.67 seconds.

The depth charge falls at a rate of 1 line every 2 frames. To hit the submarine will take 3.34 seconds.



Sea Battle (2 player)

One player controls the horizontal movement of the destroyer and the other player controls the horizontal movement of the submarine. The engine sound of the destroyer will be fast for either left or right movement and slow for no movement. Both the submarine and the destroyer will stop for a center position of the joystick. The cargo ship moves across the upper part of the screen at a fixed speed. The submarine player fires torpedoes to score 1 point for hitting the cargo ship and scores 2 points for hitting a restricted area of the destroyer. If the SKILL Switch #1 is off, the submarine player scores a point if the torpedo hits any area of the destroyer.

The destroyer player drops depth charges at the submarine and scores a point for hitting an area close to the submarine and scores 2 points for a direct hit if the SKILL Switch #2 is on.

A hit of the torpedo on the cargo ship or the destroyer will cause the cargo ship to disappear for the duration of the explosion and the destroyer ship will change color. A depth charge hitting the submarine will cause the submarine to change colors during the explosion.

Neither ship is allowed to go off-screen and only one torpedoe will appear on the screen at any time, rising from the submarine to either strike a ship and cause an explosion or disappear. Only one depth charge will appear on the screen at any time, falling from the destroyer to explode on the submarine or disappear when hitting the sea bottom.

Sounds include a destroyer engine, submarine sonar, depth charge or torpedo firing, and explosions. The game is over when either player scores 30 points.

Counterattack I (1 player)

One player controls the horizontal movement of the submarine and fires torpedoes at the destroyer ship. There is no cargo ship in this game. The destroyer ship moves across the screen dropping depth charges. As the depth charge falls it will either hit the submarine and cause an explosion or hit the sea bottom and drop another depth charge.

The player scores 1 point if the torpedo hits any area of the destroyer (SKILL Switch #1 is off). 2 points are scored if the torpedo hits a restricted area of the destroyer and SKILL Switch #1 is on. Points against the player are scored if the depth charges hit the submarine. 1 point is scored for a hit close to the submarine and 2 points for a direct hit if SKILL Switch #2 is on.

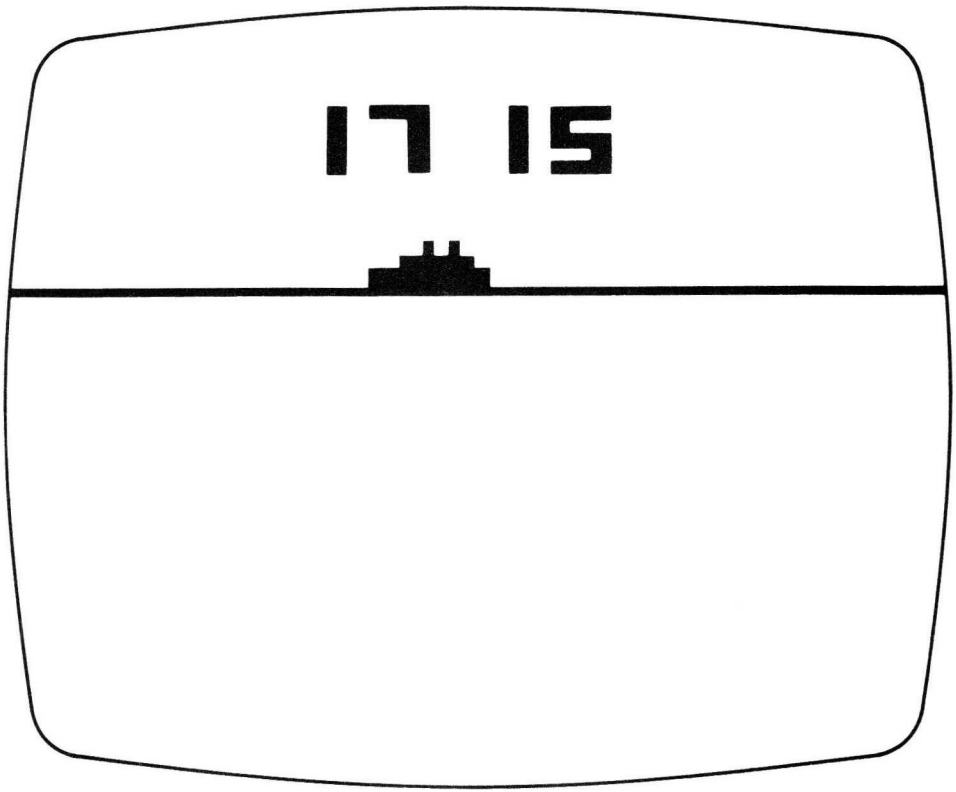
When either ship has been hit an explosion will occur and the ship that was hit will change color. It is possible that both ships have been destroyed at the same time.

The sounds include the destroyer ship engine, submarine sonar, torpedo firing, and explosions. The game is over when either the player scores 30 points or the destroyer has accumulated 30 points.

Counterattack II (1 player)

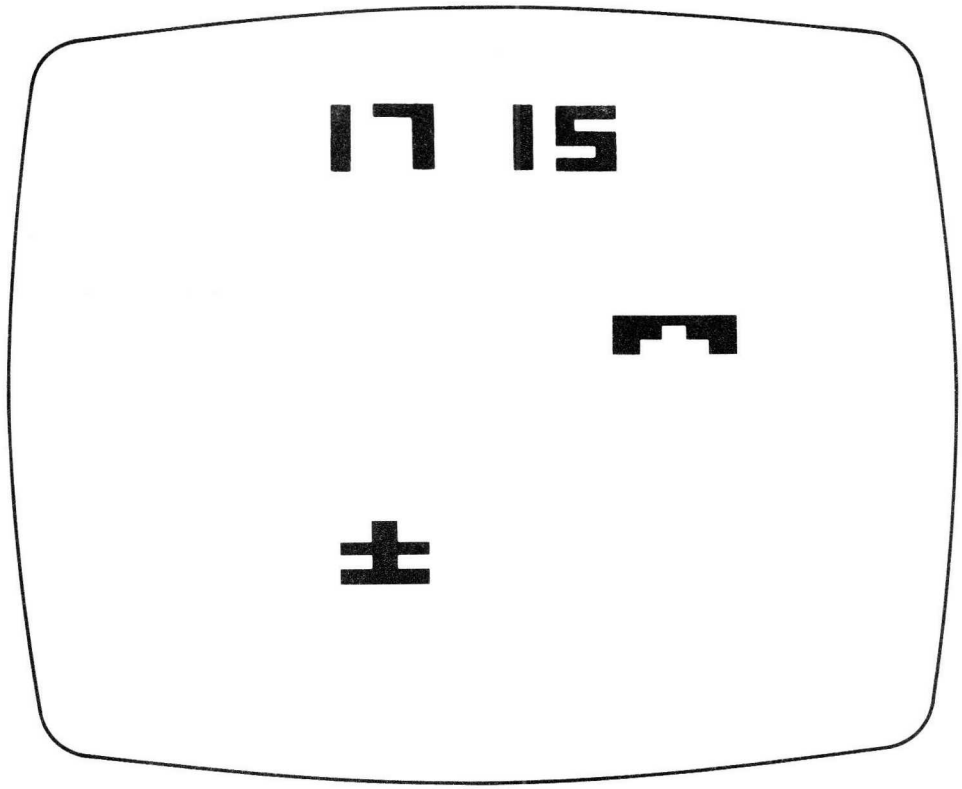
One player controls the horizontal movement of the destroyer and the firings of the depth charges. This player must protect his ship and the cargo ship from the torpedoes fired automatically from the submarine. As the submarines torpedoes destruct from a ship impact, another torpedo is launched after the 3½ second explosion. Torpedoes that miss the destroyer ship or the cargo ship will disappear in the air and a new torpedo will be launched. The submarine moves across the screen reversing its direction at each edge of the screen.

The scoring for this game is the same as for the previous games. The sounds include the destroyer ship engine, submarine sonar, depth charge firing, and explosions. The game is over when either the player scores 30 points or the submarine has accumulated 30 points.



Night Battle (2 player)

One player controls the horizontal movement of the destroyer and the other player controls the horizontal movement of the submarine. The cargo ship traverses the screen, changing directions when it reaches the edge of the screen. This game plays just like the 2 player - Sea Battle - except that the only time the submarine is visible is when a torpedo has been fired. Likewise the cargo ship and the destroyer are not visible until a depth charge has been dropped. Scoring, SKILL Switch selections, and sounds are the same as described in - Sea Battle -.



Space Battle I (2 player)

One player controls the Space Warp 1 vehicle and the other player controls the Space Warp 2 vehicle. Missiles are fired from one ship toward the other. There is no equivalent of a cargo ship from the sea battle games in this space game. The object is to fire your missiles at your opponent's vehicle and score either 1 or 2 points for the type of hit dependent on the SKILL Switch setting. The sounds include a space background and sounds for missile firings and explosions. The game is over when either player reaches 30 points.

Space Battle II (2 player)

This two player game is very similar to the Space Battle I game except that the space vehicle is only visible when it has fired a missile.

Wipeout

FEATURES

- Outputs include NTSC compatible composite sync, color burst location and blanking for AY-3-8606-1 and CCIR for AY-3-8606.
- Operation from a 3.579545 MHz clock.
- One or two player games.
- Digital on-screen scoring.
- Sound generation for tones to indicate hits of ball to bat, ball to objects, and ball to border.
- Designed for use with AY-3-8615.
- Outputs and power requirements compatible with Gimini Economy "8600" Game Series to allow plug-in operation.

DESCRIPTION

The AY-3-8606/8606-1 game circuit has been designed to provide an active paddle/squares game using a standard television receiver. The circuit is intended for use with a 525 (AY-3-8606-1) or 625 (AY-3-8606) line receiver.

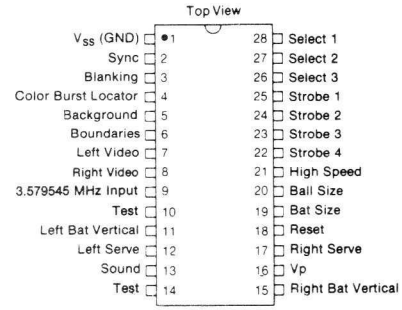
OPERATION

The AY-3-8606/8606-1 utilizes two potentiometers (one for each player) one axis only of each joystick to produce control voltages for internal Schmitt triggers. These position the player's bats in the vertical axis only to allow play of the game. The circuit displays an on-screen score color coded to each player, processes the game logic and produces a composite sync, color burst location and blanking signals for a standard 525 (625 for AY-3-8606) line TV receiver. Sound output is also included to produce tonal sounds for ball hits to bats, ball hits to borders and ball hits on objects with a minimum number of external components.

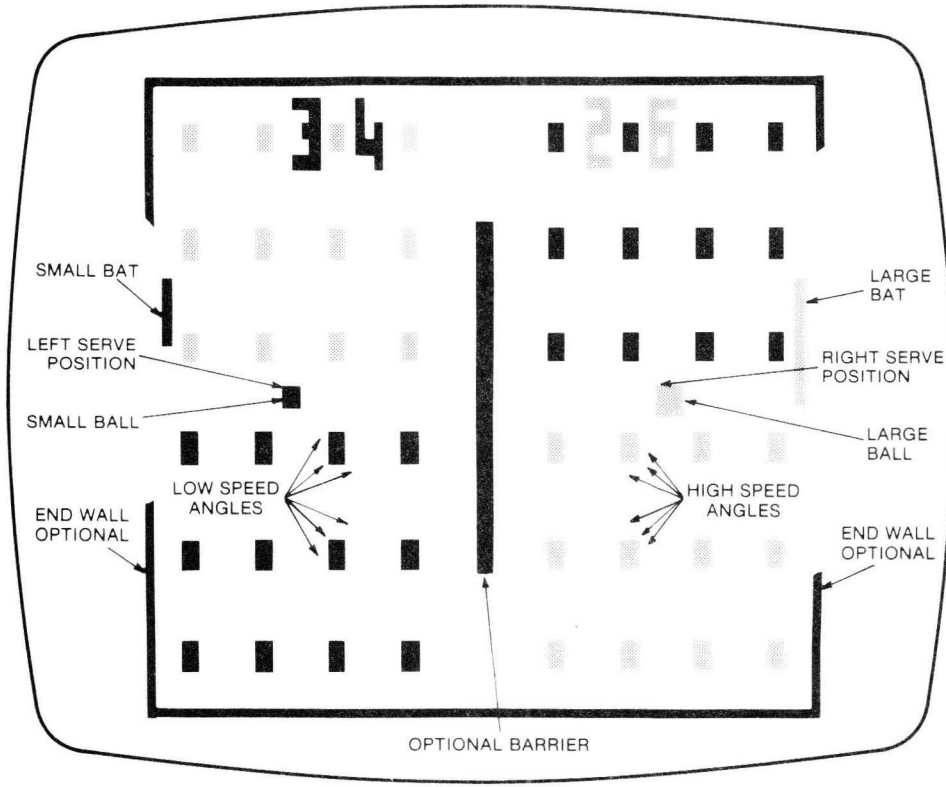
The AY-3-8606/8606-1 is made to be operated with the AY-3-8615. The outputs are designed for compatibility within the Gimini Economy "8600" Game Series. Game selection is made via a 4 strobe, 3 select switch matrix with either fixed or momentary contact closures.

PIN CONFIGURATION

28 LEAD DUAL IN LINE.



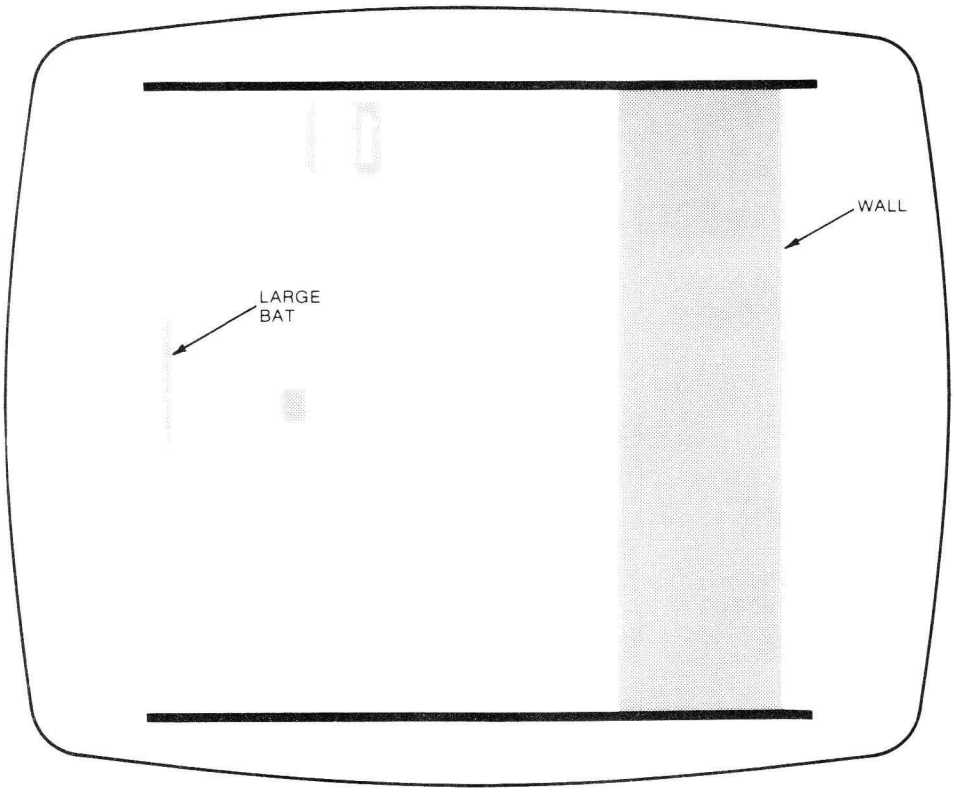
Two momentary switches that ground the input serve control pins are used to start the ball into motion after reset or when a reserve is necessary according to game rules. Three skill selection switches are used to determine game difficulty.



Wipeout I-IV
Color Squares I-IV

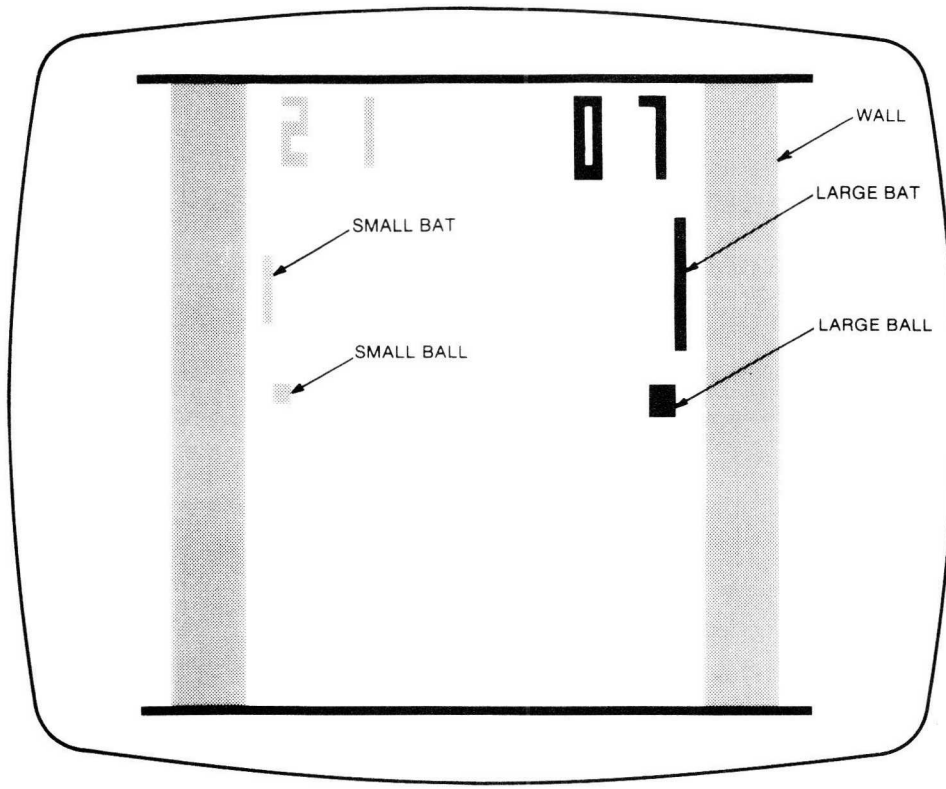
In the Wipeout and Color Squares games, the object is to eliminate squares in the playing area by controlling the ball rebound angle off the bat(s). Variations include one-player/two-player games, optional end walls, optional mid-court barriers, and size/speed/angle selections.

Game	#Players	#Bats	Barrier	End Walls
Wipeout I	1	1	NO	RIGHT
Wipeout II	1	2	NO	NO
Wipeout III	2	2	NO	RIGHT & LEFT
Wipeout IV	2	2	YES	NO
Color Squares I	1	2	NO	NO
Color Squares II	2	2	NO	NO
Color Squares III	2	2	YES	NO
Color Squares IV	1	2	NO	RIGHT



Breakthrough I

This game selection uses a playing area as shown above. It is a single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball. The objective is to break through the end wall and score on as many blocks as possible. The game ends after either seven serves or the first breakthrough.



Breakthrough II

This game selection uses a playing area as shown above. It is a two-player game in which each player manipulates his paddle in the center of the playing area in the vertical axis. The ball is kept in motion by each player trying to protect the wall behind his paddle. If a player misses a hit with the paddle, the ball will hit the wall and one block will disapear and the score will increment for the opposite player. The objective of this game is to knock out as many blocks to get a high score before breaking through the wall. The first player to hit the ball through an open section of a wall ends the game.

Shooting Gallery

FEATURES

- Outputs include NTSC (AY-3-8607-1) or CCIR (AY-3-8607) compatible composite sync, color burst location and blanking.
- Operation from a 3.579545 MHz clock.
- One or two player game.
- Digital on-screen scoring.
- Sound generation for flight, fall, hit and impact.
- Designed for use with AY-3-8615.
- Outputs and power requirements compatible with Gimini Economy "8600" Game Series to allow plug-in operation.

DESCRIPTION

The AY-3-8607/8607-1 game circuit has been designed to provide an active series of target games using a standard television receiver. The circuit is intended for use with a 525 (AY-3-8607-1) or 625 (AY-3-8607) line receiver.

OPERATION

The AY-3-8607/8607-1 utilizes an external photo cell mounted in a gun or rifle for recording hits. The logic requires the gun to input a shot pulse when the trigger is pulled and if the photocell in the gun records the hit (if on target) a pulse will be transmitted to the chip. (No pulse if off target).

Some of the two-player games require two guns.

With the two-player game where one player controls the target and the other shoots, the joystick in the console will be used for target control.

Skill select switches on the console are used for (1) target size large or small (2) target speed, fast or slow. In two-player/two-rifle games, the left joystick is used for additional handicapping/skill selection.

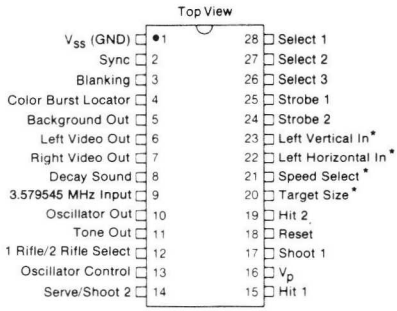
GAME SKILLS

All games will have difficulty selection in the following areas:

A. Two speeds for the target - fast and slow.
B. Two sizes for the target - large and small.
C. Joystick-selected handicap.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



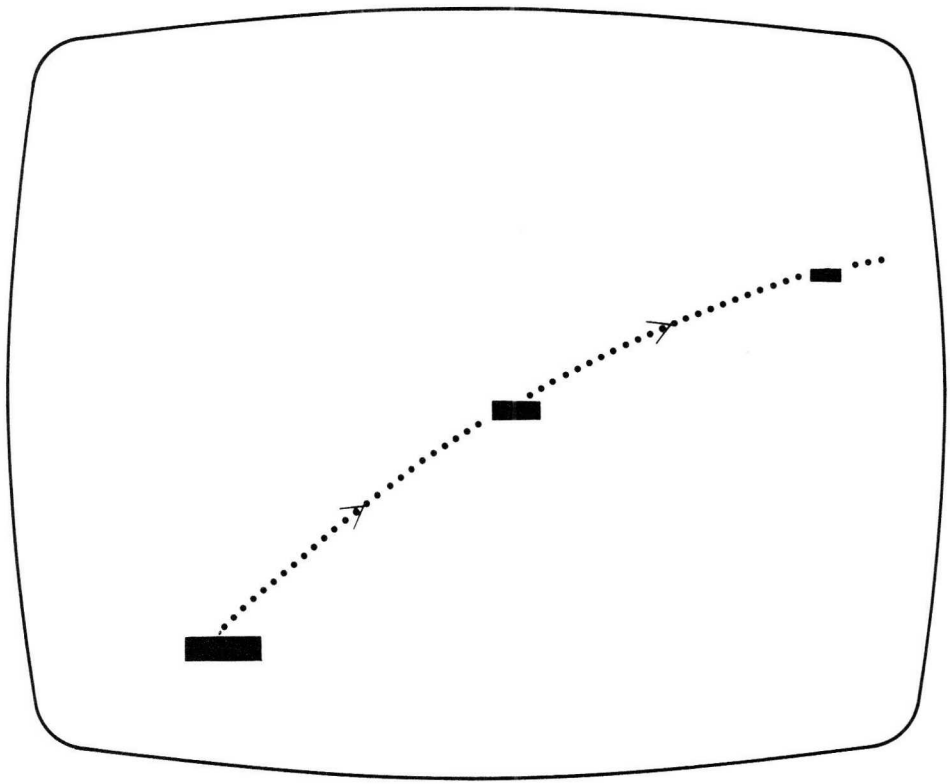
*Pin functions are for one-player games.
For two-player games, the funtions of pins 20 thru 23 are:

20 — Player 1 Target Size
21 — Player 1 Speed Select
22 — Player 2 Target Size
23 — Player 2 Speed Select

These selections are to be made on two pins which will make one selection (the easiest) when left open.

ON SCREEN SCORING

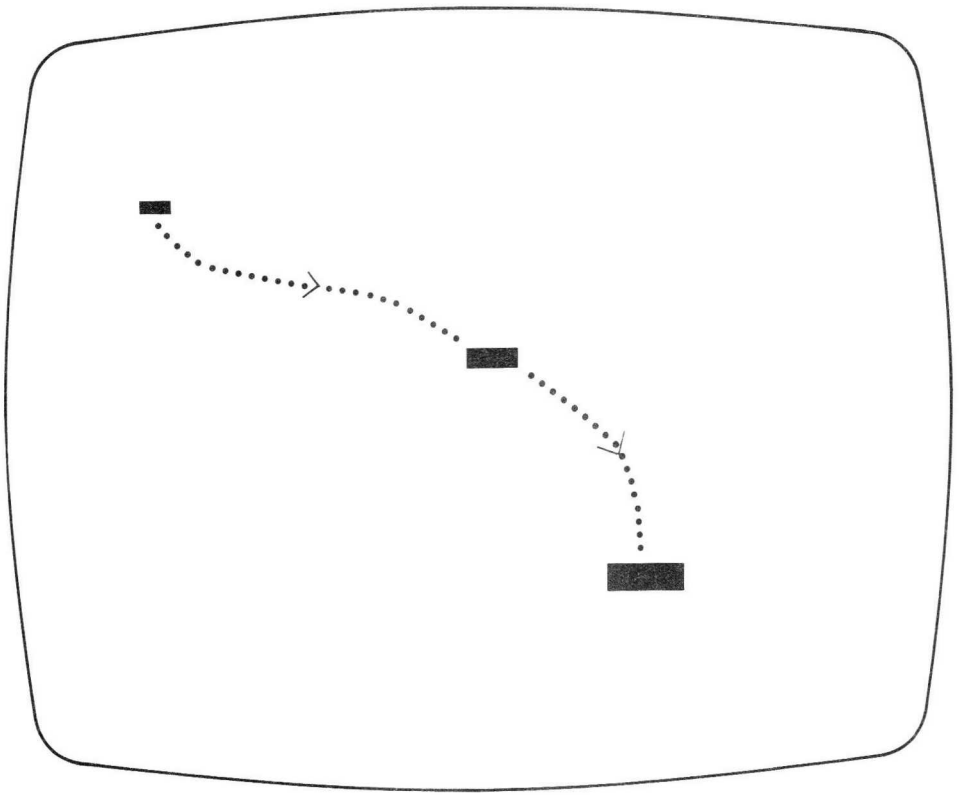
All scoring will be displayed on the screen momentarily after each flight or target sequence to show an update of the game in progress. Score is flashed at end of game.



Skeet I-IV

The Skeet games consist of a target which starts in the foreground and disappears into the background in a curved trajectory. The games may be played by one or two players: the one player games have circuit controlled target trajectory; the two player games allow the second player to have joystick control of the target trajectory; or the two players may both use external guns to shoot at the target with circuit target control.

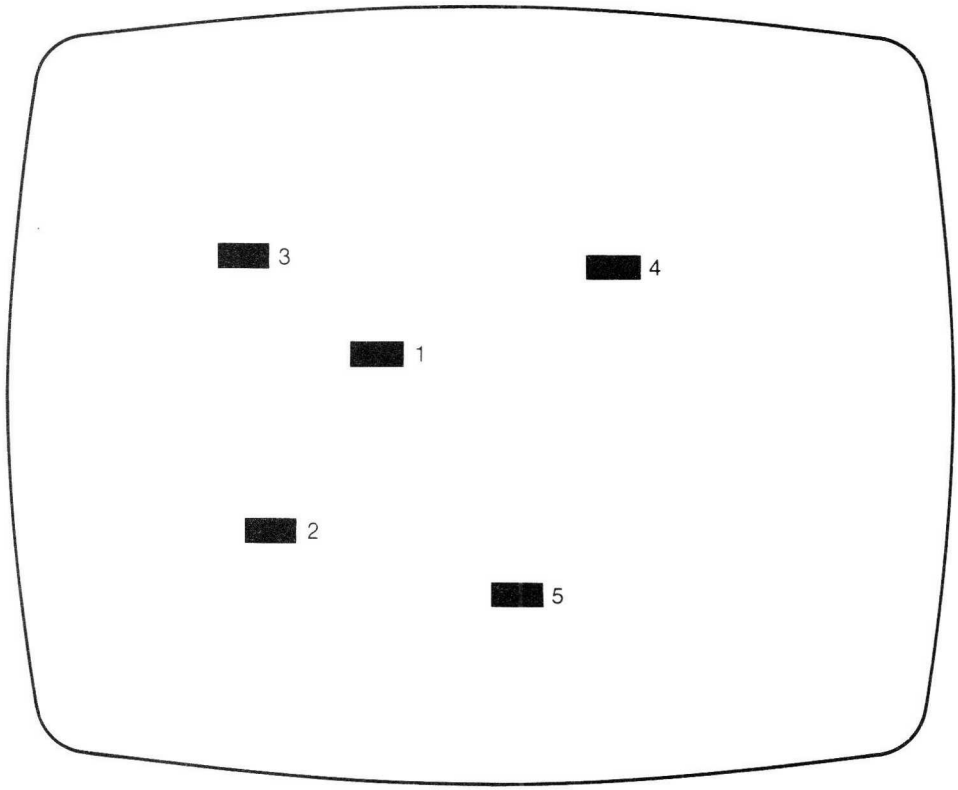
Each Skeet game produces realistic fire and explosion sounds plus target movement sounds.



Attack I-IV

The Attack games consist of a target which starts in the background and moves toward the foreground in a random trajectory. The games may be played by one or two players: the one player games have circuit controlled target flight; the two player games allow the second player to have joystick control of the target flight; or the two players may both use external guns to shoot at the target which is circuit controlled.

Each Attack game produces realistic fire and explosion sounds plus target movement sounds.



Destruct I-IV

The Destruct games consist of targets which flash either randomly or in sequence in 15 positions. The games may be played by one or two players selectively. Two player games require two guns.

Each Destruct game produces realistic fire and explosion sounds.

Supersport

FEATURES

- Full **COLOR** Operation with AY-3-8615
- Ten selectable games — tennis, hockey, soccer, squash, practice, gridball, basketball, basketball practice, one and two player target
- 625 Line (AY-3-8610) and 525 Line (AY-3-8610-1) versions
- T.V. raster generator
- Two axis player motion
- Automatic on-screen scoring, 0-15
- Automatic ball speed-up after 7 hits or may be disabled by ball speed inhibit input
- Realistic ball service and scoring
- Score color keyed to player
- Independent player selectable bat size for handicapping
- Fast ball speed inhibit
- Five segment bats giving high, low, and horizontal ball angles
- Sound outputs for hit, rebound and score
- Shooting forwards in hockey and soccer

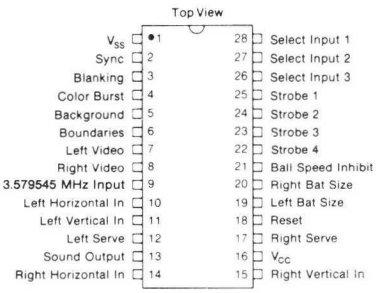
DESCRIPTION

The AY-3-8610 and AY-3-8610-1 circuits have been designed to provide a TV 'game' function which gives active entertainment using a standard color or black and white domestic television receiver.

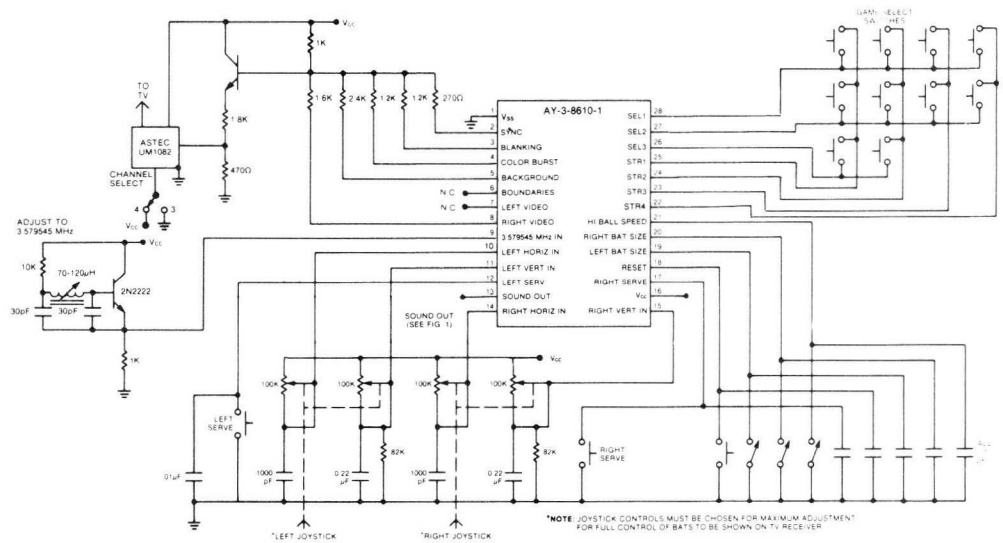
The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

PIN CONFIGURATION

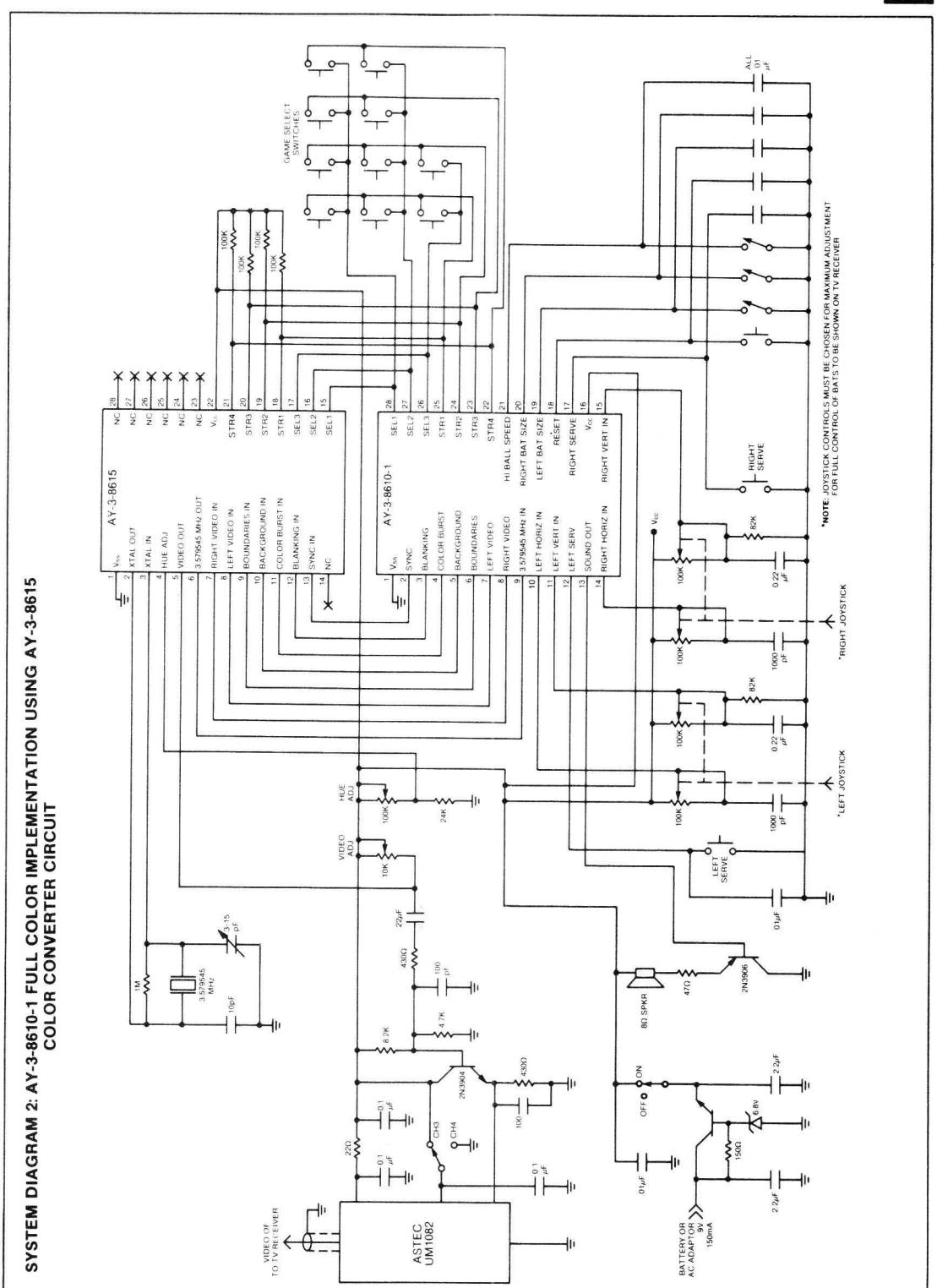
28 LEAD DUAL IN LINE



SYSTEM DIAGRAM 1: BLACK AND WHITE IMPLEMENTATION



SYSTEM DIAGRAM 2: AY-3-8610-1 FULL COLOR IMPLEMENTATION USING AY-3-8615 COLOR CONVERTER CIRCUIT



PIN FUNCTIONS

Power

V_{CC} positive supply input
V_{SS} negative (substrate) supply input

Clock Input — 3.579MHz — color burst to N.T.S.C.

For black and white operation, a simple LC oscillator can be used for the clock, but for color, the clock must be derived from a color crystal as shown in System Diagram 2.

Color Inputs

Right player vertical control
Right player horizontal control
Left player vertical control
Left player horizontal control
Right player serve
Left player serve
Right player bat size
Left player bat size
High speed ball inhibit
Game reset

The game is reset with scores set to zero and ball returned to the service position by momentarily connecting the reset input to V_{SS}.

Bat size can be selected as either small or large individually for handicapping purposes. Connection of the bat size input to V_{SS} selects small bat.

Bat position is set by a variable resistor and capacitor connected as shown in the System Diagram.

Fast ball speed may be inhibited by connecting V_{SS} to the High Speed Ball Inhibit input.

Game Select Inputs/Outputs

Strobe 1	Select Input 1
Strobe 2	Select Input 2
Strobe 3	Select Input 3
Strobe 4	

Game selection is made by the interconnection of one of the output strobes, STR 1, STR 2, STR 3, or STR 4, with one of the three input selection lines SEL 1, SEL 2, or SEL 3.

The game selections are defined as:

STR 1/SEL 1	Tennis
STR 1/SEL 2	Hockey
STR 1/SEL 3	Squash
STR 2/SEL 1	Practice
STR 2/SEL 2	Soccer
STR 2/SEL 3	Basketball
STR 3/SEL 1	Basketball Practice
STR 3/SEL 2	Gridball
STR 4/SEL 1	Single Player Target
STR 4/SEL 2	Two Player Target

Video Outputs

Right bat, score and ball
Left bat, score and ball
Boundaries
Background
Sync
Blanking
Color burst locator

All signals are present in the circuit to generate a composite video signal with composite blanking and sync. The combined video signal provides the input to the game RF modulator.

In addition to the above outputs, a color burst locator output is provided for use where external color generation is desired. The signal locates the position in the waveform behind the sync pulse.

In all games, the ball starts at slow speed. If the high speed mode has been selected the ball will switch to high speed after 7 consecutive hits by the players without a goal being scored.

The bats will be segmented into 5 zones, each zone defining a different rebound angle. The zones listed from top of bat to bottom are nominally high angle up, low angle up, horizontal, low angle down, high angle down. A ball passing through a forward from behind will have its angle influenced as above, but not its left/right direction.

All two player games will terminate when one player has 15 points at which time the bats have no further effect on the ball. The ball cannot be restarted until a game reset is applied.

Sound Output

Tone of approximately 500Hz, 1kHz and 2kHz will be output for a nominal period of 24msecs for ball hits wall, ball hits bat and score. The output is capable of directly driving 100 ohm speakers.

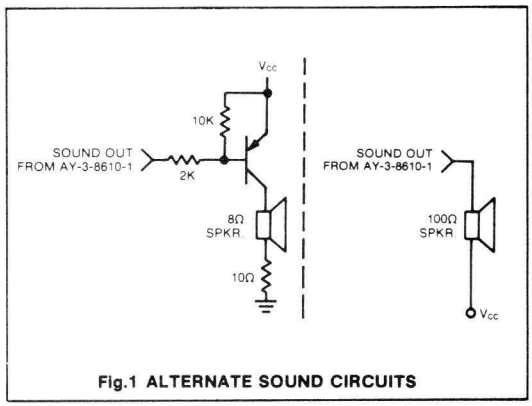


Fig.1 ALTERNATE SOUND CIRCUITS

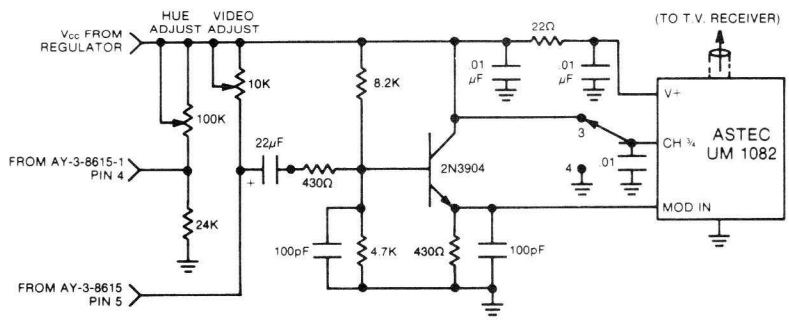


Fig.2 MODULATOR INTERFACE CIRCUIT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... −0.2 to +12V
Storage Temperature Range ..... −20°C to +70°C
Ambient Operating Temperature Range..... 0°C to +40°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V

Characteristics**	Min	Typ	Max	Units	Conditions
Clock Input					
Frequency	—	3.579545	—	MHz	
Logic '0'	0	—	0.5	Volts	50% duty cycle ±5%
Logic '1'	V_{CC} −2	—	V_{CC}	Volts	
Leakage	—	—	100	μA	
Control Inputs 12, 17, 18, 19, 20, 21, 26, 27, 28					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}−2	—	V_{CC}	Volts	
Input Impedance	—	100	—	kΩ	Pull up to V_{CC}
Outputs Pins 2-8, & 13					
On	—	—	1.0	Volts	I out = 2 mA
Off	—	—	100	μA	V out = V_{CC} (open drain)
Outputs Pins 22-25					
On	—	—	1.0	Volts	I out = 0.5 mA
Off	—	—	100	μA	V out = V_{CC} (open drain)
Power supply current	—	—	60	mA	At V_{CC} = +7.0V

**At 25°C & V_{CC} = 6V

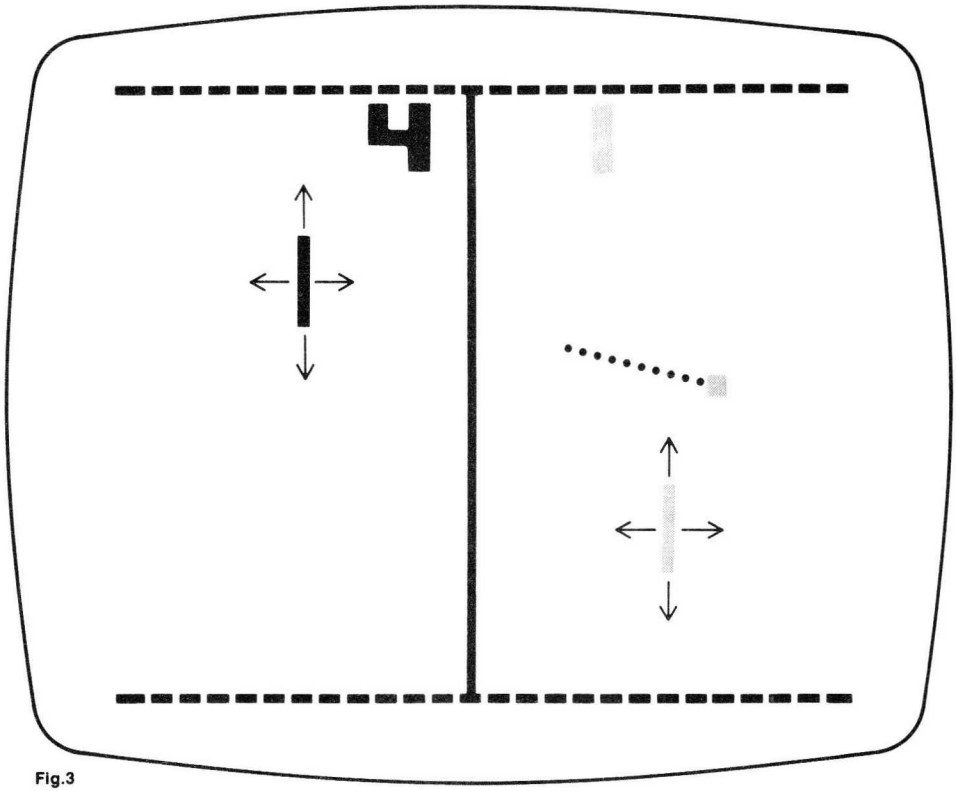


Fig.3

Tennis

This game uses a playing area as shown in Fig. 3. Each player can only move around his side of the court. The game will start when the player whose turn it is to serve, depresses his service button. The service will automatically change every five points scored. At service the ball will move away from the service point with a random angle but always toward the net.

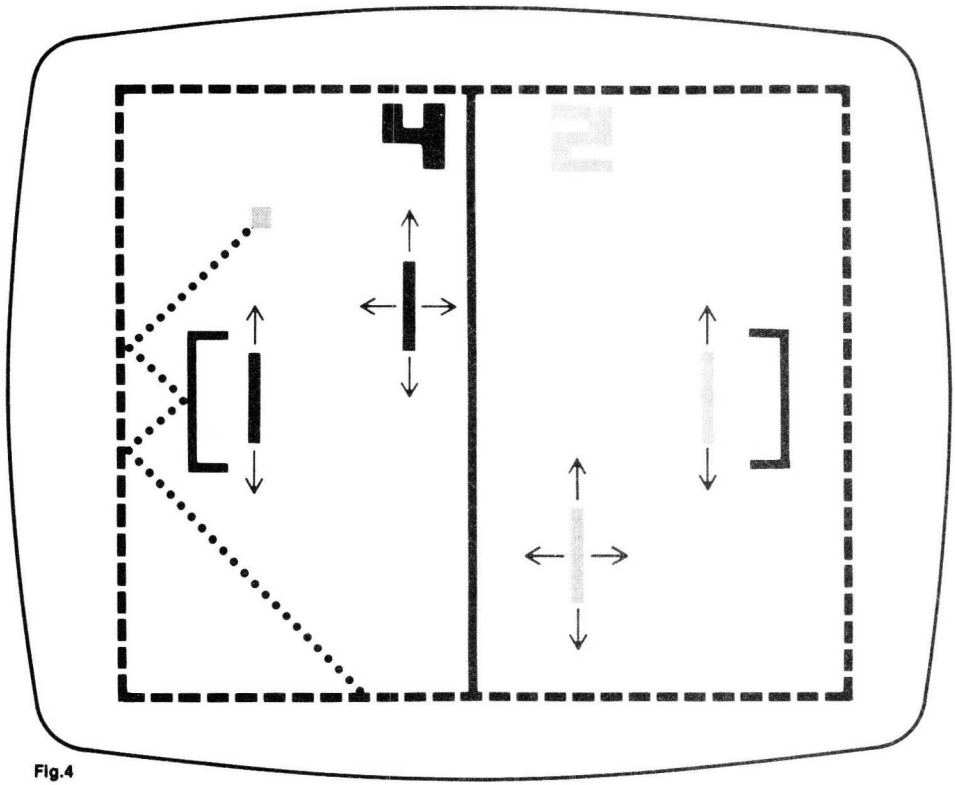


Fig.4

Hockey

This game uses a playing area as shown in Fig. 4. The forwards on both sides have freedom to move over the entire playing area. The goal keepers will be locked in the horizontal axis in front of their respective goals but will move in the vertical axis in the same manner as the forwards.

The game starts when both players have depressed their service buttons. The ball will move away from the face off point with a randomly selected angle in either direction.

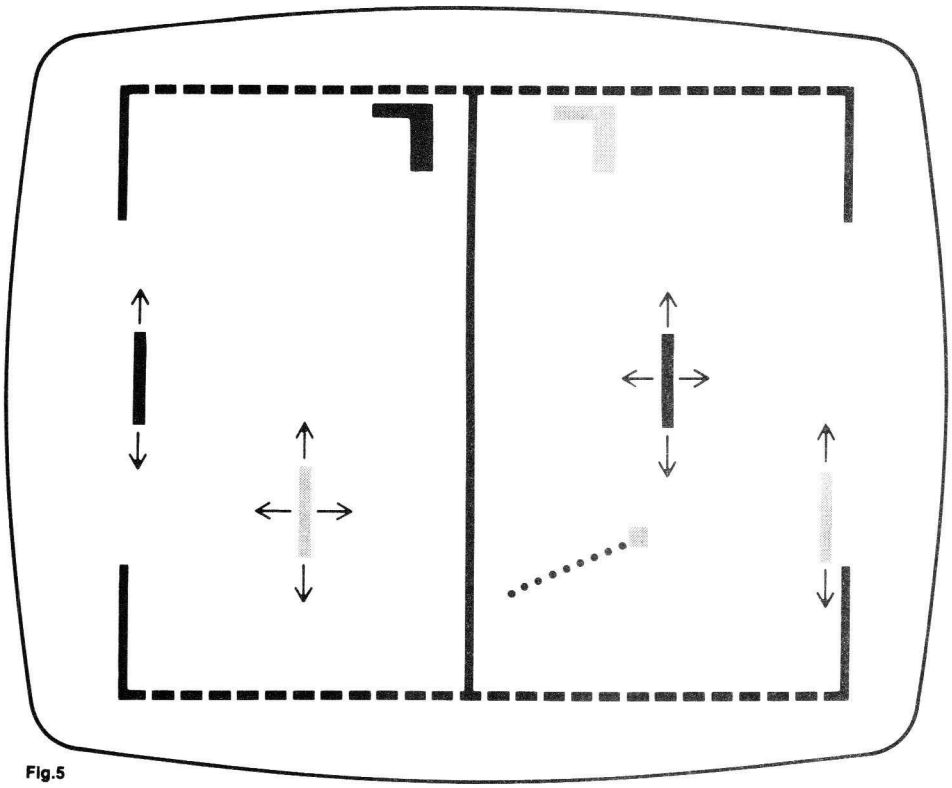


Fig.5

Soccer

This game uses a playing area as shown in Fig. 5. The motion of the players is as in the hockey game. The game will start when the loser of the previous goal depresses his service button. The ball will move away from the kickoff point with a randomly selected angle but always towards the goal of the winner of the previous goal.

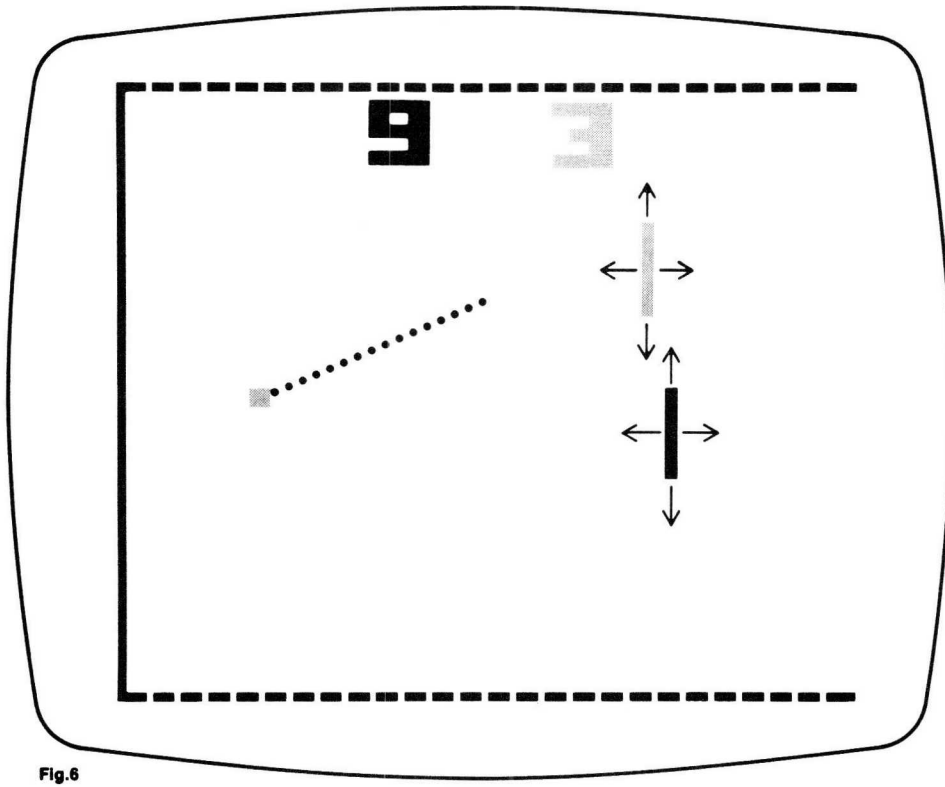


Fig.6

Squash

This game uses a playing area as shown in Fig. 6. Each player can move over the whole court. The game will start when the player whose service it is, depresses his service button. The ball moves off with a random angle toward the front wall. The color of the ball will change to the color code of the next player to hit the ball. Should the wrong player intercept or be hit by the ball it will be considered a fault. Points will only be given if won on player's own service. Points won on opponents serve will only cause a service change.

Practice

This game is a single player squash (See Fig. 7). The right score counts the number of successive hits in the current game (to a maximum of 15), the left score the number of volleys played.

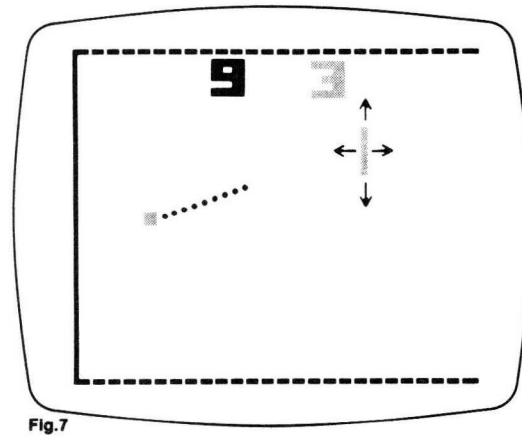


Fig.7

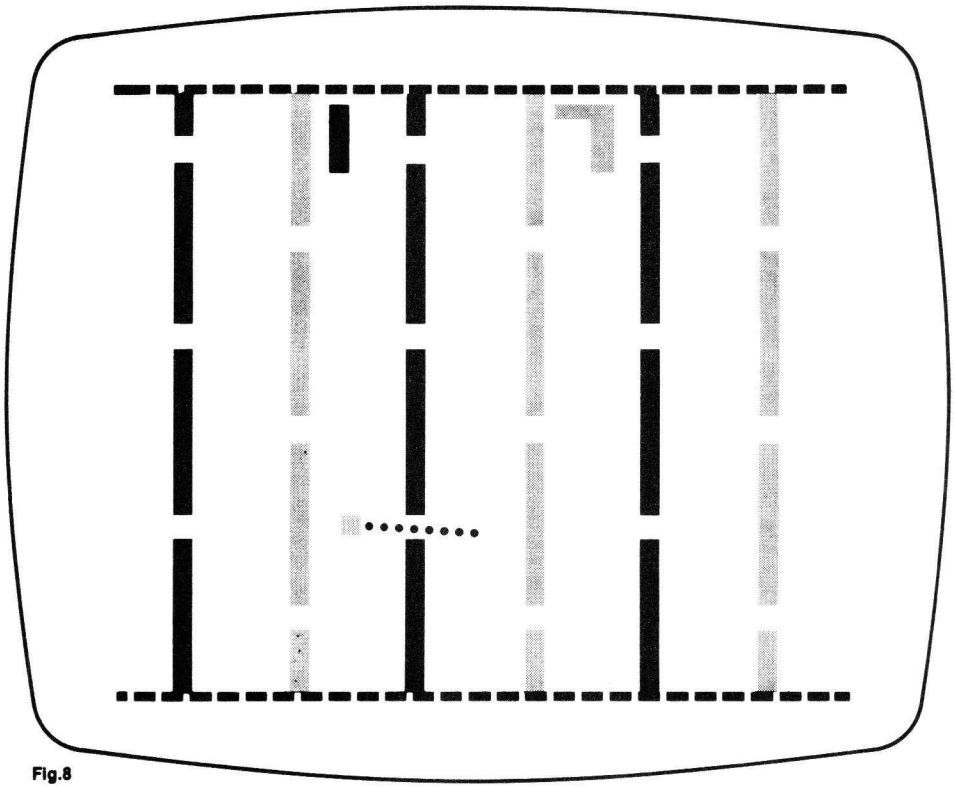


Fig.8

Gridball

This game uses a playing area as shown in Fig. 8. Each player has three sets of vertically moving barriers to block the ball from approaching his end and opening in the barriers to permit the ball to advance toward the opponent's end. The game starts when both players have depressed their service buttons. The ball moves away from the face off point with a random angle in either direction.

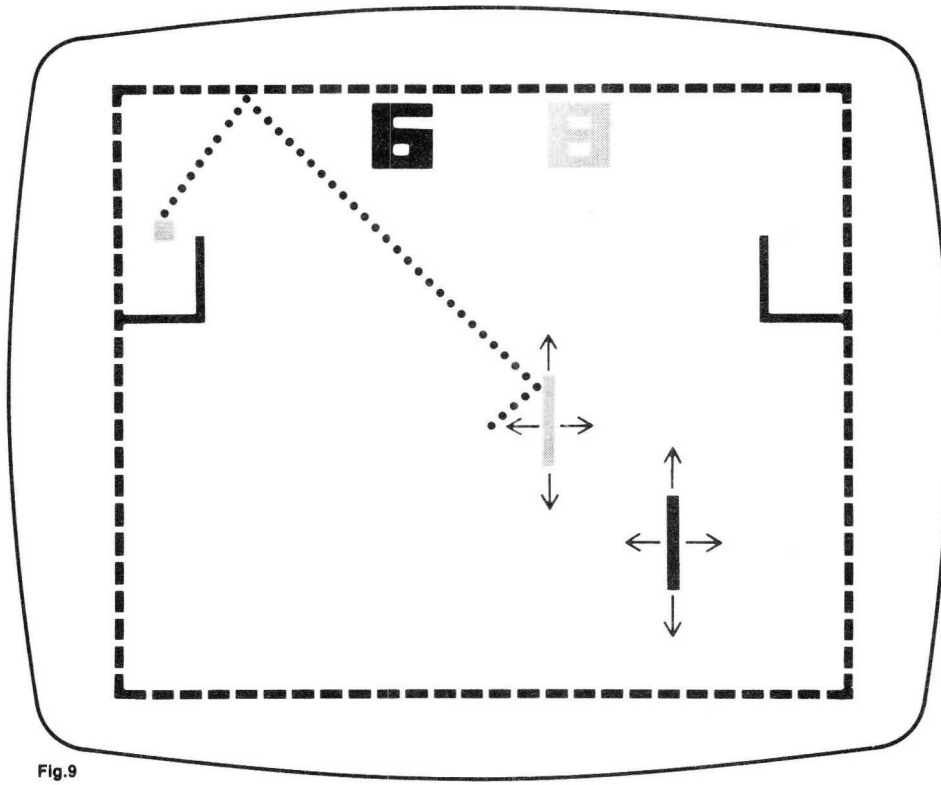


Fig.9

Basketball

The basketball games use the closed playing area as shown in Fig. 9. The players must deflect the ball and cause it to either the top of the goal to score. The game starts when both players depress the service buttons. The ball moves from the serve point with a random angle in either direction.

Basketball Practice

Basketball practice is a one player game which utilizes only the left basket as shown in Fig. 10. The right counter displays the number of hits the player makes without scoring while the left counter shows the number of baskets made. Play starts when the right serve button is depressed.

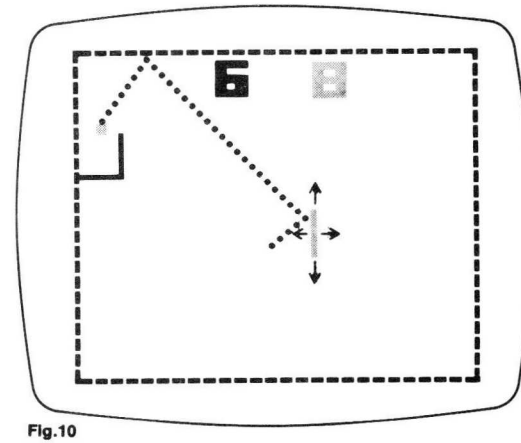


Fig.10

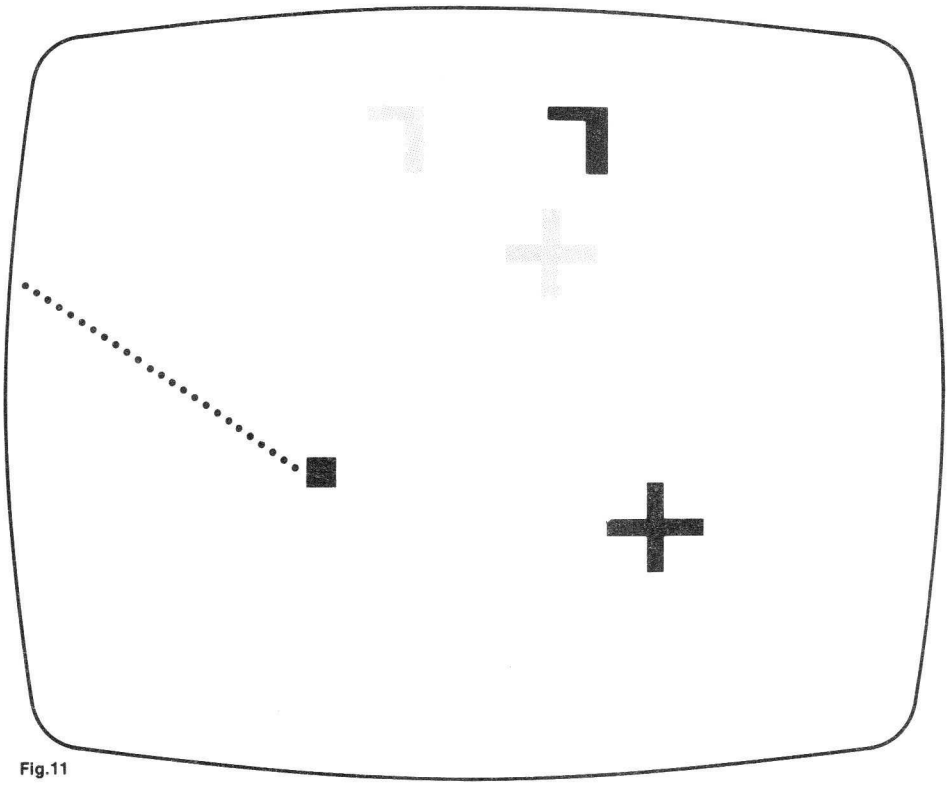


Fig.11

Two Player Target

The two player target game follows the same rules as the single player game except that both players control their own cursors and shot buttons. The left score displayed is for the left player and the right score displayed is for the right player. The target can only be shot at once on each traverse by either player but only recognizes the first hit. The first player to reach a score of 15 wins the game.

Single Player Target

The single player target game is a game in which the player moves a cursor displayed on the T.V. screen over a moving target and depresses the serve button for shots to be taken. The player has only one "shot" for each traversal of the screen by the target. Additional "shots" are ignored after the first shot on each traverse. The right score indicates the number of hits made and the left score indicates the misses. A count is made on either score on each traverse of the target across the screen. The target disappears when hit and the game ends when either of the scores displayed reaches 15.

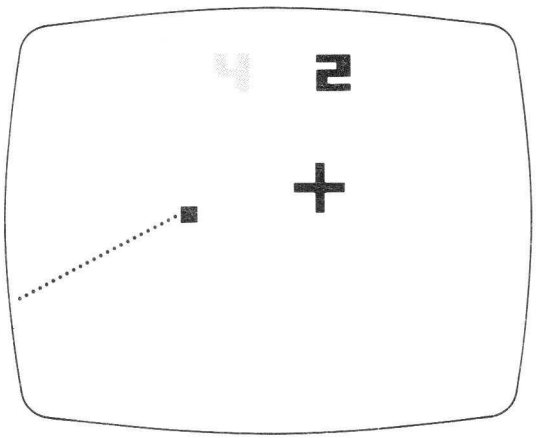


Fig.12

Color Processor

DESCRIPTION

The AY-3-8615 is a single N-Channel MOS circuit which processes video signals from any of the Gimini "8600" Game Series circuitry. It converts these video signals into a single color composite video output. The colors of the background and objects are selectively changed directly by the game select matrix. The circuit also provides, as an output, a buffered 3.579545 MHz clock for the game chip.

OPERATION

The AY-3-8615 provides a color composite video signal with color burst envelope and sync for input to the RF modulator of a TV game.

Sync: The sync input from any of the "8600" games is OR'ed with the video output of the color circuit. The sync amplitude level is compensated to ensure correct operation in color TV circuits.

Color Burst: A color burst signal, containing ten cycles of the 3.579MHz color reference is supplied after sync. The color phase of the burst is internally shifted by the game matrix inputs with respect to the phases of the background, right player and left player so that different colors may be rendered for each game. This color change may be affected with no external components.

Video Inputs: Seven video inputs are provided on the AY-3-8615. These are: field, background, color burst locator, left player, right player, blanking, and sync.

Video Output Mixer: With OR'ed sync, color burst and blanking, the video consists of background, field scores, right player, left player, and objects on a single output pin.

Grounded Select Input	Back-ground	Field	Right Player	Left Player
1. Sel1/Str1, Sel2/Str2, Sel2/Str4	Green	Yellow	Magenta	Blue
2. Sel2/Str1 Sel2/Str3	Blue	Cyan Blue	Dk. Blue	Red
3. Sel3/Str1, Sel3/Str2	Magenta	Lt. Red	Blue	Yellow
4. Sel1/Str2, Sel1/Str3, Sel1/Str4	Cyan Green	Green	Brown	Blue

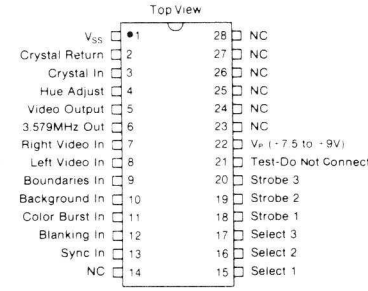
Colors may be adjusted for system variations by the chip hue control which varies the phase delay of the color outputs.

Luminesence Levels: The luminesence levels of the various signals in the composite video output have been selected to provide black and white compatibility. The field and left player signals are set to near white levels, the right to near black, and the background is set at a mid level to show gray.

Figure 1 shows the typical composite video waveform from the circuit.

In order to assure the correct video levels, a 2K variable potentiometer should be used to adjust the output to the min/max values specified for the modulator used.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



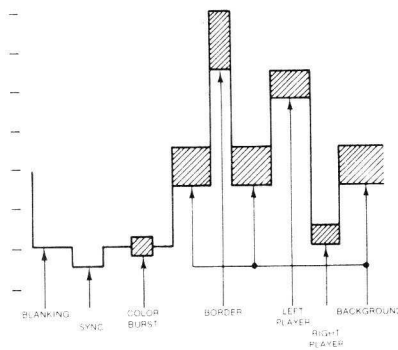


Fig. 1 COMPOSITE VIDEO OUTPUT

CLOCK INPUT

The AY-3-8615 is operated directly from a 3.579545 MHz crystal input. A variable capacitor with a range of 3 to 15 pF should be used to tune the crystal.

CLOCK OUTPUT

The AY-3-8615 generates low impedance 3.579545 MHz clock to directly drive the "8600" series game chips without external components.

Characteristics at +25° C	Min	Typ	Max	Units
Clock Input (Crystal)	—	3.579545	—	MHz
Video & Game Select				
Logic "0" (Select)	—	—	0.2	Volts
Logic "0" (Video)	—	—	1.0	Volts
Logic "1" (all)	V_P–2	—	—	Volts
Hue Adjust (External)	2.0	—	V_P	Volts
Video Output (2 K pot to V_P)	—	1K	—	Ω
Clock Output Rise & Fall Time	—	100	—	ns
Supply Current	—	—	25	mA

TV GAMES

Battle

FEATURES

- Two independently controllable tanks
- Tank explosion and sounds when hit by shell or mine
- Exploding mines
- Shell firing and burst video and sound
- Three forward and reverse tank speeds
- 32 rotational angles
- Fixed terrain barriers
- Realistic tank sounds
- Automatic on-screen scoring
- Scores color keyed to player
- 625 Line (AY-3-8710) and 525 Line (AY-3-8700-1) Versions
- TV raster generator

DESCRIPTION

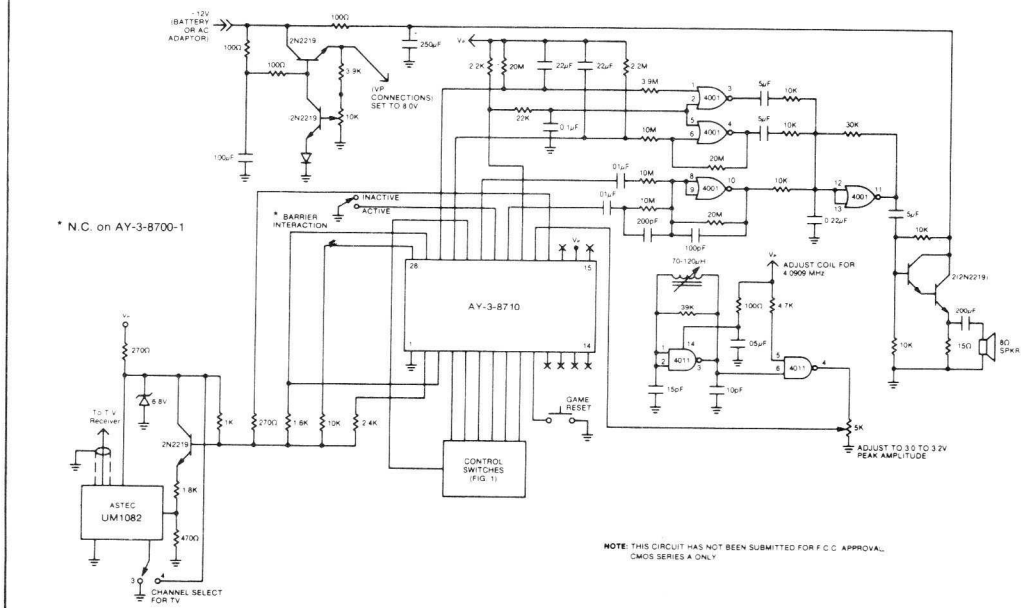
The AY-3-8710/8700-1 circuit is a "tank battle game" and has been designed for two players where each player has a completely steerable tank with forward and reverse speed control and a firing button. Barricades and mines are in the battlefield to retard the games progress while under battle conditions. The object of the game is to score as many hits on the enemy tank as possible. The circuit is designed to be used with standard domestic television receivers. The AY-3-8710/8700-1 is manufactured in a 28 pin dual-in-line package and can be used in battery systems with a minimum number of components to provide a complete game.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

* N.C. on AY-3-8700-1; do not connect anything to this pin.

SYSTEM DIAGRAM



PIN FUNCTIONS

Sound Outputs

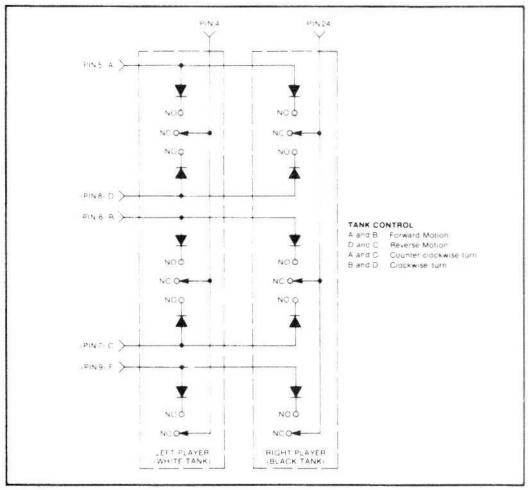
Tank 1 motor
Tank 2 motor
Bearing and track squeak
Explosion envelope
Gun fire envelope
Explosion and gun fire noise

Power Input

V_{CC} positive voltage
V_{SS} substrate (negative) voltage

Control Inputs and Outputs

A Input
B Input
C Input
D Input
F Input
Control strobe 1
Control strobe 2
Game reset



Video outputs

Right player tank, shell, shell burst, score and mines.
Left player tank, shell, shell burst, score and fixed barriers.
Blanking
Background
Sync
Color burst locator

All signals are present in the circuit to generate a composite video signal with a sync waveform which includes composite blanking equalization pulses and color burst locator. This video signal provides the input to the game RF modulator.

The luminance levels are set by the ratios of the resistor shown in the System Diagram. This output configuration provides maximum flexibility to the user.

Five outputs are provided; sync, right player, left player, background and blanking. The right player output includes the tank symbol, right player score, shells fired by the right tank, shell burst from right tank shells and mines. The left player output includes the left tank, left player score, shells fired by the left tank, left tank shell bursts and fixed barriers.

One tank is displayed in white, one in black, and the background in gray.

The blanking and black outputs are shown connected to a single resistor since the modulation level is approximately the same for both.

In addition to the preceding five outputs, a color burst locator is provided to enable users who wish to provide a color background to locate the color burst envelope at the correct waveform position after the sync output.

Clock Input

4.09MHz clock input—This is the only clock required for black and white operation. A typical 4.09MHz oscillator circuit with control input is shown in the System Diagram.

ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

Maximum Ratings

Voltage on any pin with respect to V_{SS} ..... 0 to 12V
Storage temperature range ..... −20°C to 70°C
Ambient Operating Temperature Range ..... 0° to +40°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (Unless stated otherwise)

V_{CC} = +6.0 to 7.0 volts (subject to further characterization)
V_{SS} = 0 volts

Characteristics at 25°C, V_{CC}=6 Volts	Min	Typ	Max	Units	Conditions
Clock input frequency (Duty Cycle 50% ± 5%)	—	4.0909	—	MHz	
Rise and Fall Times	—	—	40	ns	
Logic '0'	0	—	0.5	Volts	
Logic '1'	3.0	—	4.0	Volts	
Input Current	—	—	100	μA	
Outputs: Pins 2, 3, 4, 17, 18, 20, 24, 25, 26, 27, 28 (Open drain)	—	—	300	Ω	V_{OUT} = 0.5V, 4.7K to V_{CC}
Outputs: Pins 21, 23 (push pull)					
Logic '0'	0	—	0.5		
Logic '1'	V_{CC} −2	—	V_{CC}	Volts	
Inputs: Pins 5, 6, 7, 8, 9					
Logic '1'	V_{CC} −2	—	V_{CC}	Volts	See System Diagram for correct circuit
Maximum supply current	—	—	75	mA	

TV GAMES

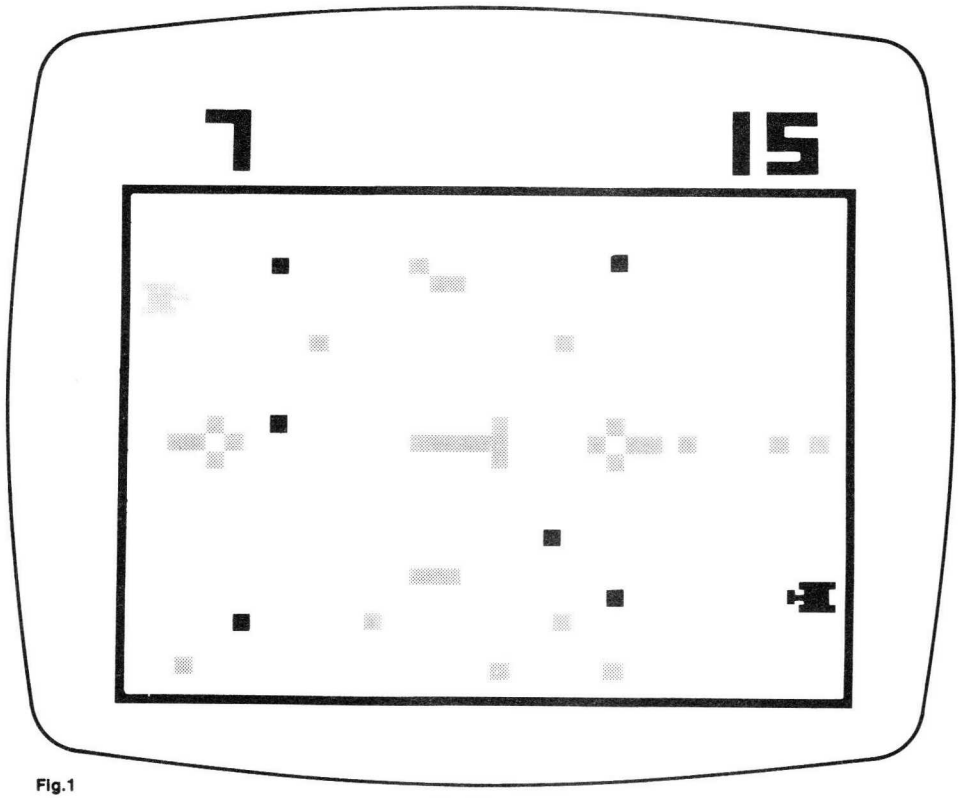


Fig.1

Battle

DISPLAY SYMBOLS AND CONTROL

TANKS

Control — The tanks are controlled by connecting the appropriate strobe outputs to the inputs A, B, C, D, or F. Forward motion is achieved when both the A and B inputs are connected to the strobe. On connection, the tank will advance in low speed. If the connection is held, the medium speed will select after one half second. After another one half second of connection, high speed is selected. Breaking the connection when any speed is achieved will cause the tank to remain at the selected speed. The controls should each be single pole double throw center off momentary switch. To stop the tank, the controls should be momentarily contacted opposite to tank direction.

The tank can be made to go through the three reverse speeds at one half second intervals by connection of the C and D inputs to the appropriate strobe output. Tank rotation in a clockwise (right turn) direction is caused by connection of the B and D inputs to the strobe while counterclockwise (left turn) direction is caused by connection of the A and C inputs to the strobe. The tanks are able to turn while either in forward or reverse speed and rotate when stationary.

Tank Details

Definition and resolution	64 bits (8x8) or 8/100 of TV screen width
Orientations	32
Direction of travel and firing angles	32
Forward speeds	3
Reverse speeds	3
White tank exhibits line displacement on top.	

SHELLS

Firing — connection of the gun fire input to a strobe output with a SPST normally open pushbutton switch causes the firing of a tank gun and release of a shell. The firing rate is approximately once every four seconds and the refire requires release of the button and redepression. Depression made during the four second interfiring time will initiate fire sound but will not initiate shell.

When a shell is in flight, the rotation of the tank will cause the shell to follow a curved trajectory in the direction of tank rotation.

Range — the range of a shell is approximately 2/3 of the screen length or width dependent on firing angle.

Size — the shell is a 1x1 bit dot.

BATTLEFIELD BARRIERS

Fixed Terrain Barriers — Twenty two fixed terrain barriers are on the battlefield to provide protection from shells. Tanks cannot pass through barriers when Barrier Interaction is selected (AY-3-8710 only).

Mines — six mines are distributed on the battlefield. Hitting a mine with a tank causes the tank to explode and become stationary with its gun inactive for a period of 2 to 4 seconds. The mine then vanishes for the duration of battle. A mine being hit scores for the enemy tank.

Barrier Sizes — barriers and mines are 4x4 bit square minimum size.

EXPLOSIONS (VIDEO)

Shell Bursts — shell burst patterns are produced when a shell is at end of range or when the shell makes contact with a barrier.

Tank Explosions — a tank will explode and fragment momentarily when a tank hits a mine or is struck by a shell.

SCORING

Separate scores, color coded to the tank, are indicated for each player. A player's score is incremented when his tank scores a hit on his opponent's tank or the opponent's tank hits a mine. The game ends when the score flashes at a 1 Hz rate and no further hits are recorded.

RESET

The game is reset by momentarily connecting Reset input to V_{SS} through an SPST pushbutton. On reset, the scores are cleared to zero, mines replaced and the tanks reset to the upper left and lower right corners in the stationary condition.

SOUND OUTPUT

GENERAL

The sound outputs produced by the circuit are low frequency typical of those associated with heavy equipment motors and of explosions. It is recommended that the sound be reproduced through the TV set or in a large speaker so the full richness of the sound can add the proper atmosphere to the game.

ENGINE SOUND

Outputs are provided for the engine sound associated with each tank. Four motor frequencies are provided; three for the three speed ranges and one for stationary condition. A typical sound circuit for filtering each output is shown in the System Diagram.

GUN FIRE SOUND

Gun fire sounds are produced mixing the noise output with the fire output. The fire output should be filtered and mixed with the noise output as shown in the System Diagram.

SHELL BURST AND TANK EXPLOSION SOUNDS

Shell burst sounds are produced when a shell reaches the end of its range or hits a barrier, a border, or the enemy tank. Tank explosion sounds are produced when a tank hits a mine or is struck by a shell. A typical circuit is shown in the System Diagram.

SPECIAL CONSIDERATIONS FOR AY-3-8700-1

1. Both tanks should be kept in the visual area of the screen. They can travel outside the boundary and not return under certain conditions.
2. Upon scoring, the black tank rotates and the white tank does not. This gives a theoretical advantage to the white tank which is overcome by the approx. four second interval between shots.
3. Mines may periodically disappear upon interaction with tanks.
4. Borders vary in width from chip to chip.
5. Both tanks may have varying shape.

SPECIAL CONSIDERATIONS FOR AY-3-8710

There are certain danger areas (see Fig. 2) that the tanks should avoid. If a tank enters these danger areas, it is possible for it to get trapped in the border. The game is over at that point and the opposing tank is recognized as the winner. When interaction is selected (tanks cannot drive thru barriers), it is possible for tanks to get trapped in barriers. If this occurs, the interaction should be momentarily deselected to allow the trapped tank to free itself. During the course of play, it is possible for the tanks to get locked together in a way in which they cannot be separated by use of either set of controls. Should this occur, the game must be reset and started over again.

Upon reset a random explosion may occur, which may be visible below the bottom border. This has no effect on the play of the game. During the course of play either tank may occasionally misfire, ie, the shell may appear to explode in a position to which the player is not aiming, or the shell may appear to not be fired from the tank. This does not affect the play of the game. There is a "misfire zone" shown as the cross hatched area in Figure 2. The black tank will misfire when its gun falls within the misfire zone and the tank is facing towards the left at any of the angles shown.

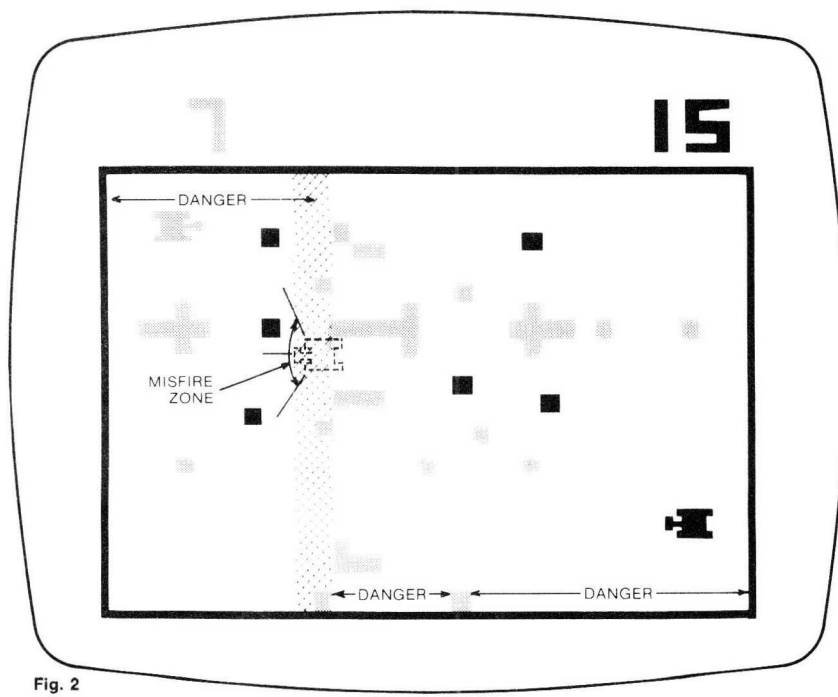


Fig. 2

Motorcycle

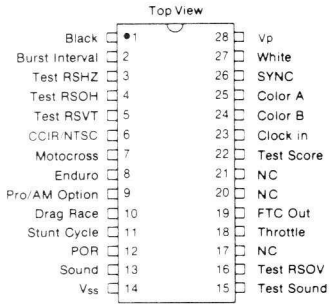
DESCRIPTION

Motorcycle is a game for one player who controls the speed of a motorbike and rider. At the start of each game, the motorbike and rider are stationary at the upper left-hand side of the TV screen. As the player turns the throttle controller, the motorbike and rider move across the screen on track 1. The motorbike sound starts with the bike movement and as the bike and rider accelerate, the motorbike sound reflects these speed changes. The motorbike wheels have an appearance of rotating at a speed also related to the throttle setting.

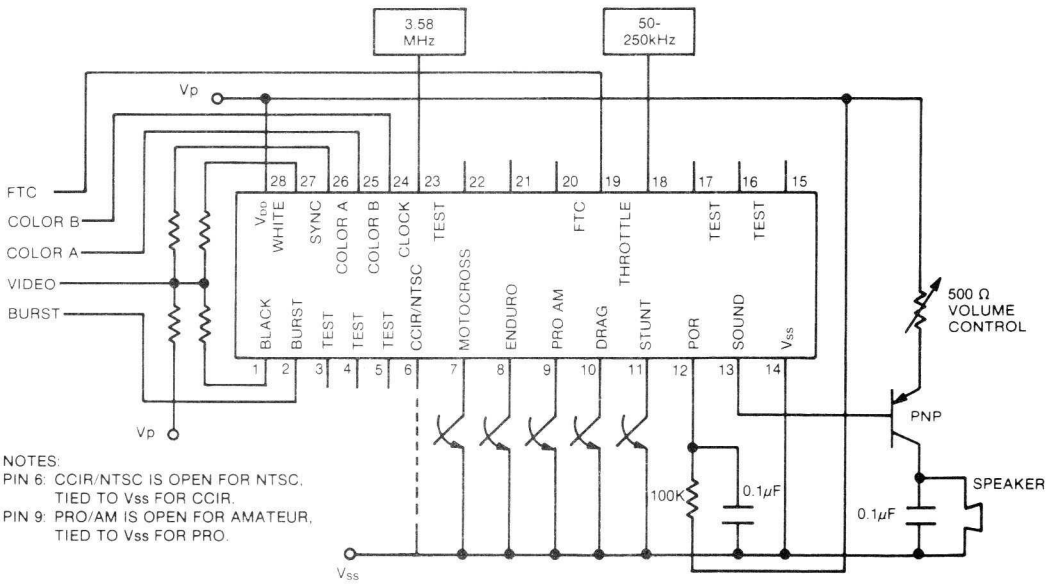
At the end of track 1, the bike and rider reappear on track 2 at the left-hand side, and likewise at the end of track 2 the bike appears on track 3 at the left-hand side of the screen. The movement of the bike and rider on track 3 to the right edge of the screen will cause a reinitialization of the bike and rider at the left of the screen on track 1. There will be no movement until the throttle is reset to a slow speed and then increased. A system diagram is shown below.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	Black	The output of this pin is the video signal of ramps, tracks and the composite blanking.
2	Burst Interval	The output of this pin is the color time slot which occurs after the SYNC signal during Horizontal Blanking.
3	Test RSHZ	Functional test input. Normally open pin NOT to be used as a tie point.
4	Test RSOH	Functional test input. Normally open pin NOT to be used as a tie point.
5	Test RSVT	Functional test input. Normally open pin NOT to be used as a tie point.
6	CCIR/NTSC	This input is provided with an internal resistor pull-up to V_{DD}. If this input is tied to V_{SS}, NTSC (262 vertical lines) is selected. If this input is tied to V_{DD} or allowed to float, CCIR (312 vertical lines) is selected.
7	Motocross	This pin is provided with an internal resistor pull-up to V_{DD}. If this input is momentarily connected to V_{SS}, this game will be selected. Otherwise, this pin is normally open.
8	ENDURO	This pin is provided with an internal resistor pull-up to V_{DD}. If this input is momentarily connected to V_{SS}, this game will be selected. Otherwise, this pin is normally open.
9	PRO/AM Option	This pin is provided with an internal resistor pull-up to V_{DD}. If this input is switched to V_{SS}, the PRO (hard) mode is selected. Switching this pin to V_{DD} or allowing it to float selects the AM (easy) mode.
10	Drag Race	This pin is provided with an internal resistor pull-up to V_{DD}. If this input is momentarily connected to V_{SS}, this game is selected. This pin is normally open.
11	Stunt Cycle	This pin is provided with an internal resistor pull-up to V_{DD}. If this input is momentarily connected to V_{SS}, this game is selected. This pin is normally open.
12	POR	The input to this pin is provided by an external RC network which generates a power-on reset signal. This network consists of 100K resistor from this pin to V_{DD} and a 0.1μF capacitor from this pin to V_{SS}.
13	Sound	The output of this pin are the sounds for the bike engine, bus hit, crash, screech, and a good jump. This output is designed to drive a PNP transistor which in-turn drives the game speaker.
14	V_{SS}	This input is the negative power supply.
15	Test Sound	Functional test input. Normally open pin NOT to be used as a tie point.
16	Test RSOV	Functional test input. Normally open pin NOT to be used as a tie point.
17	NC	Not connected.
18	Throttle	The input to this pin is an oscillator signal for controlling the motion of the bike and rider.
19	FTC Out	The output of this pin controls the intensity of the display. When this output is V_{DD}, it indicates that the game has not been initiated, no motion exists on the screen, and the intensity is at a reduced level.
20	NC	Not connected.
21	NC	Not connected.
22	Test Score	Functional test input. Normally open pin NOT to be used as a tie point.
23	Clock In	The input to this pin is the 3.58 MHz oscillator.
24	Color B	See TABLE 1 Below
25	Color A	See TABLE 1 Below
26	SYNC	This pin provides the combined output of horizontal SYNC or vertical flyback.
27	White	The output of this pin is the video output signal for the bike, buses, score and obstacles.
28	Vp	This input is the positive power supply.

Table 1

	Color Pin A	Color Pin B
Motocross (Green)	Off Fet	$\overline{Clk}$
Enduro/Stunt Cycle (Blue)	$\overline{Clk}$	Off Fet
Drag Race (Red)	Clk	Clk
Burst	Clk	Off Fet
Sync	Off Fet	Off Fet

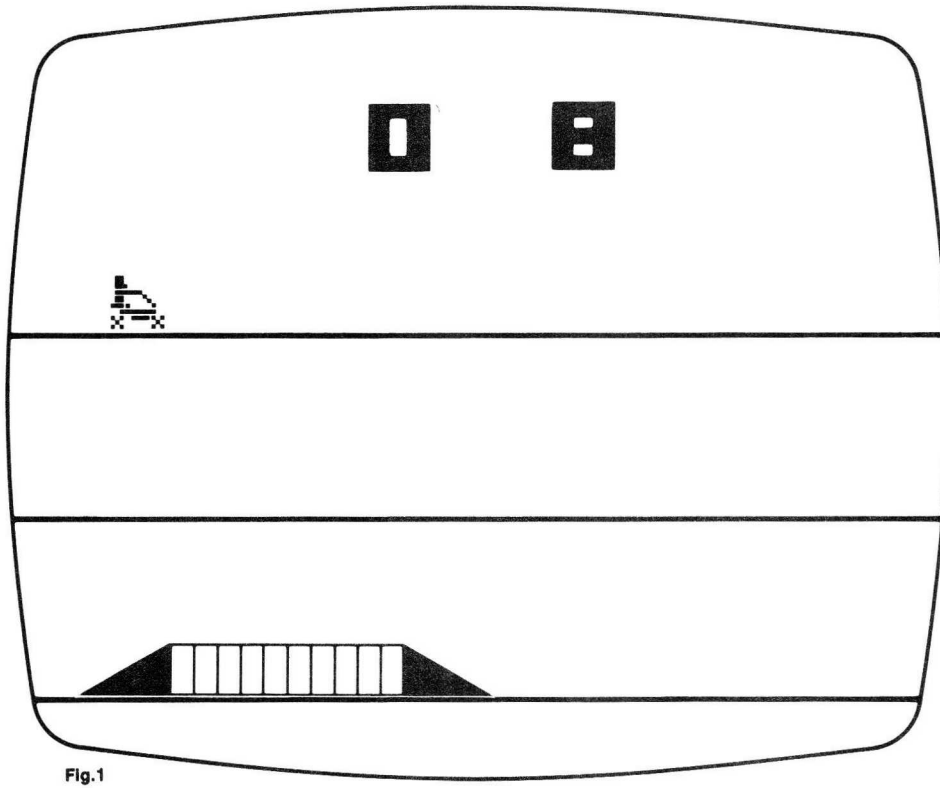


Fig.1

Stunt Cycle

The object of this game is to control the throttle speed to properly jump the ramp and buses located on track 3. The game begins with 8 buses and with each successful jump over the ramp and buses, an additional bus appears. The game is over when the maximum number of errors has been reached, which is 3 or 7 errors depending on the position of the PRO/AM switch. The game is then started by reselecting the Stunt Cycle game input.

Errors are caused by accelerating too rapidly, insufficient speed to clear the buses, or landing too far past the back ramp after the jump. The bike and rider flip upside down and a screeching sound indicates an error. The score records the number of errors in the first digit and the number of displayed buses in the next two digits.

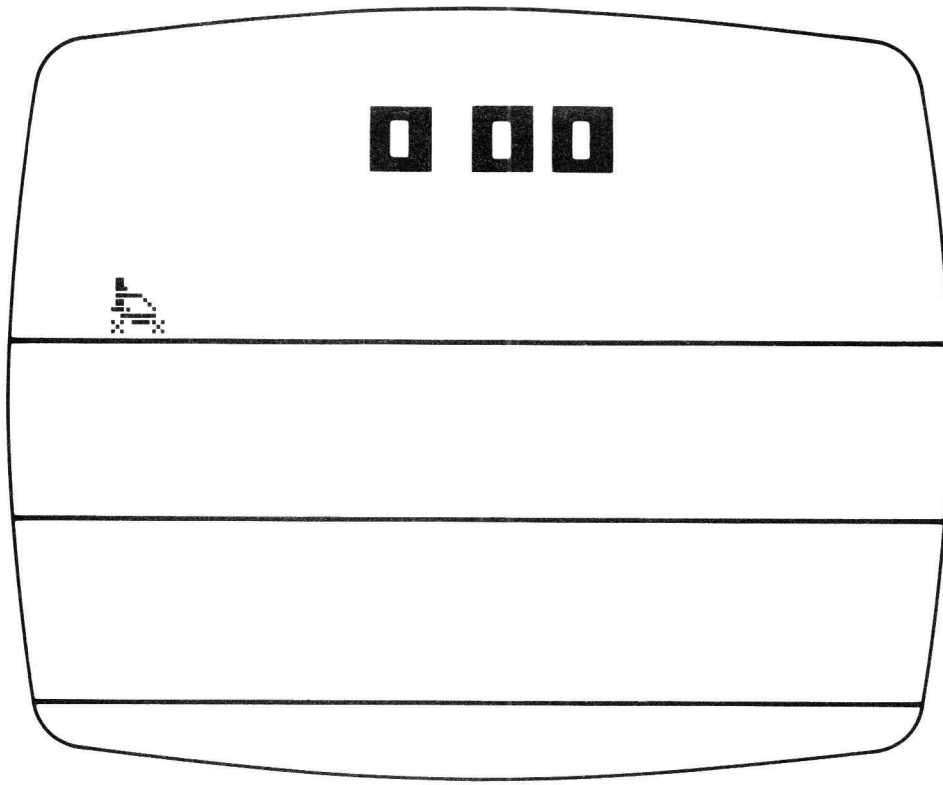


Fig.2

Drag Race

The object of this game is to reach the end of track 3 in the shortest time. The three-digit score is automatically reset as the rider first begins to move on track 1 and the score is incremented until the game is over. The score appears centered on the screen above track 1, and the score remains until the start of the next game.

Drag Race requires a speed shifting to achieve the lowest time scores. As the throttle speed is increased and the rider begins to move, the bike object is in speed one and moves at a set rate across the screen. The only way to accelerate the bike object motion is to return the throttle to a "slow" position and then turn to a "fast" position. This shifting procedure will move the bike into speed 2 and the object will go across the screen at a faster rate. Another "shift" will allow speed 3.

A PRO/AM option switch is provided to select a difficulty factor. In the hard mode, a crash occurs if the player tries to increase the throttle speed too rapidly. A crash will flip the bike and rider upside down and the sound will be a high-pitch screech. At the end of the crash, the bike and rider are reinitialized on track 1 and the score reset. In the easy mode, no crash is allowed.

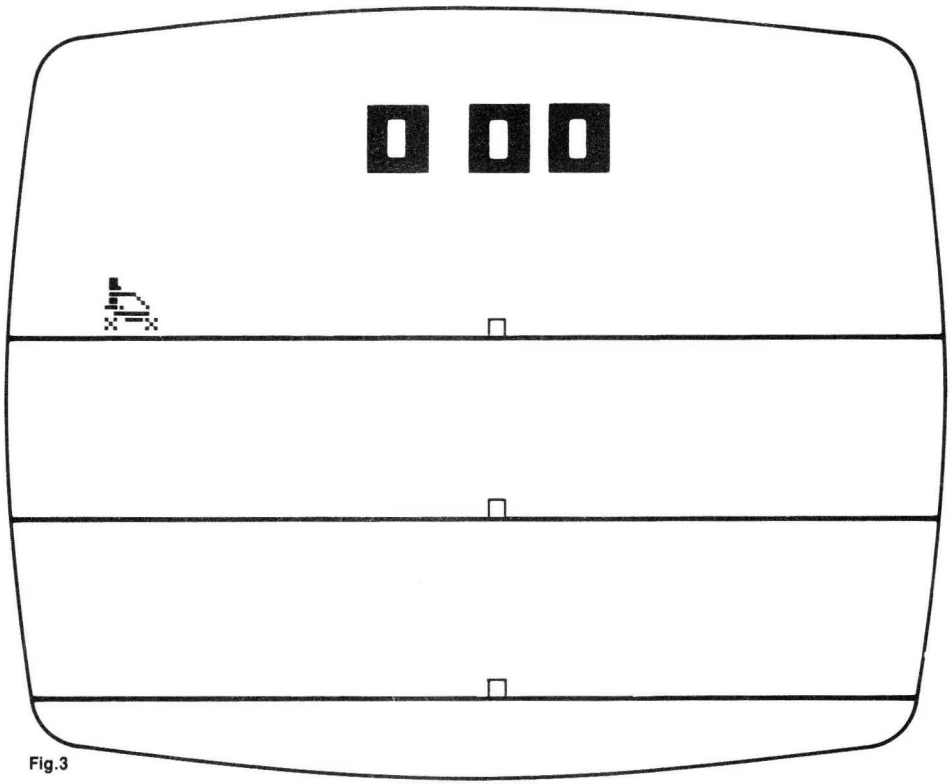


Fig.3

Motocross (Easy Mode)

As the throttle speed is increased, the bike and rider move across track 1 at a rate determined by the throttle controller setting. Motocross has no speed shifting. Located on each of the three tracks are obstacles. The easy/hard option switch selects the number of obstacles per track. The easy mode has one obstacle per track and the hard mode has two obstacles per track.

The object of this game is to traverse the three tracks in the shortest time, doing a wheelie over each obstacle. The score counters record the run time in the same manner as the Sprint game.

In Motocross, the crash is not caused by accelerating too rapidly. The crash is caused by not doing a wheelie over an obstacle. In the wheelie position, the bike will have the front wheel lifted off the track. A crash into an obstacle will flip the bike upside down and produce the screech sound. The score is reset at the end of the crash.

Motocross (Hard Mode)

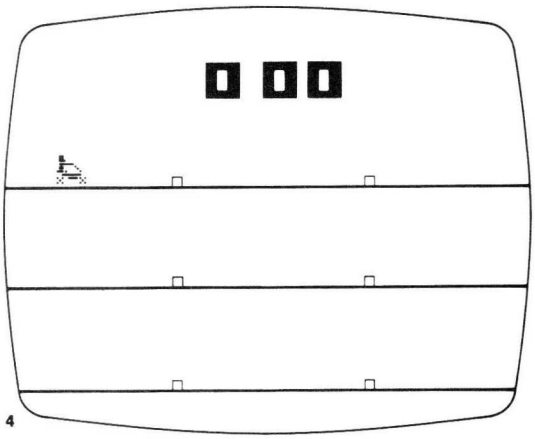


Fig. 4

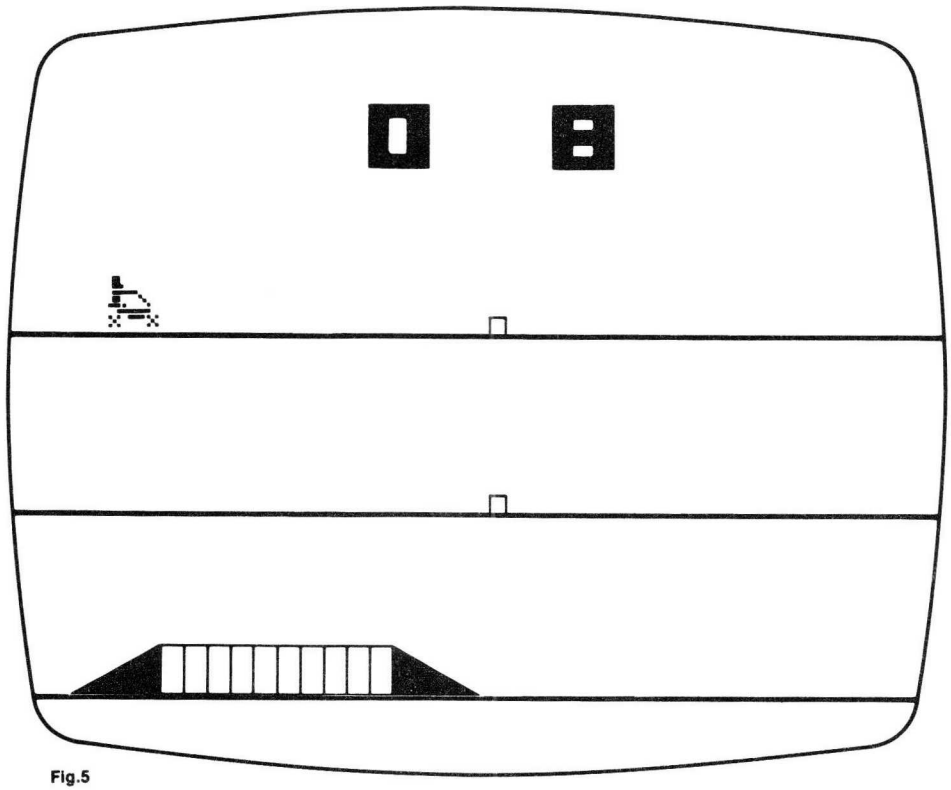


Fig.5

Enduro (Easy Mode)

This game is similar to Stunt Cycle with the addition of obstacles on track 1 and track 2. The object of Enduro is to do a wheelie over each obstacle and then adjust the throttle for the correct speed to jump the buses on track 3. The PRO/AM option switch selects 2 obstacles per track and allows 3 errors per game in the hard mode, and 1 obstacle per track and 7 errors per game in the easy mode. Errors are caused by accelerating too rapidly, not in wheelie position over the obstacles, insufficient speed to clear the buses, or landing too far past the back ramp after the jump. The score records the number of errors and the number of buses displayed the same as in the game of Stunt Cycle.

Enduro (Hard Mode)

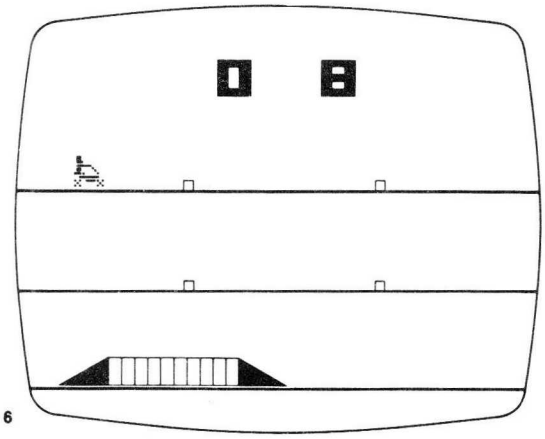


Fig. 6

MICRO ELECTRONICS

PROGRAMMABLE TV GAMES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
GIMINI ECONOMY "8600" PROGRAMMABLE GAME SYSTEM	With a single AY-3-8615 "resident processor" chip in the game console, the GIMINI Economy "8600" minimizes system cost. Each game cartridge provides full color games with realistic sounds and scoring.	AY-3-8615	7-64
		AY-3-8603	7-68
		AY-3-8603-1	7-68
		AY-3-8605	7-69
		AY-3-8605-1	7-69
		AY-3-8606	7-70
		AY-3-8606-1	7-70
		AY-3-8607	7-71
		AY-3-8607-1	7-71
		AY-3-8610	7-72
		AY-3-8610-1	7-72
		AY-3-8765	7-73
GIMINI CHALLENGER "8950" PROGRAMMABLE GAME SYSTEM	BASIC COMPONENTS: A complete microprocessor programmable game with only 3 LSI chips (plus standard RAM), the GIMINI Challenger "8950" is ideal for sports games and games of chance and mental skill.	CP1610	7-86
		AY-3-8950	7-78
		AY-3-8950-1	7-78
		RO-3-9501	7-92
		2112A	7-99
	OPTIONAL COMPONENTS: The basic "8950" system can be expanded to include additional ROM and RAM, and to add complex sound generation.	RO-3-9500	7-92
		2112A/2114	7-99
		AY-3-8910	7-100
GIMINI DELUXE "8900" PROGRAMMABLE GAME SYSTEM	BASIC COMPONENTS: A complete microprocessor programmable game with only 5 LSI chips, the GIMINI Deluxe "8900" offers the capability for maximum game flexibility with detailed graphics definition and manipulation.	CP1610	7-107
		AY-3-8900	7-107
		AY-3-8900-1	7-107
		RO-3-9502	7-108
		RO-3-9503	7-108
		RA-3-9600	7-108
	OPTIONAL COMPONENTS: The basic "8900" system can easily be expanded to include additional games plus software-controlled graphics interaction, complex sound generation, and supplementary peripherals.	RO-3-9500	7-109
		2112A/2114	7-109
		AY-3-8910	7-109
		AY-3-8915	7-109
		AY-3-8920	7-109
		IOB 1680	7-109

GIMINI Economy "8600" Programmable Game System

The GIMINI "8600" system consists of a main console designed for either NTSC (ref. Fig. 2) or CCIR (ref. Fig. 3) compatibility, and plug-in cartridges which each contain a "dedicated" game chip.

DESCRIPTION

The console consists of a resident AY-3-8615 game/color processor, an R.F. video modulator, a calculator type keyboard for game selection, a set of three skill select switches, and a game reset switch. Attached to the console are the player controllers which can consist of joysticks or a variety of controls suited to the game.

The console need never be opened once in operation; all changes to the system are plugged in externally. The cartridges and controls are the only items that are altered to give the Economy 8600 system new game characteristics.

The block diagram shows the basic system with its expandability. Detailed console schematics for NTSC color and CCIR black and white are shown in Figs. 2 and 3 respectively.

SECTION A

There are three switches that will allow skill selections. These skills will be determined by the specific game cartridge and will control speeds, sizes and shapes of objects in any particular game cartridge. A fourth switch acts as game reset.

SECTION B

The game selections will be made by a maximum of ten momentary switches similar to the calculator keyboard. Again the number of games is determined by the cartridge.

SECTION C

The controls are always in pairs to allow for two players. Depending on the game cartridge, a variety of controls may be used. Basically most games can be controlled by resistance joysticks. If controls are remote, the connectors used should be a minimum of six pins each to allow for game flexibility.

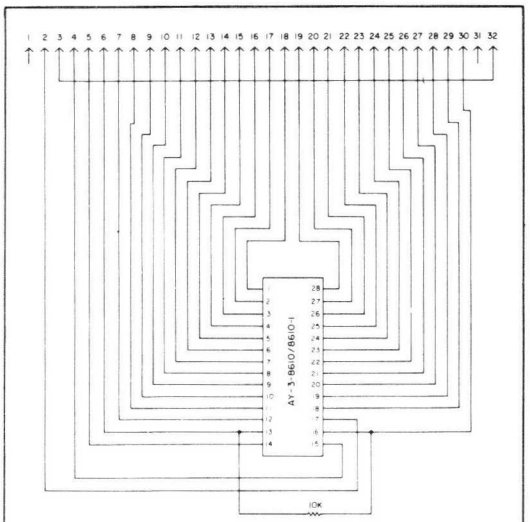
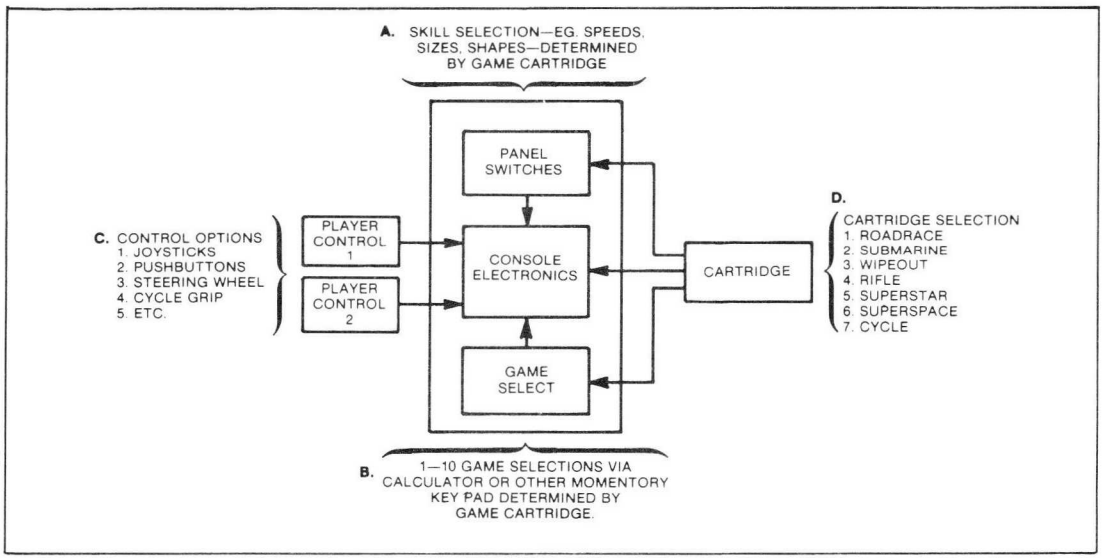


Fig. 1 AY-3-8610/8610-1 CARTRIDGE

SECTION D

The cartridges will all be compatible with the console and a variety will be offered. Each cartridge will give the game a completely new objective. The cartridge should have a minimum of 34 pins to allow for special connections such as sound effects, etc., and remain compatible with the system.

Fig. 1 illustrates as an example the straightforward layout for the AY-3-8610/8610-1 Supersport game cartridge.



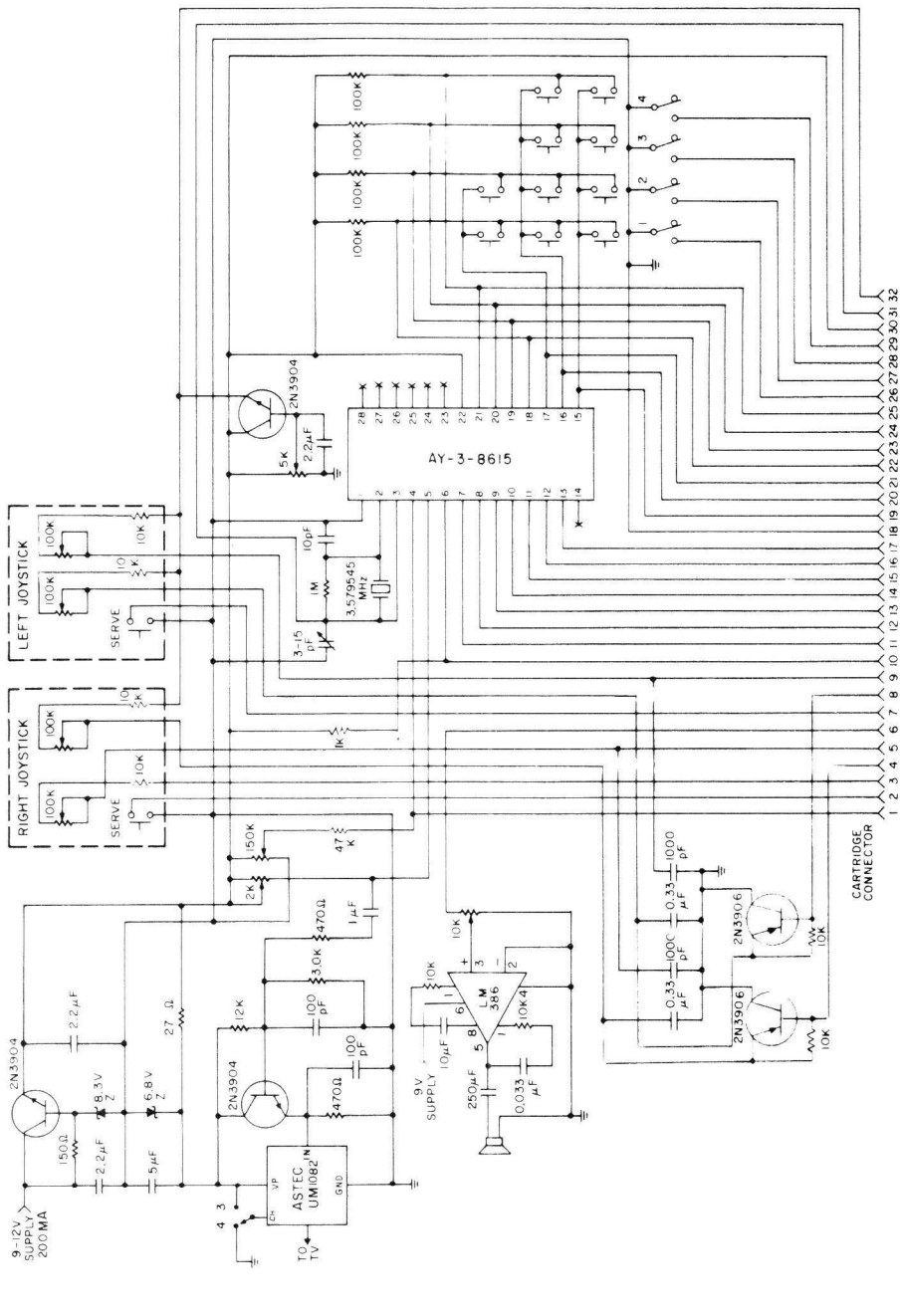


Fig. 2 GIMINI ECONOMY "8600" CONSOLE: NTSC COLOR

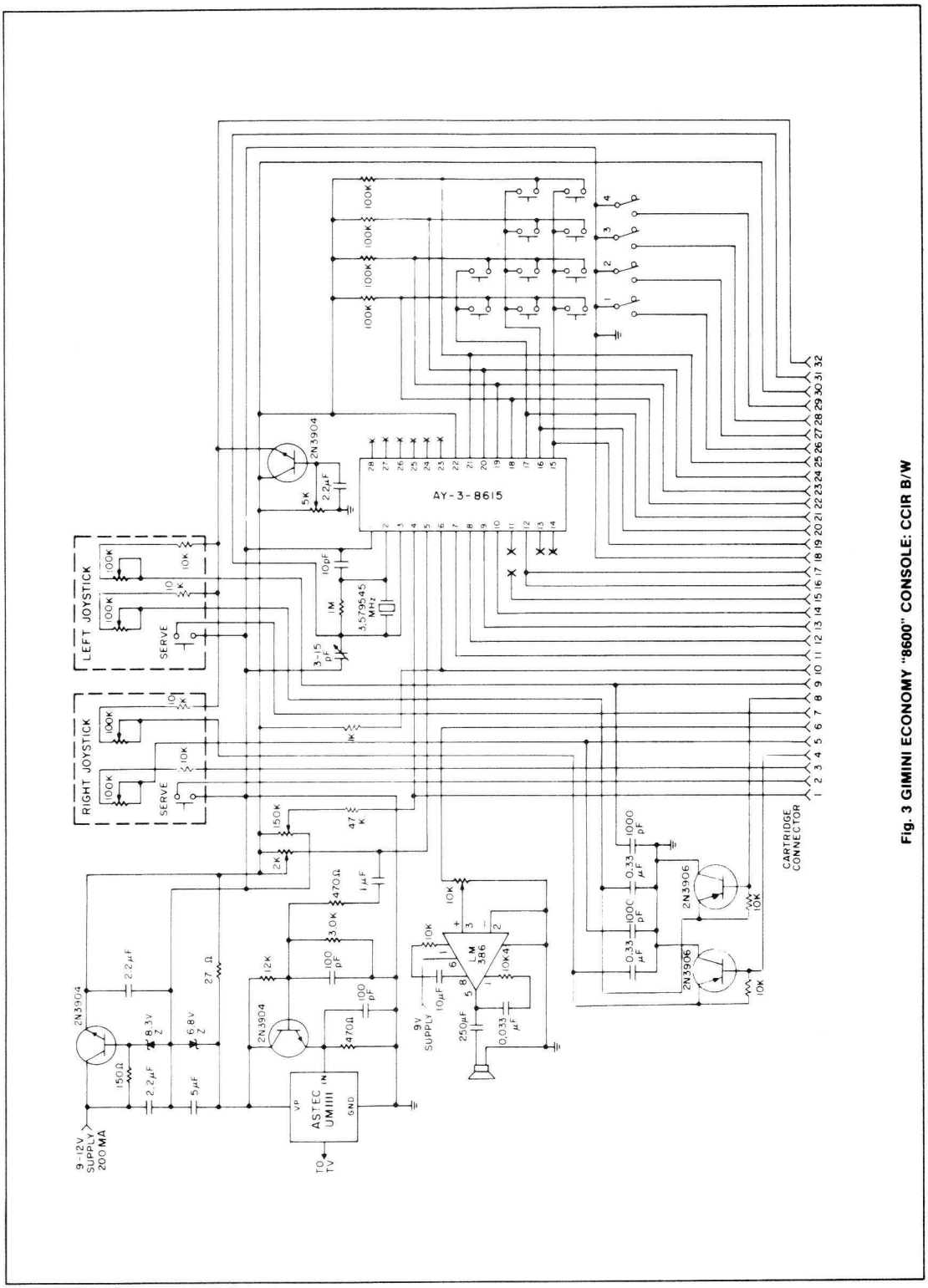


Fig. 3 GIMINI ECONOMY "8600" CONSOLE: CCIR B/W

AY-3-8615 RESIDENT PROCESSOR

DESCRIPTION

The AY-3-8615 is a single N-Channel MOS circuit which processes video signals from any of the Gimini "8600" Game Series circuitry. It converts these video signals into a single color composite video output. The colors of the background and objects are selectively changed directly by the game select matrix. The circuit also provides, as an output, a buffered 3.579545 MHz clock for the game chip.

OPERATION

The AY-3-8615 provides a color composite video signal with color burst envelope and sync for input to the RF modulator of a TV game.

Sync: The sync input from any of the "8600" games is OR'ed with the video output of the color circuit. The sync amplitude level is compensated to ensure correct operation in color TV circuits.

Color Burst: A color burst signal, containing ten cycles of the 3.579MHz color reference is supplied after sync. The color phase of the burst is internally shifted by the game matrix inputs with respect to the phases of the background, right player and left player so that different colors may be rendered for each game. This color change may be affected with no external components.

Video Inputs: Seven video inputs are provided on the AY-3-8615. These are: field, background, color burst locator, left player, right player, blanking, and sync.

Video Output Mixer: With OR'ed sync, color burst and blanking, the video consists of background, field scores, right player, left player, and objects on a single output pin.

Grounded Select Input	Back-ground	Field	Right Player	Left Player
1. Sel1/Str1, Sel2/Str2, Sel2/Str4	Green	Yellow	Magenta	Blue
2. Sel2/Str1 Sel2/Str3	Blue	Cyan Blue	Dk. Blue	Red
3. Sel3/Str1, Sel3/Str2	Magenta	Lt. Red	Blue	Yellow
4. Sel1/Str2, Sel1/Str3, Sel1/Str4	Cyan Green	Green	Brown	Blue

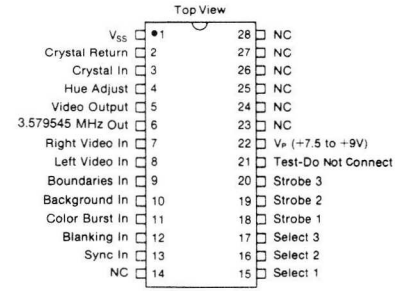
Colors may be adjusted for system variations by the chip hue control which varies the phase delay of the color outputs.

Luminescence Levels: The luminescence levels of the various signals in the composite video output have been selected to provide black and white compatibility. The field and left player signals are set to near white levels, the right to near black, and the background is set at a mid level to show gray.

Figure 4 shows the typical composite video waveform from the circuit.

In order to assure the correct video levels, a 2K variable potentiometer should be used to adjust the output to the min/max values specified for the modulator used.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



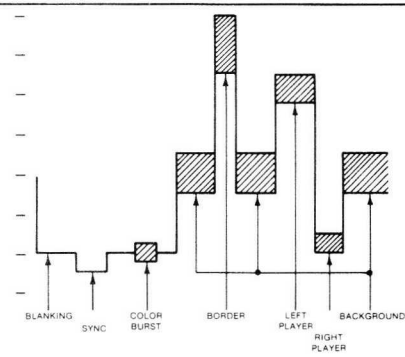


Fig. 4 COMPOSITE VIDEO OUTPUT

CLOCK INPUT

The AY-3-8615 is operated directly from a 3.579545 MHz crystal input. A variable capacitor with a range of 3 to 15 pF should be used to tune the crystal.

CLOCK OUTPUT

The AY-3-8615 generates low impedance 3.579545 MHz clock to directly drive the "8600" series game chips without external components.

Characteristics at +25° C	Min	Typ	Max	Units
Clock Input (Crystal)	—	3.579545	—	MHz
Video & Game Select				
Logic "0" (Select)	—	—	0.2	Volts
Logic "0" (Video)	—	—	1.0	Volts
Logic "1" (all)	V_P–2	—	—	Volts
Hue Adjust (External)	2.0	—	V_P	Volts
Video Output (2 K pot to V_P)	—	1K	—	Ω
Clock Output Rise & Fall Time	—	100	—	ns
Supply Current	—	—	25	mA

TV GAMES

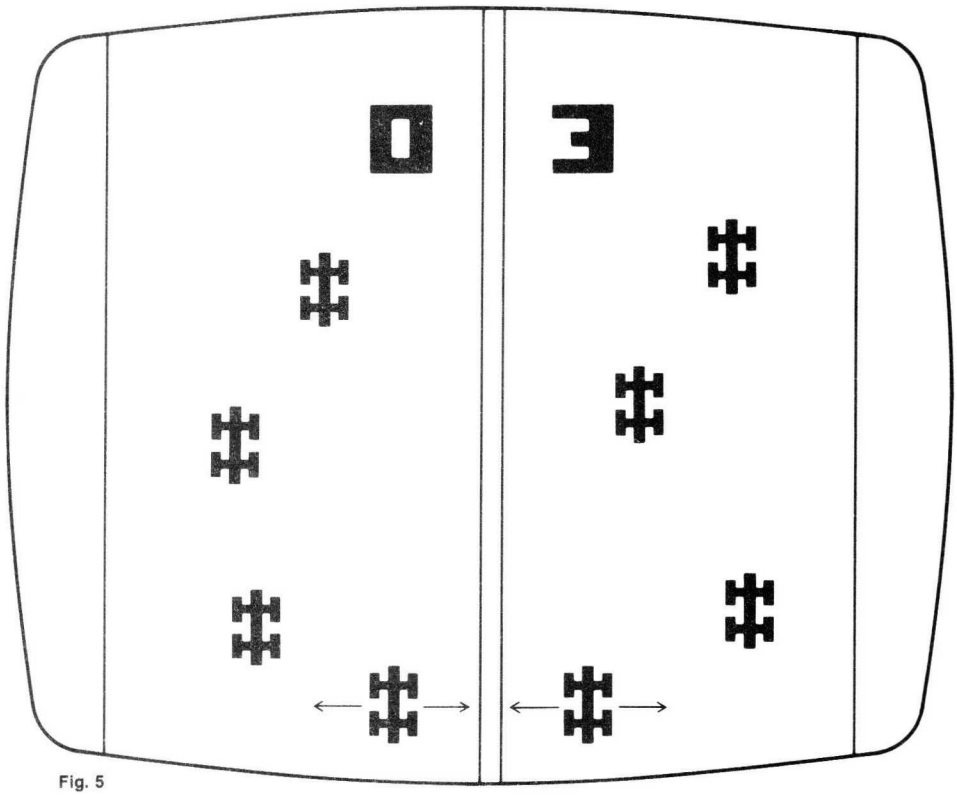


Fig. 5

Roadrace Cartridge (AY-3-8603/8603-1)

A typical T.V. screen display for the game is shown in Figure 5. One driver for each car located at the bottom of each track controls his horizontal position only. After the game is reset the game starts as the picture produced simulates a race track in motion where each driver must maneuver his car around the other cars on the track. Both tracks have the same random obstacle, car pattern with two visible per track, the pattern on the right is 24 lines ahead of the left pattern. This produces random cars on both tracks at one time with the same degree of difficulty for each driver. Video speeds increase every two seconds up to a maximum of seven speeds forward or until either player crashes his car into an obstacle car. Upon a crash, the video motion will stop and a crash sound will be generated. When the game restarts, the forward motion will start from slow and progress in speeds once again.

Simulated engine sound is produced during the game. The engine starts from low and increases in pitch at four second intervals during motion to simulate shift points during the game progress. Every crash scores one point for the opponent. Scores are shown over each track.

The one-player game selection removes the car image on the right track and left driver plays. A point is scored for the driver after passing every eight consecutive obstacle cars. Every crash gives the game, (right track) score one point. The first player or game to score 15 ends the game in either one or two player selection.

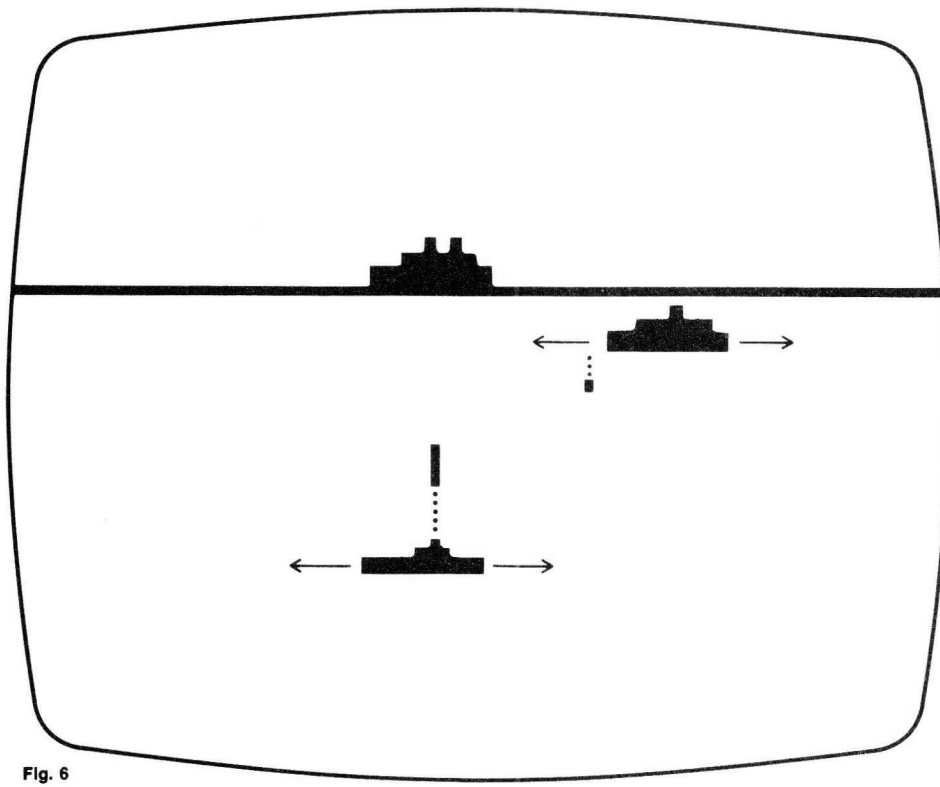


Fig. 6

Warfare Cartridge
(AY-3-8605/8605-1)

A typical T.V. screen display for the game is shown in Figure 6. One player for the submarine and one for the destroyer each controls his horizontal position only. After the game is reset the game starts as the picture produced simulates ships moving across the sea at various speeds. One player controlling the destroyer must protect the ships and depth charge the submarine while the submarine controller tries to torpedo the ships and/or the destroyer.

The destroyer and the submarine are each controlled horizontally by a single pole double throw center off switch. The destroyer moves at twice the speed of the submarine, with the control switch in the center position the vessel controlled stops all movement.

The submarine and the destroyer can only fire torpedoes and depth charges respectively at one shot per four second rate maximum. Torpedo movement is only in the vertical upward direction and depth charge movement is only vertically down. All depth charge hits on the submarine are counted as two points for the destroyer. The submarine scores 1 point for hitting a cargo ship, 2 points for a premium (capital) ship, and 5 points for the destroyer.

Both submarine and destroyer stop movement for 2 seconds when hit by opponents. The cargo ships disappear when hit.

Upon a hit the explosion output envelope from the chip goes to a zero level and gates the white noise on with external circuitry. Sonar sound is emitted throughout game play.

The one-player game selection makes the destroyer move continuously back and forth dropping depth charges at the maximum rate. Each hit for the destroyer (game) is recorded in the same manner as the two-player game. The first player or game to score 15 points ends and wins the game.

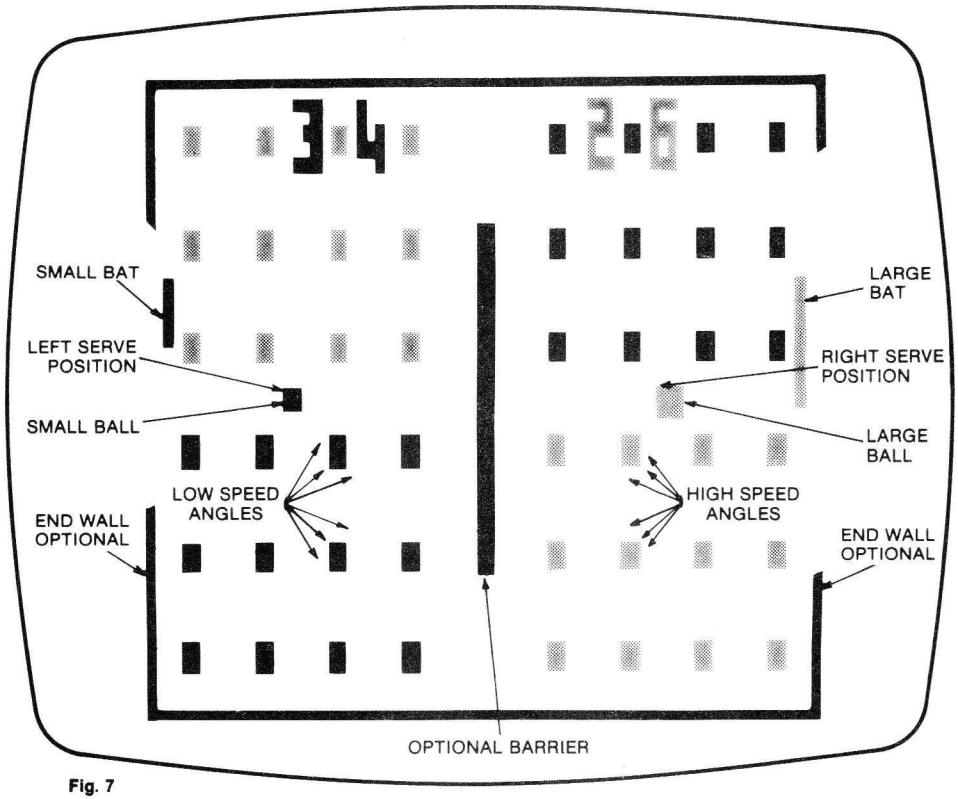


Fig. 7

Wipeout Cartridge (AY-3-8606/8606-1)

This game cartridge contains 10 different games with variable skill selections for one or two players. The object of this set of games is to 'wipe out' more objects than the opponent by scoring the highest number of points without letting the ball out of the playing area. Premium scoring is effective at the start of the game; each time the ball leaves the playing area the premium scoring decreases.

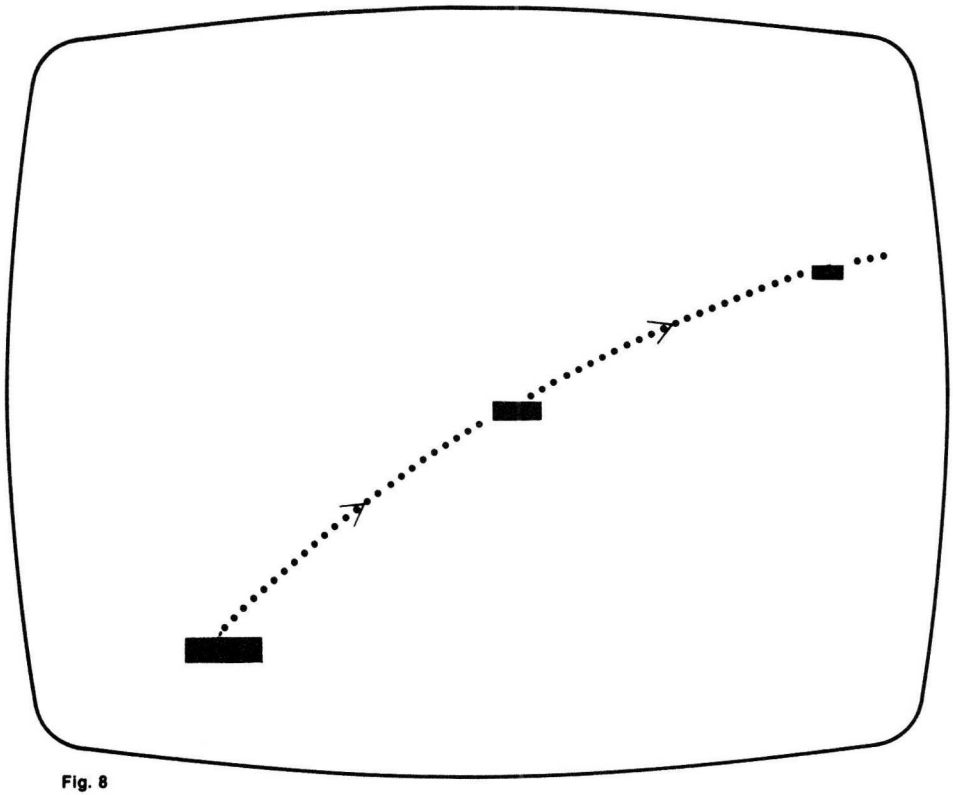


Fig. 8

Shooting Gallery Cartridge (AY-3-8607/8607-1)

The Shooting Gallery game cartridge contains twelve different games with multiple skill selections. The object of this set of games is to shoot at skeet moving across the screen. The skeet move continuously from foreground to background. Realistic sounds are built in.

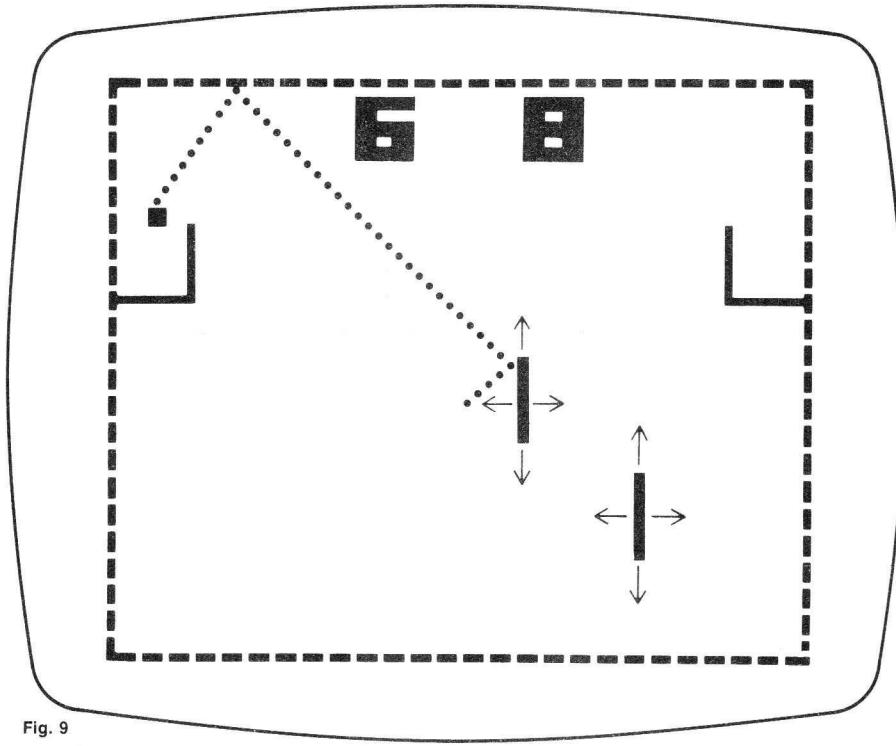


Fig. 9

Supersport Cartridge (AY-3-8610/8610-1)

The Supersport game cartridge contains ten selectable games for one or two players: tennis, hockey, soccer, squash, practice, gridball, basketball, basketball practice, target I, and target II, with realistic game rules, ball serving, and scoring. The two target games do not require extra circuitry or a pistol. Sound generation on hits, boundary and score.

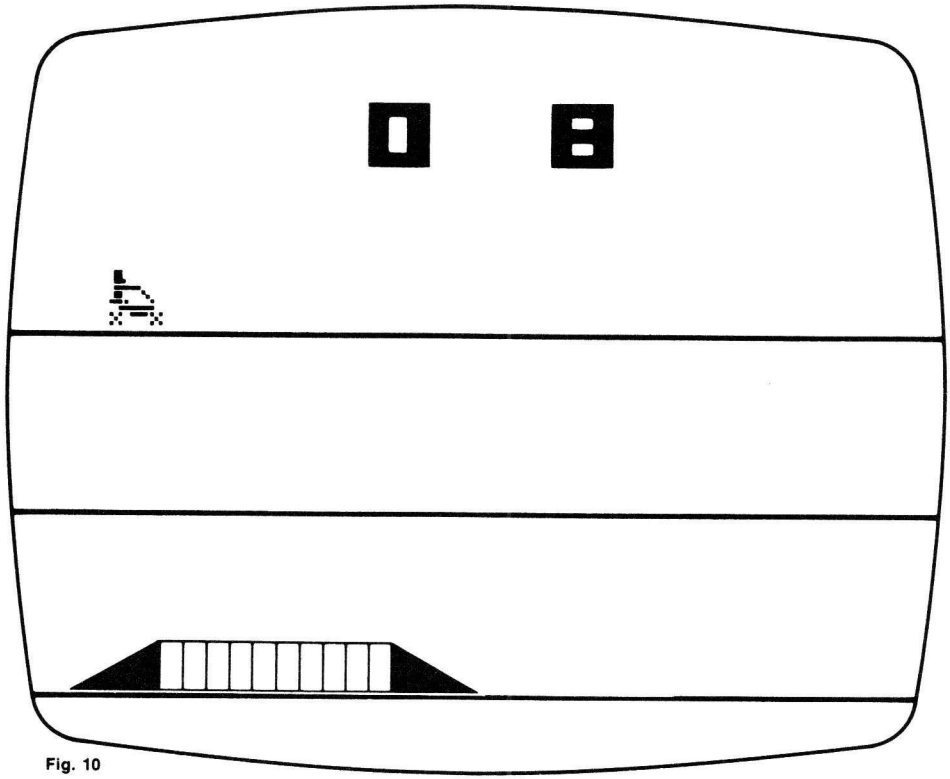


Fig. 10

Motorcycle Cartridge (AY-3-8765)

The AY-3-8765 Cycle cartridge game consists of a cycle game with variable skill selection. The object of this set of games is to simulate cycle jumping, racing and tricks. For one player only. Special sound effects add to the entertainment.

GIMINI Challenger "8950" Programmable Game Set

FEATURES

- User game design capability
- Completely software programmable
- Extensive game library availability in addition to custom software development
- Versatile game instruction set
- NTSC compatible T.V. sync generator
- Color circuitry
- Software controlled score and playfield placement capability

DESCRIPTION

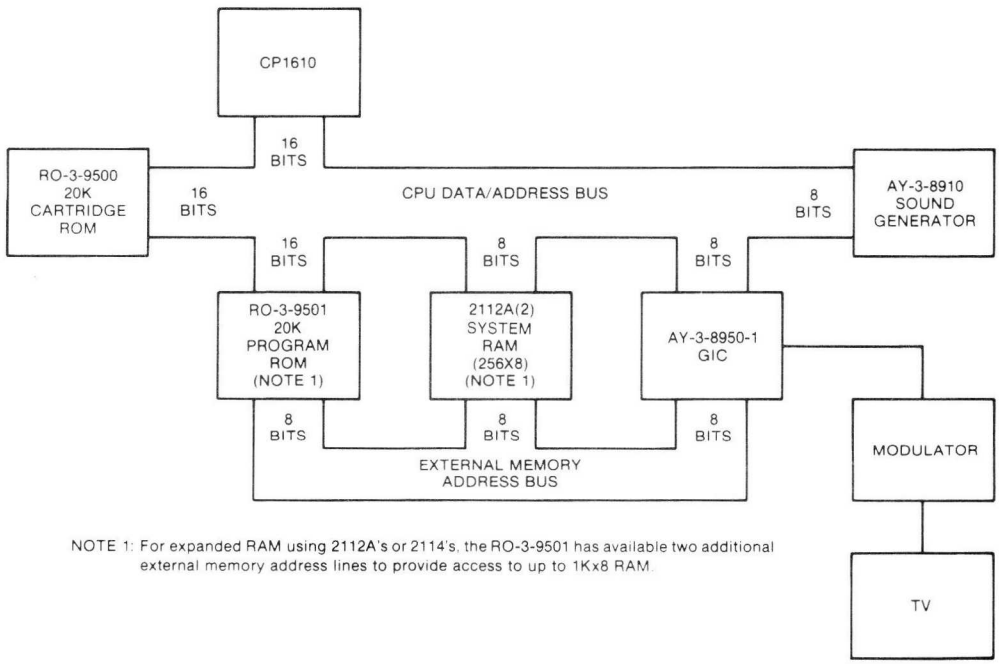
The GIMINI Challenger "8950" Programmable Game Set is a multichip set which can accept different programming ROMs, programmed by the user or available form our extensive game library. The Game Set provides an unlimited number of games; including aggression games, racing games, gambling games, etc. The set consists of the CP1610 microprocessor, a 20K resident ROM game program chip (RO-3-9501), two user-supplied 256 × 4 static RAMs (2112A), and the AY-3-8950-1 graphics interface circuit. Cartridge ROMs (RO-3-9500) extend the user's game options, and the AY-3-8910 Programmable Sound Generator provides game sound effects as well as I/O ports for the game control units.

The GIMINI "8950" system has been desinged as a minimum chip system which provides a very cost-effective and flexible solution to programmability. Since the architecture of the system is based on the CP1610 microprocessor, not only are variations of games limitless, but an endless variety of functions beyond a "game" function are possible.

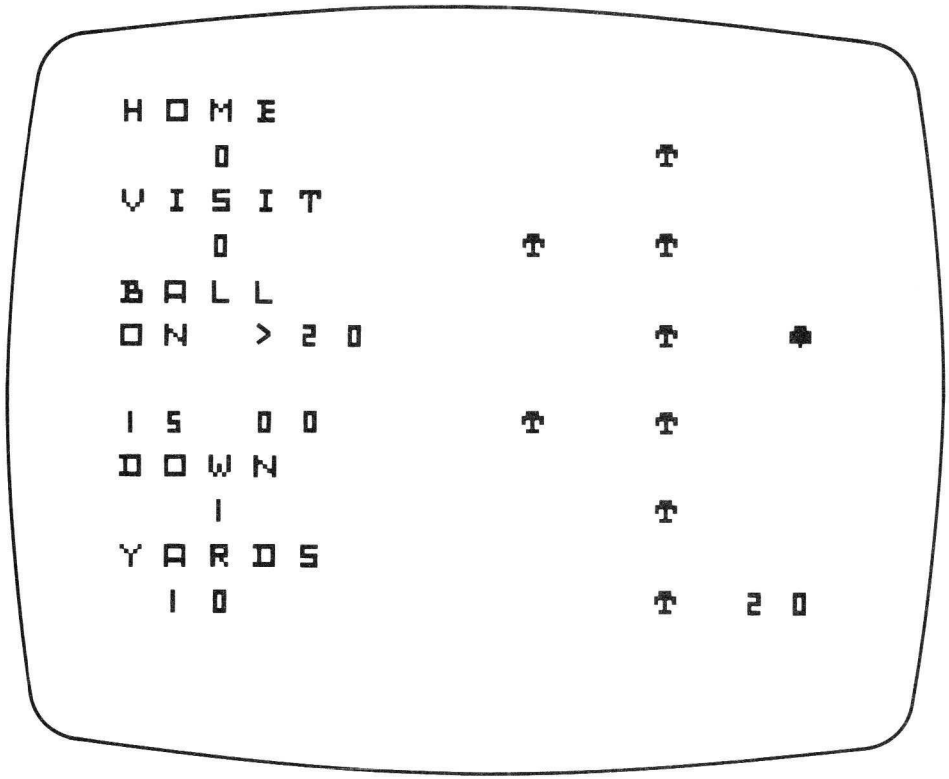
The GIMINI "8950" system is supported by an extremely flexible emulator/development system which provides the capability for a manufacturer to develop and generate new games and to demonstrate these games prior to committing the game program to ROM.

Full details on the GIMINI "8950" system components are contained in the data sheets in this section.

SYSTEM DIAGRAM



NOTE 1: For expanded RAM using 2112A's or 2114's, the RO-3-9501 has available two additional external memory address lines to provide access to up to 1Kx8 RAM.



Computer Mini Football Cartridge

It's you against a friend with the computer controlling the defense.

Start the game by pushing "YES" when "PRO" or "SEMI PRO" appears to choose the strength of the defense. Player one is the Home team (Clubs) and defends the left goal. Player two is the Visiting team (Spades) and defends the right goal.

Try to make ten yards in four carries by moving your offensive player according to the arrows on the control. You may leave your direction control depressed and let the computer move for you, or keep pushing and releasing the button to move faster.

The computer controls the six line men and two defensive backs and is programmed to tackle you. When you are tackled, the player responsible flashes and the crowd roars.

The screen shows thirteen yards and is set up at the beginning of the play with three yards behind you and ten ahead, and the ball on the line of scrimmage. If you run past all of the defenders, the computer "pans" the field ahead thirteen yards and watches you enter from the other end. If you make at least ten yards in four downs or less, you are given a "first and ten" where the ball was downed.

On fourth down you may elect to kick by pushing "yes" or continue the fourth down play by pushing "no". The computer randomly controls the distance of the kick and the run back. If the ball passes between the goal posts, you get a three point filed goal. If the ball is turned over to the other team, their fight song is played.

If you evade all of the defenders and cross the "G" goal line, you are awarded seven points and the computer plays "charge". If you are caught in your own end zone, your opponent is given two points and the ball.

The game has four quarters of fifteen "mini-minutes" each. At two minutes before half time and the end of the game, a two minute warning is given.

Strategy Cartridge

Strategy is a 1-4 player dice game. If less than 4 players are selected, the computer may also play against the other players. The object of the game is to accumulate the highest score possible on your score card. The score card consists of 13 categories and a bonus section. The categories are as follows: ones, twos, threes, fours, fives, sixes, three of a kind, four of a kind, full house, small straight (i.e. 1, 2, 3, 4), large straight (i.e. 1, 2, 3, 4, 5), chance, and stragety (five of a kind).

Points are scored by rolling five dice (computer simulated) and totalling the resulting score in an unused category on your card. Players take turns "rolling dice" and scoring points until every category on the score card is filled. At the end of the game, scores are automatically totalled and displayed. Each player's turn consists of up to 3 rolls of the dice from 1 to 5 dice. Scoring for the categories is as follows:

Ones = Total of dice equal to 1
Twos = Total of dice equal to 2
Threes = Total of dice equal to 3
Fours = Total of dice equal to 4
Fives = Total of dice equal to 5
Sixes = Total of dice equal to 6
3 of a Kind = Total of the 3 dice (3 sixes = 18)
4 of a Kind = Total of the 4 dice
Full House = 25
Small Straight = 30
Large Straight = 40
Chance = Total of all dice
Strategy = 50

One hundred bonus points are scored for every "strategy" after the first one.

Spellbound Cartridge

Spellbound is a word game in which each of two players, in turn, is randomly dealt a "tray" of seven letters, on screen, by the computer. Using his control-unit, player #1, may elect to either form a word or discard any two of his letters when the message "DISCARD?" is displayed. If player #1 so chooses, he may discard by operating his "YES" button which causes the first (left-most) letter of his "tray" to flash. Operation of the "NO" button causes the next letter to flash and he may now decide to discard or retain it. This sequence continues until he has chosen two letters to discard. (The computer will provide two additional random letters after the second player's turn). After player #1's second discard, control reverts to player #2, who may elect to form a word or discard.

Points are awarded based on the letters used and their relative positions. The computer randomly assigns letter and word multipliers for each round, keeping track of each player's score and displaying them in the upper left of the screen. In the example above, using a "Z" over the X3 awards 30 points instead of the single letter value of 10 for "Z". The word multiplier is also random and may be "SINGLE", "DOUBLE" or "TRIPLE". It appears in the lower left of the screen. In the example above, the word "BUZZARD" has a "DOUBLE" word score of 106 points. Prior to awarding the point value, the opposing player is asked to verify the assembled word. Upon verification, the player's score is adjusted and he is given the opportunity of discarding two of the letters in the assembled word. These two letters are replaced, randomly, by the computer after the opponent has concluded his round. The first player to accumulate 200 points wins the game.

Jumble Cartridge

Jumble is a variation of the popular scrambled letters word guessing game. Words can be from four through six letters which are selected and jumbled by the computer randomly. Should the same word be selected by the computer at another time, it is likely to have the letters jumbled in a different order. The first player to unscramble the jumbled word will be awarded a variable number of points, with more points awarded for an early guess. The first player to reach ten points wins the game.

Hangman Cartridge

The object of Hangman is to guess a mystery word that the computer has chosen. The computer uses a 300 word dictionary comprised of 100 four-letter, 100 five-letter, and 100 six-letter words. At the start of the game, the computer displays the alphabet and 4, 5, or 6 dashes to indicate how many letters are in the mystery word. The player then selects a letter from the alphabet. If the chosen letter is in the mystery word, it is displayed in the correct position(s) and play continues. For every wrong letter guess, a different portion of a "man" is displayed on the left portion of the screen. Play continues until the mystery word is correctly spelled or until the "man" is completely displayed. Six wrong guesses will "hang the man."

Astrowar Cartridge

An enemy warship has sent 3 nuclear torpedoes directed for destruction of your vessel. Your only means of survival is destroyinrpedoes before they reach you. The only means of determining their exact location is thru magnetic directors. A salvo of 3 are launched in the direction of an incoming torpedo. When the directors pass by the incoming torpedo, a computer readout gives the sum of the (X, Y) coordinates of the distance of the miss. After the 3 "sums of the coordinates" are given, a determination must be quickly made on the exact location of the torpedo, and the torpedo destroyed before it reaches the vicinity of your vessel (a time-to-impact readout is given). All 3 torpedoes must be destroyed, one after the other.

If this is accomplished, your vessel goes on the offensive and you must destroy the enemy warship before he fires another salvo of torpedoes.

The game goes on and on until an enemy torpedo destroys your starship (a lose message is displayed), or the enemy is destroyed (a win message is displayed).

Battleship Cartridge

This game is played on a 13×5 matrix displayed on the TV screen as "A" thru "M" horizontally and "1" thru "5" vertically. Ships consist of 1 to 5 horizontal units: aircraft carrier = 5, battleship = 3, destroyer = 2, submarine = 1. 1 aircraft carrier, 2 battleships, 2 destroyers, and 4 subs are randomly placed invisibly in the matrix area. The game is initially played with 45 torpedoes. The player selects an area by a coordinate pair of digits and fires his torpedoes one at a time. A miss is recorded by placing a dash in the appropriate location on the screen; a hit places a zero. To win the game, all locations of a ship, and all ships must be hit before running out of torpedoes. A win message is displayed. If the player runs out of torpedoes before the last ship is totally destroyed, the game is over and a loss message is displayed.

The following games introduce a new factor only possible with "computer" games. The computer actually "learns" by playing to effectively become a more skilled opponent.

Awari Cartridge

You play against a modern computer at the world's oldest game. In ancient days, the game was played using pebbles in pits in the ground. Your computer shows the number of pebbles in the pits with a number. The computer plays on the black squares and you play on the red.

The rules are simple. You pick up all of the pebbles in a pit and deposit them one at a time into the following pits, going counter clockwise. If the last beam drops into the scoring pit on the right side of the screen, you get one more turn. If the last bean falls into an empty pit, the computer moves it and the pebbles in the pit acress from it into the scoring pit (if the other pit is not empty).

The game begins when you answer "yes" or "no" when asked if you want to make the first move.

The game is over when you or the computer have no pebbles left in the playing pits. You win if you have more pebbles in your scoring pit. The computer offers legal moves by placing an arrow over the pit. A "yes" will begin the move, and a "no" will advance to the next legal move.

Be careful - as you gain in skill, the computer is programmed to begin playing more intelligently.

Nim Cartridge

Nim is a game of logic where the player who takes the last piece wins.

If you allow the computer to set up the board, it will randomly set from one to six rows of from one to thirteen pieces. You are allowed to set up the board by choosing the number of rows with variable number of pieces in each row.

Since the player who goes first has an advantage, the computer flips a coin and allows you to call heads by pressing "yes" and tails by pushing "no". If our choice comes up, you may choose to go first by pushing "yes" when the computer asks.

When it is your turn, you first choose the row by pushing "no" until the proper row is chosen, then "yes". Once you have chosen a row, each depression of "yes" takes another piece until the "no" is pushed or all pieces are gone.

As with Awari, the computer gets "smarter" if you beat it often enough.

Tic Tac Toe Cartridge

Similar to the conventional game, but computer learns through successive plays.

Hex Pawn Cartridge

The game is played on a 3×3 grid, each player (you and the computer) has 3 pawns on his side of the grid. The pawns move in a similar manner to chess. The program learns by elimination of bad moves. This successfully makes the machine a better opponent. The philosophy behind this game leads to other cybernetic games in which the computer "learns" as it plays.

Even—Cybernetics Game Cartridge

An odd number of objects is placed in a row. You take turns with the computer picking up between one and four objects each turn. The game ends when there are no objects left, and the winner is the one with an even number of objects picked up. The computer starts out only knowing the rules of the game. Using techniques of artificial intelligence, it gradually learns to play from its mistakes until it plays a very good game. After approx. 20 games, the computer is a challenge to beat.

Munch Cartridge

Game for 1-4 players on a 12 (horizontal) × 5 (vertical) grid. A poison "P" square is positioned in the upper left-hand of the cookie grid. Each player, in turn, munches a piece of the cookie avoiding the poison square. To munch the cookie, the player selects a row and column after which all the squares on the row and column selected and the squares below and to the right of the selection disappear. The victor is the player that survives.

Graphics Interface

FEATURES

- On-chip 64 character generator ROM
- On-chip oscillator/amplifier
- Direct interface to CP1610, RO-3-9500 Series ROMS, 2112A/2114 Series RAMS, and AY-3-8910 Programmable Sound Generator.
- On-chip NTSC compatible T.V. sync generator
- On-chip color circuitry

DESCRIPTION

The AY-3-8950-1 Graphics Interface Chip (GIC) is the T.V. display generator for the GIMINI "Challenger" programmable game system. The GIC reads the contents of the RAM, decodes it and displays the requested information on a standard 525 line T.V. The GIC provides the complete T.V. signal including sync, color burst, blanking and video data.

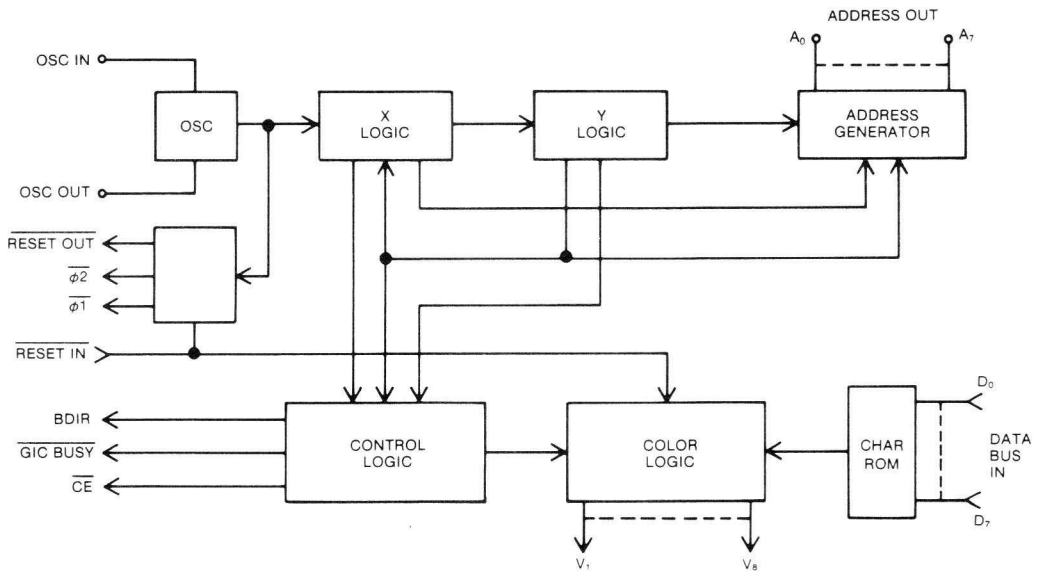
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

Color Burst Hi	1	40	V_{SS}
Color Burst Lo	2	39	Red Hi/White Hi
Blanking & Black	3	38	Red Lo
Test	4	37	Green Lo
Hue Control	5	36	Green Hi
Sync	6	35	Address Output A_0
Input D_0	7	34	NC
Input D_1	8	33	Address Output A_1
Input D_2	9	32	Address Output A_2
Input D_3	10	31	Address Output A_3
Input D_4	11	30	Address Output A_4
Input D_5	12	29	Address Output A_5
Input D_6	13	28	Address Output A_6
Input D_7	14	27	Address Output A_7
NC	15	26	$\overline{CE}$ Output
$\overline{Gic\ Busy}$	16	25	BDIR Output
$\overline{Reset\ Out}$	17	24	Sound Output
$\overline{\phi 2}$ Output	18	23	OSC/Amplifier Out
$\overline{\phi 1}$ Output	19	22	OSC/Amplifier In
V_{DD}	20	21	$\overline{Reset\ In}$

BLOCK DIAGRAM



PIN FUNCTIONS

Pin	Name	Function
10 VIDEO PINS:		
36	Green Hi	This is an open drain output device to V_{SS}. It is low impedance whenever green is to be displayed. It is high impedance otherwise.
37	Green Lo	This is an open drain output device to V_{SS}. It is low impedance at a 3.58 MHz rate when green is selected. It is high impedance otherwise.
39	Red Hi/White Hi	This has two open drain output devices to V_{SS}. It is low impedance whenever red or white is to be displayed. White and red are never on together. When white is to be displayed, the output reaches voltage V_{OUT} 1. When red is to be displayed the output reaches voltage V_{OUT} 2 which is a different voltage level than V_{OUT} 1.
3	Black/Blanking	This has two open drain devices similar to Pin 39. One device is on when black is to be displayed. The other is on when blanking is displayed.
38	Red Lo	This is an open drain device to V_{SS} similar to green lo.
1	CBH-Color Burst Hi	This is an open drain device to V_{SS} similar to Pins 36 and 39.
2	CBL-Color Burst Lo	This is an open drain device to V_{SS} similar to Pins 36, 39 and 1. It is identical to Pin 39 because there are two output devices connected to this pin. Only one output device can be on at one time.
6	Sync	This is an open drain device to V_{SS} similar to Pins 36, 39, 1 and 3.
4	Test	This input disables the 3.58 MHz from appearing on the color outputs. There is an internal pull down on this input.
5	Hue Control	This input changes the phase of the 3.58 MHz on the color outputs.
8 DATA INPUTS:		
7-14	D0-D7	These are inputs to the ROM section of the GIC. The 8 bit input is decoded into 1 of 64 alphanumeric characters or special characters. There is a pull-up resistor of 5K ohms on each input. The 64 alphanumeric characters are shown in Appendix A. To select character inputs D6 and D7 must be zero. Alphanumeric

	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	6	BIT	OCTAL	CODE		
PINS	14	13	12	11	10	9	8	7

EXAMPLES:

LETTER "G"	0	0	0	0	0	1	1	1
NUMBER "5"	0	0	1	1	0	1	0	1

TO SELECT A SPECIAL CHARACTER MAKE D6 = 1

0	1	6	BIT	OCTAL	CODE		

EXAMPLES:

EX. 1	0	1	1	1	1	0	1	1
EX. 2	0	1	1	0	1	1	1	0

THE CODES TO SELECT SPECIALS ARE SHOWN IN APPENDIX B.

8 ADDRESS OUTPUTS:		
35, 33-27	A0-A7	These are outputs from the GIC to the RAM. They address the RAM to produce the 8 bit word for the data input Pins 7-14. To put a character in a particular place on the screen, write the code number into the appropriate RAM address. The location of the data on the screen is shown in Appendix D. To display a G, write the code 00000111 into RAM location 164 as shown in Appendix "C". The outputs addressing the RAM are push-pull.

TV GAMES

PIN FUNCTIONS (continued)

Pin	Name	Function
4 SYSTEM OUTPUTS:		
16	$\overline{\text{GIC Busy}}$	This is a push-pull output. It goes low at line 46 and high at line 240.
25	BDIR	This is a push pull output. It goes high at line 47 from X position 50 to X position 86 for each frame.
26	$\overline{\text{CE}}$	This is an open drain single device to Vss. It goes low at line 48 and remains low until line 240 when it returns to high.
24	Sound	This is a push-pull output. It is low when there is no sound. When sound is selected the output is 2kHz. 1kHz or 500 Hz depending on the data in RAM location 226. D0 in loc. 226 selects 2kHz, D1 in loc. 226 selects 1kHz and D2 selects 500 Hz. The sound lasts for the duration of the data bits in RAM location 226.
6 CLOCKS AND RESETS I/O:		
23	Osc. Input	This is a hi-impedance input to the oscillator. Osc. freq. is 3.579545 MHz.
22	Osc. Output	This is the output of the internal oscillator amplifier.
19	$\overline{\phi 1}$ Output	These 2 pins are push-pull outputs which drive the CPU clock generators at one-half of the osc. freq.
18	$\overline{\phi 2}$ Output	
21	$\overline{\text{Reset}}$ In	This input resets the GIC sync generator. The osc. is not affected. ϕ 1 is reset Hi, ϕ 2 low, M sync out low, GIC Busy Hi, BDIR low, CE hi, Sound is not determined, address outputs are hi impedance, and color outputs are off.
17	$\overline{\text{Reset}}$ Out	This output to the CPU is a push-pull signal.

ELECTRICAL CHARACTERISTICS

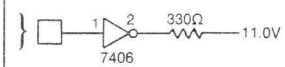
Maximum Ratings*

V_{DD} ..... -0.3 to +12.0V
Storage Temperature ..... -20°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

STANDARD CONDITIONS (unless otherwise noted)

V_{DD}=5.0V ± 5%
V_{SS}=0.0V
Ambient Temperature=0°C to +40°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock Frequency	–	3.579	–	MHz	Std. color crystal
Input Logic Levels					
Logic 0	0.0	–	0.5	V	
Logic 1	3.5	–	V_{DD}	V	
I_{DD}	–	–	125	mA	@ 5V
Input Currents					
Data Inputs D0-D7	-0.3	–	-4.0	mA	Input connected to V_{SS}
Master Clear Input	-0.1	–	-1.3	mA	Input connected to V_{SS}
Test Input	30	–	400	μA	Input connected to V_{DD}
Address Outputs					2.7K Ω to V_{DD}
Logic 0	0.0	–	1.0	V	
Logic 1	3.0	–	V_{DD}	V	
Output current in high imped. state	-0.15	–	-2.0	mA	Out. connected to V_{SS} Reset pin at gnd.
System Outputs					
$\overline{\phi 1}$, $\overline{\phi 2}$					
Logic 0	0.0	–	1.0	V	
Logic 1	3.0	–	V_{DD}	V	
BDIR, $\overline{\text{GIC BUSY}}$, Sound					
Logic 0	0.0	–	1.0	V	2.7K to V_{DD}
Logic 1	3.0	–	V_{DD}	V	
$\overline{\text{CE}}$ open collector output					
Logic 0	0.0	–	1.0	V	2.7K to V_{DD}

SYSTEM OPERATION

The System Diagram is shown below. During the time the GIC busy signal is high, the CP 1610 is operating to make game and display computations. The 20K ROM supplies the instructions to the CP 1610. The RAM locations 227-377 (octal) provide scratch pad memory for the CP 1610. The address code in GIC ROM of the character to be displayed is written into the appropriate RAM locations by the CP 1610.

When the GIC busy signal goes low the CP1610 stops all computations and goes into a waiting mode. The GIC chip then reads the RAM to determine what is to be displayed on the T.V. The GIC automatically formats the T.V. screen as shown in Appendix D. Each of the first 225 (octal) RAM Locations corresponds to specific T.V. picture slots as shown. For example, the code for the letter "G" (00000111) when placed in RAM location 164_8 causes the "G" to appear on the T.V. screen in slot 164_8.

Alphanumeric characters can be written in any screen slot as shown in Appendix E. In addition, special characters can be displayed on the right hand side of the T.V. screen as shown in Appendix F.

When the GIC chip stops accessing the RAM, the GIC busy signal goes high again. The CP 1610 goes out of the waiting mode and resumes its computations from where it left off. The CP 1610 computes for 4 millisec out of every 16 millisec available.

SYSTEM ORGANIZATION

When the GIC busy signal is high, the external address bus and data bus are controlled by the CPU and the status of these buses is indicated by BC1, BC2 and BDIR.

AY-3-8950-1 OPERATION

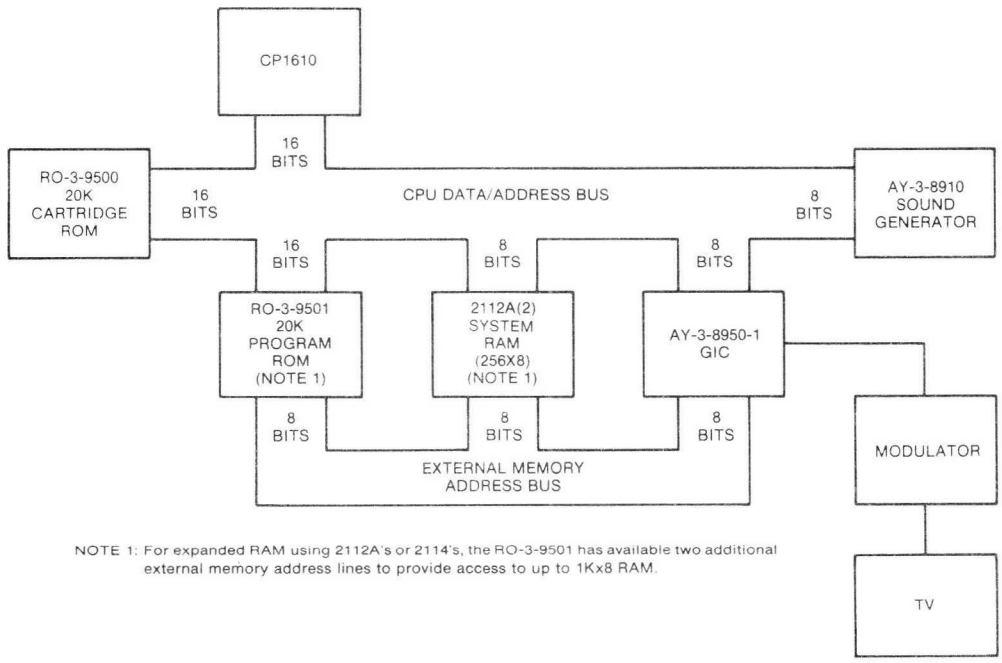
The GIC can display alphanumeric messages on the T.V. as shown in Appendix E. The character set is shown in Appendix A. The characters include the most widely used Alphanumerics.

To write the message in Appendix E, the CPU has placed the following codes in the RAM.

LOC (Octal)	Data (Octal)	T.V. Symbol
111	0024	T
112	0010	H
113	0005	E
114	0000	Space
		Etc.

The GIC automatically reads the RAM in the proper sequence. The data from the RAM addresses the internal GIC character generator ROM. The resultant data is loaded into register and shifted out.

SYSTEM DIAGRAM



NOTE 1: For expanded RAM using 2112A's or 2114's, the RO-3-9501 has available two additional external memory address lines to provide access to up to 1Kx8 RAM.

RULES OF GIC SYSTEM VIDEO OUTPUT

The left side of screen can display 64 alphanumeric symbols contained in memory on boxes arranged 6 across and 12 down. The 5 x 7 characters are placed on the 6 x 8 boxes to provide spacing between them. The characters are white on a green background. (See Appendix A)

The right side of the screen can display any one of the 64 alpha numeric characters 5 x 7 in size on the bottom portion of the 9 x 16 boxes arranged 13 across and 6 down. The characters are white on a green background. (See Appendix A)

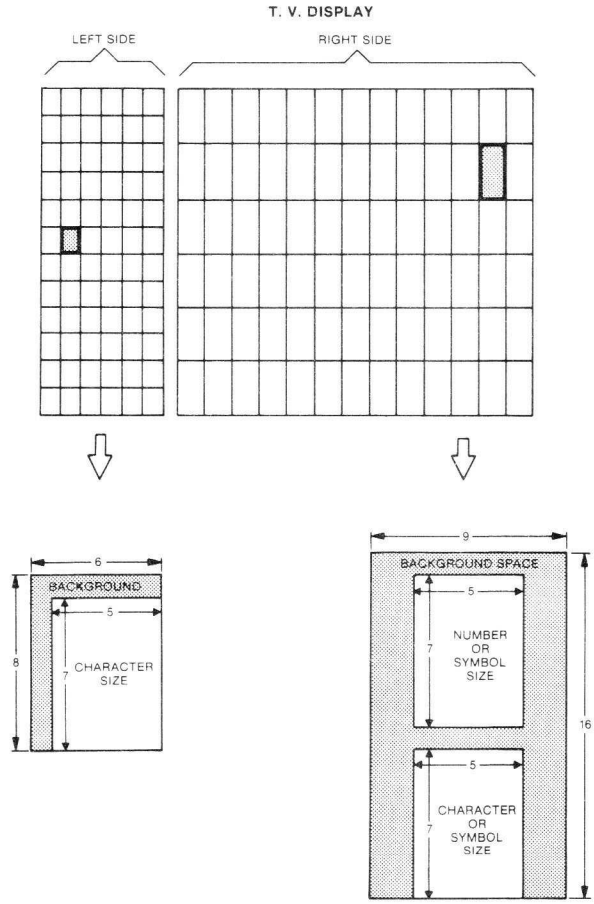
OR

The right side of the screen can display the numbers 0 to 10, J, Q, K, and A on the top portion of the 9 × 16 boxes. The bottom portion can display a club, a diamond, a spade, or a heart only. (See Applendix B)

The character chosen for the bottom portion of the box determines the background color for the entire box. A club or a spade specifies a black box while a diamond or a heart specifies a red rectangle. All characters are displayed as white.

OR

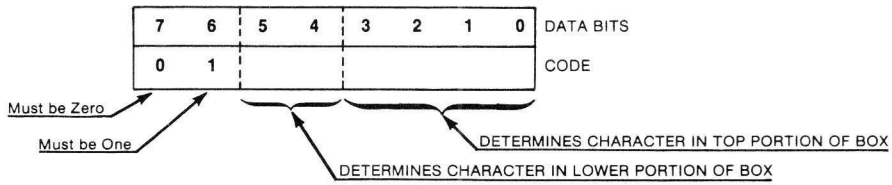
The right side of the screen can display a white output for the full size of the 9 x 16 box when chosen.



APPENDIX A: Alphanumeric Shapes

Code	Character	Code	Character	Code	Character	Code	Character
00	Space	20	P	40	Space	60	0
01	A	21	Q	41	!	61	1
02	B	22	R	42	"	62	2
03	C	23	S	43	#	63	3
04	D	24	T	44	$	64	4
05	E	25	U	45	%	65	5
06	F	26	V	46	&	66	6
07	G	27	W	47	'	67	7
10	H	30	X	50	)	70	8
11	I	31	Y	51	(	71	9
12	J	32	Z	52	:	72	10
13	K	33	↓	53	+	73	J
14	L	34	Club	54	-	74	Q
15	M	35	Diamond	55	=	75	K
16	N	36	Spade	56	.	76	A
17	O	37	Heart	57	÷	77	?

APPENDIX B: Color Mode Right Hand Screen



DATA IN UPPER RECTANGLE

Data Bits 3	2	1	0	Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	J
1	1	0	0	Q
1	1	0	1	K
1	1	1	0	A
1	1	1	1	?

DATA IN LOWER RECTANGLE

Data Bits 5	4	Character
0	0	Club - BLACK
0	1	Diamond - RED
1	0	Spade - BLACK
1	1	Heart - RED

7	6	5	4	3	2	1	0	
1	1	–	–	–	–	–	–	CODE

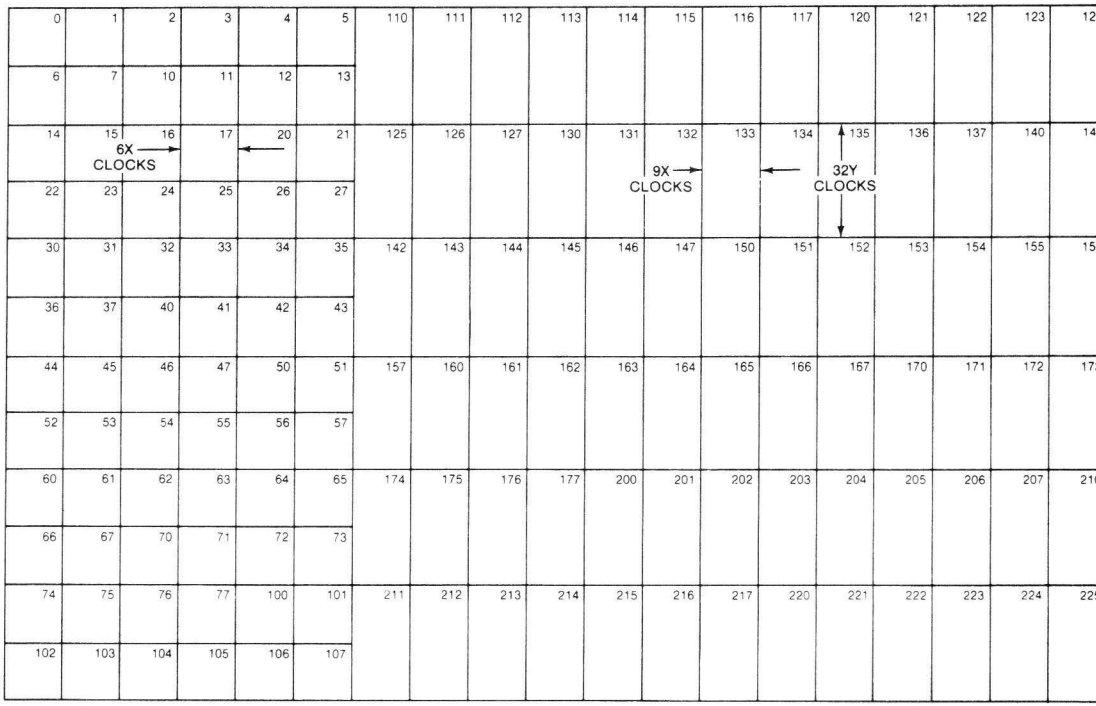
DATA BITS

This code causes the entire rectangle to be white.

APPENDIX C Chart for Programming RAM

LOC	Data	LOC	Data	LOC	Data	LOC	Data	LOC	Data	LOC	Data	LOC	Data
0		30		60		110		140		170		220	
1		31		61		111		141		171		221	
2		32		62		112		142		172		222	
3		33		63		113		143		173		223	
4		34		64		114		144		174		224	
5		35		65		115		145		175		225	
6		36		66		116		146		176			
7		37		67		117		147		177			
10		40		70		120		150		200			
11		41		71		121		151		201			
12		42		72		122		152		202			
13		43		73		123		153		203			
14		44		74		124		154		204			
15		45		75		125		155		205			
16		46		76		126		156		206			
17		47		77		127		157		207			
20		50		100		130		160		210			
21		51		101		131		161		211			
22		52		102		132		162		212			
23		53		103		133		163		213			
24		54		104		134		164	**00000111**	214			
25		55		105		135		165		215			
26		56		106		136		166		216			
27		57		107		137		167		217			

APPENDIX D: Octal Location of RAM Addresses Display by GIC



226-SOUND 277 → 377 - SCRATCH (CPU)

APPENDIX E: AY-3-8950-1 Display RAM Layout

ALPHANUMERICS

0 T	1 H	2 E	3 S	4 E	5	110	111 T	112 H	113 E	114	115 G	116 I	117 C	120	121 C	122 A	123 N	124
6 C	7 A	10 N	11	12	13													
14 A	15 L	16 S	17 O	20	21	125 D	126 I	127 S	130 P	131 L	132 A	133 Y	134	135 6	136 4	137	140	141
22 B	23 E	24	25	26	27													
30 S	31 H	32 O	33 W	34 N	35	142	143	144	145	146	147	150	151	152	153	154	155	156
36	37	40	41	42	43	A	L	P	H	A	N	U	M	E	R	I	C	
44 $	45 $	46 $	47 %	50 %	51 %	157	160	161	162	163	164	165	166	167	170	171	172	173
52 +	53 +	54 +	55 —	56 —	57 —		C	H	A	R	A	C	T	E	R	S		
60 •	61 •	62 •	63 /	64 /	65 /	174	175	176	177	200	201	202	203	204	205	206	207	210
66	67	70	71	72	73													
74 E	75 T	76 C	77 •	100	101	211	212	213	214	215	216	217	220	221	222	223	224	225
102	103	104	105	106	107													

226-SOUND 277 → 377 - SCRATCH (CPU)

APPENDIX: E: AY-3-8950-1 Special Characters

ALPHANUMERICS

0	1	2	3	4	5	110	111	112 GREEN BACKGROUND	113	114	115	116	117	120	121	122	123	124
6	7	10	11	12	13													
14	15	16	17	20	21	125	126	127	130	131	132	133	134	135	136	137	140	141
22	23	24	25	26	27													
30	31	32	33	34	35	142	143	144 J ◇ RED	145	146 7 ◇ RED	147	150	151	152	153	154 K ♣ BLACK	155	156
36	37	40	41	42	43													
44	45	46	47	50	51	157	160	161 2 ♜ BLACK	162	163 A ◇ RED	164	165 K ♜ BLACK	166	167	170	171	172	173
52	53	54	55	56	57													
60	61	62	63	64	65	174	175	176	177	200	201	202	203	204	205	206	207	210
66	67	70	71	72	73													
74	75	76	77	100	101	211	212	213	214	215	216	217	220	221	222	223	224	225
102	103	104	105	106	107													

226-SOUND 277 - 377 - SCRATCH (CPU)

16-Bit Single-Chip Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 87 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- 1 μs cycle time, 2 MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

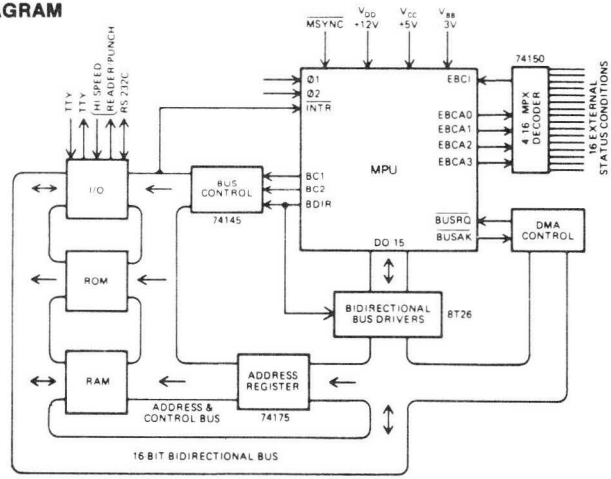
DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories, and Random Access Read/Write Memories are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program, memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1610 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROLS

$\overline{\text{STPST}}$
Input
STop-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

$\overline{\text{MSYNC}}$
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL SIGNALS

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

$\overline{\text{BUSRQ}}$
Input

$\overline{\text{BUSAK}}$
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

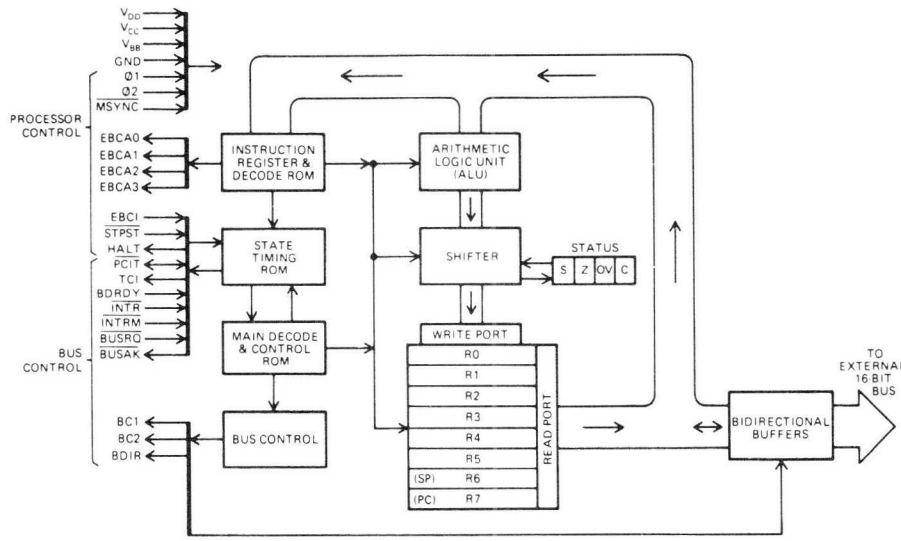
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

$\overline{\text{INTR}}$, $\overline{\text{INTRM}}$
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

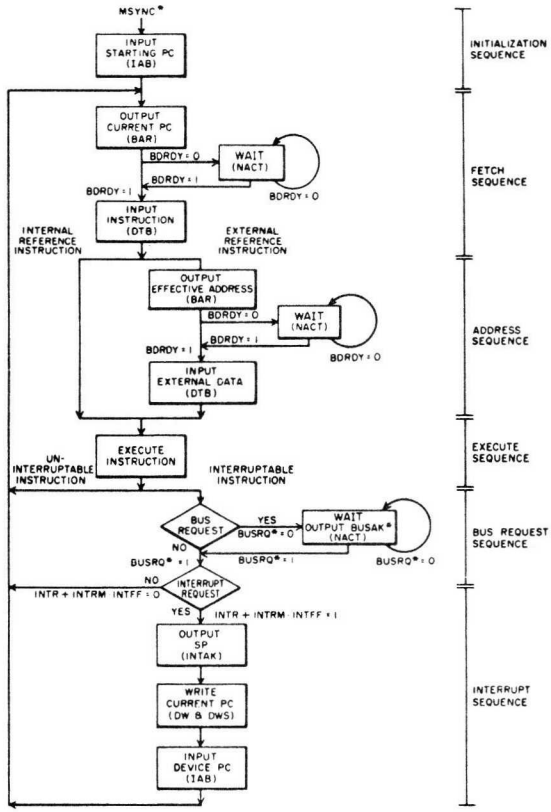
TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

$\overline{\text{PCIT}}$
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1600 INTERNAL BLOCK DIAGRAM



SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

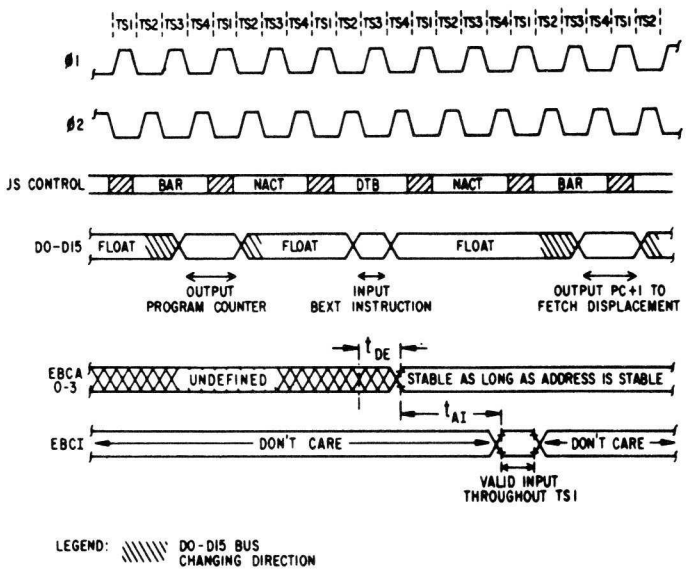
INSTRUCTION SET SUMMARY

		Mnemonics	Operation	Microcycles Dir.	Indr.	Imm.	Stack	Comments
External Reference Instructions	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	
	I/O	MVO	MoVe In	10	8	8	11	
		MVI	MoVe In	10	8	8	11	
Internal Register Instructions	Register to Register	ADDR	ADD contents of Registers	6				Add one cycle
		SUBR	SUBtract contents of Registers	6				if Register 6 or 7, except*.
		CMPR	CoMPare Registers by subtr.	6				Result not saved
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		MOVR	MOVe Register	6				
	Single Register	CLRR	CLeaR Register	6				XORR with itself
		TSTR	TeST Register	6				
		JR	Jump to address in Register	7*				PC←(RRR)
		INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				Two Words
		SIN	Software INterrupt	6				Pulse to PCIT pin
		RSWD	Return Status WorD	6				
		PULR	PULl from stack to Register	11*				PULR=MVI @ R6
		PSHR	PuSH Register to stack	9*				PSHR=MVO @ R6
	Register Shift	SLL	Shift Logical Left	6				one or two position shift capability. Add two cycles for 2-position shift
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
		SWAP	SWAP 8-bit bytes	6				2-position=SWAP twice
Control Instructions		HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				Not Interruptible
		TCI	Terminate Current Interrupt	4				
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
Jump Instructions		J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable Interrupt	12				
Conditional Branch Instructions		B	unconditional Branch	7				Displacement in PC+1
		BC, BLGE	Branch on Carry, C=1	7				PC←PC±Displacement
		BNC, BLLT	Branch on No Carry, C=0	7				Add 2 cycles if test condition
		BOV	Branch on OVerflow, OV=1	7				is true.
		BNOV	Branch on No OVerflow, OV=0	7				
		BPL	Branch on PLus, S=0	7				
		BMI	Branch on Minus, S=1	7				
		BZE, BEQ	Branch on ZEro or EQual	7				Z=1
		BNZE, BNEQ	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S∀OV=1
		BGE	Branch if Greater than or Equal	7				S∀OV=0
		BLE	Branch if Less than or Equal	7				ZV(S∀OV)=1
		BGT	Branch if Greater Than	7				ZV(S∀OV)=0
		BUSC	Branch if Sign ≠ Carry	7				C∀S=1
		BESC	Branch if Sign = Carry	7				C∀S=0
		BEXT	Branch if External condition is True	7				4 LSB of Instruction are decoded to select 1 of 16 external conditions.

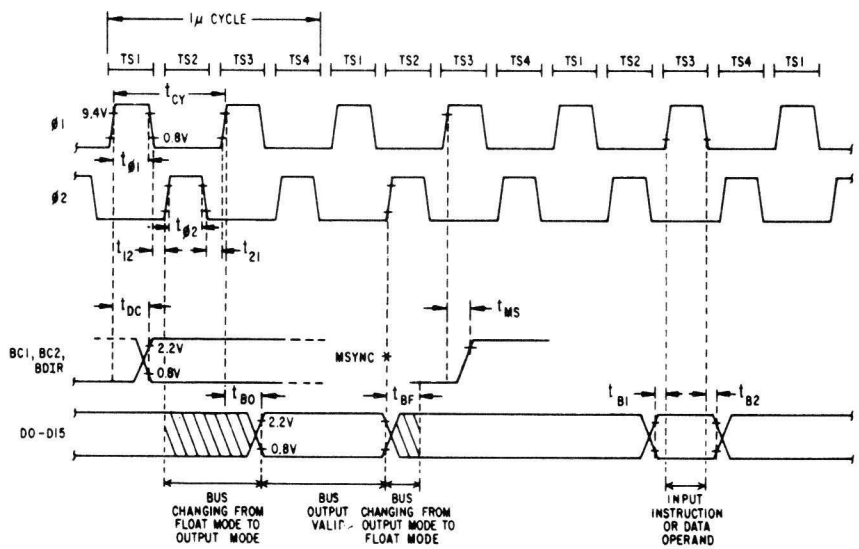
1 MICROCYCLE = 2 CLOCK CYCLES

TV GAMES

BUS TIMING DIAGRAM



TYPICAL INSTRUCTION SEQUENCE



BRANCH ON EXTERNAL CONDITION INSTRUCTION

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions: (unless otherwise noted)
V_{DD}=+11V±5%, 70mA(typ), 110mA(max.) V_{BB}= −3V±10%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.0	–	V_{DD}	V	
Low	V_{ILC}	0	–	0.6	V	
Input current	—	—	—	15	mA	$V_{IHC} = V_{DD} - 1$
Logic Inputs						
Low	V_{IL}	0	–	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	–	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	–	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	–	–	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	–	–	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	–	–	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	250		–	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	–	–	ns	
Clock Period	t_{CY}	0.5	–	2.0	μs	
Rise & Fall Times	tr, tf	–	–	15	ns	
Master SYNC:						
Delay from φ	tms	–	–	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	–	–	200	ns	1 TTL Load & 25 pF
Output delay from φ2 (output to float)	t_{BF}	–	50	–	ns	
Input setup time before φ1	t_{B1}	0	–	–	ns	
Input hold time after φ1	t_{B2}	10	–	–	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	–	–	200	ns	
BUSAK Output delay from φ1	t_{BU}	–	150	–	ns	
TCI Output delay from φ1	t_{TO}	–	200	–	ns	
TCI Pulse Width	t_{TW}	–	300	–	ns	
EBCA output delay from BEXT input	t_{DE}	–	–	150	ns	
EBCA wait time for EBCI input	t_{AI}	–	–	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; $t_{\phi 1}$ $t_{\phi 2}$ = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
Input Capacitance						
D0-D15	CIN	—	6	12	pF	
All Other	—	—	5	10	pF	
Output Capacitance						
D0-D15 in high impedance state	C_D	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

20480 Bit Static Read Only Memories

FEATURES

- 2048 × 10 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 1K of external RAM (RO-3-9501) or up to 65K of external RAM (RO-3-9502).
- Internal address status and data bits latched
- 300 ns typical data access time
- 1.8μs complete cycle time
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION: RO-3-9501

The RO-3-9501 is a unique 20,480 bit ROM employing a single 16 bit address and data tristate buss. The RO-3-9501 increases the power of single buss microprocessors or microcontrollers by providing separate latched address and control lines for static RAM chips. The RO-3-9501 internally decodes ROM and external RAM control codes. ROM addressing is via an 11-bit word address and a 5-bit chip select code. Ten bit data is outputted on the lower 10 bits of the I/O buss. In addition there are two programmable 16-bit interrupt response codes, one for the first interrupt after master clear and one for all other interrupts. These codes are output to the I/O bus in response to control codes, which do not require a chip select code. The RO-3-9501 contains a 10 bit latch and address output port; the 10-bit address appearing at this port may be used to control an external RAM. The address is latched by a control code on the three mode control lines, and the RAM enable signal which consists of all zeros on data bits 11 through 15. The stored address is copied from bits 0 through 9 on the data buss.

The RO-3-9501 has two programmable features, in addition to the 2048 word by 10-bit ROM. A five bit chip select code decodes data bits 11 through 15 in order to generate the internal chip enable signal. Second, the two 16-bit interrupt response codes are programmable.

DESCRIPTION: RO-3-9502

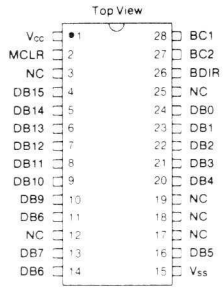
The RO-3-9502 has all the features of the RO-3-9501 described above except that it has a full 16-bit latch and address port for external RAM.

DESCRIPTION: RO-3-9500

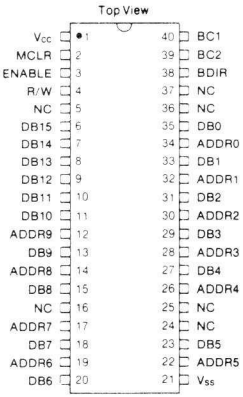
The RO-3-9500 does not provide address facilities for external RAM allowing for its packaging in a 28 lead DIP.

PIN CONFIGURATIONS

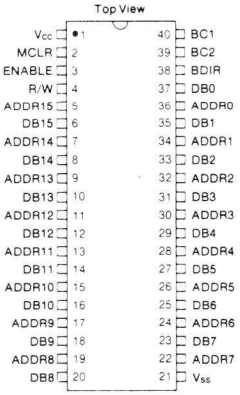
28 LEAD DUAL IN LINE
RO-3-9500



40 LEAD DUAL IN LINE
RO-3-9501



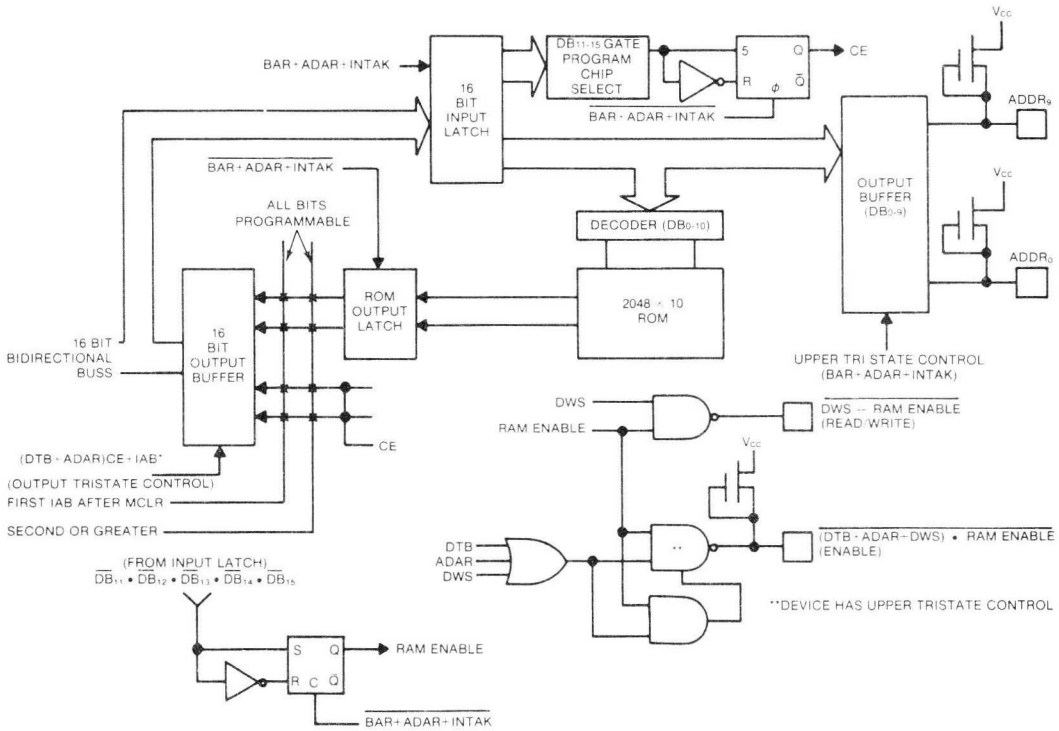
RO-3-9502



PIN FUNCTIONS

Enable (RO-3-9501/02)	An ouput pin to select external RAM (low = true)
R/W (RO-3-9501/02)	An output pin for read/write control of external RAM, a positive pulse controls the write cycle.
ADDR0-9 (RO-3-9501) ADDR0-15 (RO-3-9502)	Output address lines to external RAMs.
DB0-DB15	Bidirectional, tristate data and address buss, high output impedance for NACT control code.
BC1, BC2 BDIR	Buss control 1 and 2, and buss direction control signals determine chip mode control
V_{CC}	+5 volts
V_{SS}	Ground
MCLR	Master clear, sets all outputs to high impedance state when low.

BLOCK DIAGRAM: RO-3-9501



NOTES:

1. Input data and internal chip enable latched by control codes = BAR + ADAR + INTAK
2. Internal chip enable signal cleared by = BAR + ADAR + INTAR
3. Internal RAM enable signal flip flop set by PB11-15 all zeros, cleared by = BAR + ADAR + INTAK
4. RAM enable plus DWS creates low on Read/Write line.
5. RAM enable plus DTB, ADAR or DWS creates enable output signal.
6. DTB or ADAR plus internal chip enable puts output ROM data to tristate buss.
7. Maximum skew time between control code transitions is 40 nsec to avoid false states.
8. Enable R/W and ADDRO — 9 lines normally high impedance outputs. When circuits are enabled, active pull up transistors turned on to allow wired or connection to other chips. RAM control signals and output addresses revert to high impedance state in 2 and 0 - 3μsec respectively. After master clear, chip enable and RAM enable flip-flops turned off and all outputs in high impedance states.

OPERATING MODES

The RO-3-9501 is designed to enhance the system operation of 16-bit Microprocessors that use a single multiplexed buss for data and memory addresses, such as the GI CP1600, the Intel 8085 and the Fairchild 9440. The state diagram shows recommended sequences for initialization, program storage with RAM addressing, and interrupt handling.

The three mode control lines BC1, BC2 and BDIR create 8 functions. As shown in figure one, these functions are chosen to simplify program and data storage in the ROM. Functionally the RO-3-9501 performs the following functions in a microprocessor system:

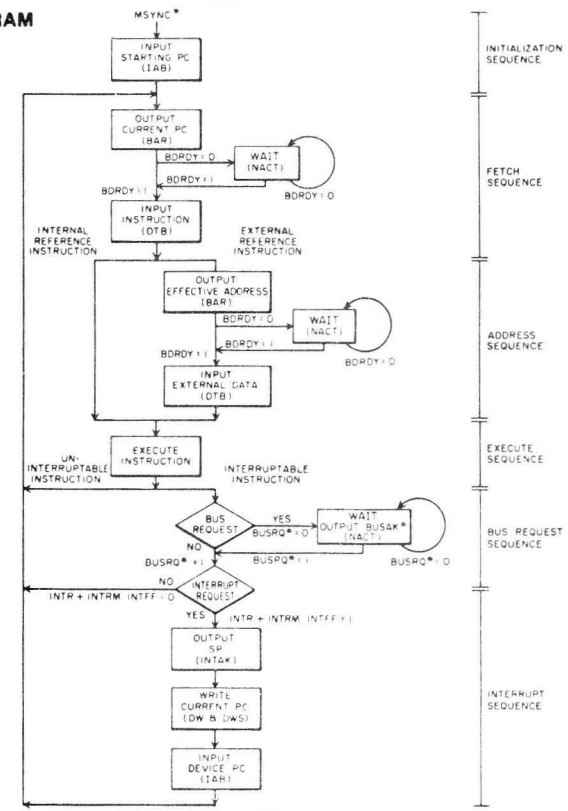
A. When the CPU generates a 5 chip select and seven bits of ROM address, the RO-3-9501 generates a 10-bit response from the 2048 × 10 bit ROM.

B. The ROM output data can be used to create a ten-bit immediate or indexed RAM address, which is then stored in the RO-3-9501 ten output latches and the RAM control lines. In addition the RAM enable and R/W control lines are generated by inernal logic.

C. In response to initial clear and the first interrupt, the RO-3-9501 can be programmed to place a 16-bit trap address on the I/O buss for restarting a chosen program sequence. The RO-3-9501 can additionally be programmed to generate a different 16-bit trap address in response to subsequent IAB's.

For the IAB (Interrupt Address to Buss) commands to work properly, an address must first be loaded into the chip to disable the internally latched chip enable code.

SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and all other input/output voltages with respect to GND .....−0.3V to +18V
Storage Temperature ..... −55°C to 150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

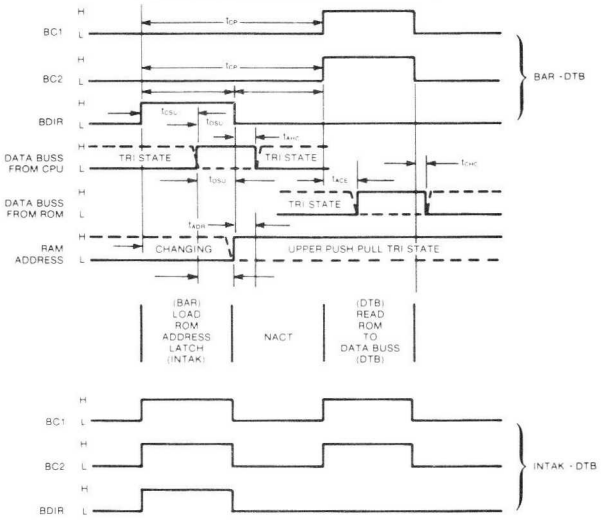
Standard Conditions (unless otherwise noted)

All voltages referenced to GND
V_{DD} = +12V ±5%
Operating Temperature (T_A) = 0°C to +75°C

Standard Conditions (V_{CC} = 5±10%; t = 0°, 70°C)

Characteristic	Symbol	Min.	Typ.*	Max.	Units	Conditions
DC CHARACTERISTICS						
Logic '0' Input	V_{IL}	0	—	0.6	V	
Logic 'I' Input	V_{IH}	1.4	—	V_{CC}	V	
Logic '0' Output	V_{OL}	0	—	0.4	V	I_{sink} = 1mA
Logic 'I' Output	V_{OH}	2.[illegible]	—	V_{CC}	V	I_{source} = 100μA
Input leakage	I_L	—	—	10	μA	
Power Supply Current	I_{CC}	60	—	70	mA	V_{CC} = 5.0V
AC CHARACTERISTICS						
ROM Data Access	t_{ACC}	250	—	350	ns	Fig. 1,5
ROM Data Hold	t_{AHC}	50	—	300	ns	Fig. 1,5
RAM Address Setup	t_{ADR}	150	—	250	ns	Fig. 1, 2, 3, 4
Control Setup	t_{CSU}	500	—	—	ns	Fig. 1
Address Setup	t_{ASU}	300	—	—	ns	Fig. 1
Control Hold Time	t_{OHC}	50	—	—	ns	Fig. 1
No Action Time	t_{NACT}	0	—	2000	ns	Fig. 1
Control Period	t_C	800	—	—	ns	Fig. 1, 2, 3, 4, 5
Code Time	t_{CP}	1600	—	2800	ns	Fig. 1, 2, 3, 4
No Action Time	t_{NACT}	500	—	2000	ns	Fig. 2, 3, 5
Data Setup	t_{DSU}	—	—	300	ns	Fig. 1, 2
RAM Address Hold	t_{AHR}	300	—	2000	ns	Fig. 2, 3, 4
RAM Access Time	t_{ACR}	150	—	300	ns	Fig. 2, 3
Master Clear	t_{MC}	100	—	10,000	ns	Fig. 5

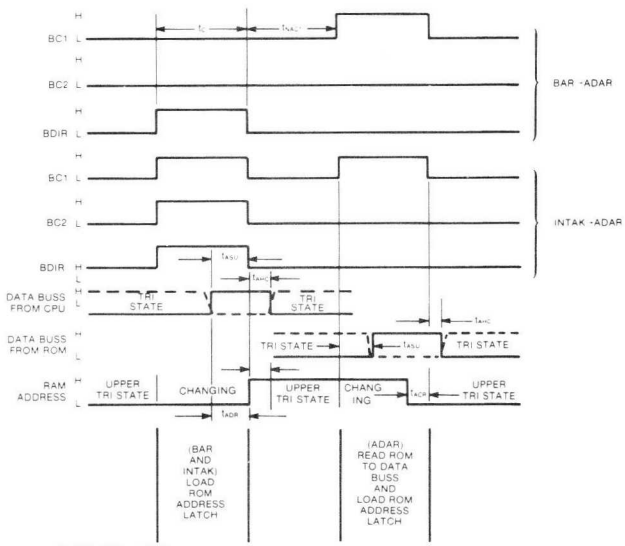
20K ROM
BAR/INTAK INSTRUCTION FOLLOWED BY DTB INSTRUCTION



* Minimum hold time after DTB before going tristate. Maximum time to tristate = 300ns. (all time in nSec)
** BC1, BC2 and BDIR are return to zero signals
*** Upper tristate means that the upper push pull output device is disabled and an internal load resistor will hold the output positive
**** Proper CE address must be latched to allow ROM output to function during DTB
***** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 1

20K ROM
BAR/INTAK INSTRUCTION FOLLOWED BY ADAR INSTRUCTION



** BC1, BC2 and BDIR are return to zero signals
**** Proper CE address must be latched to allow ROM output to function during DTB
***** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 2

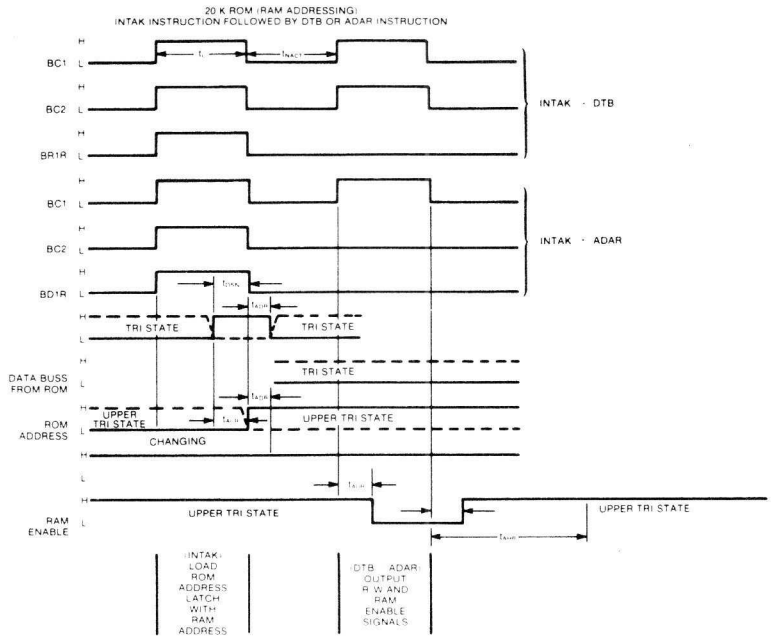
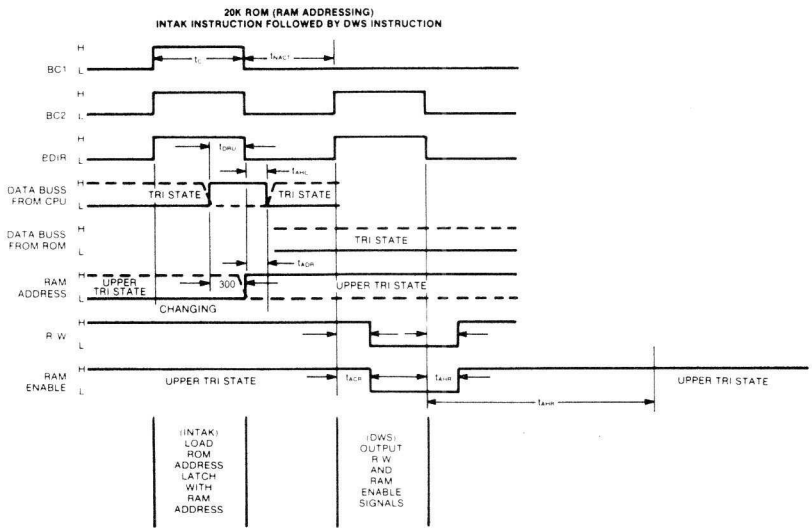
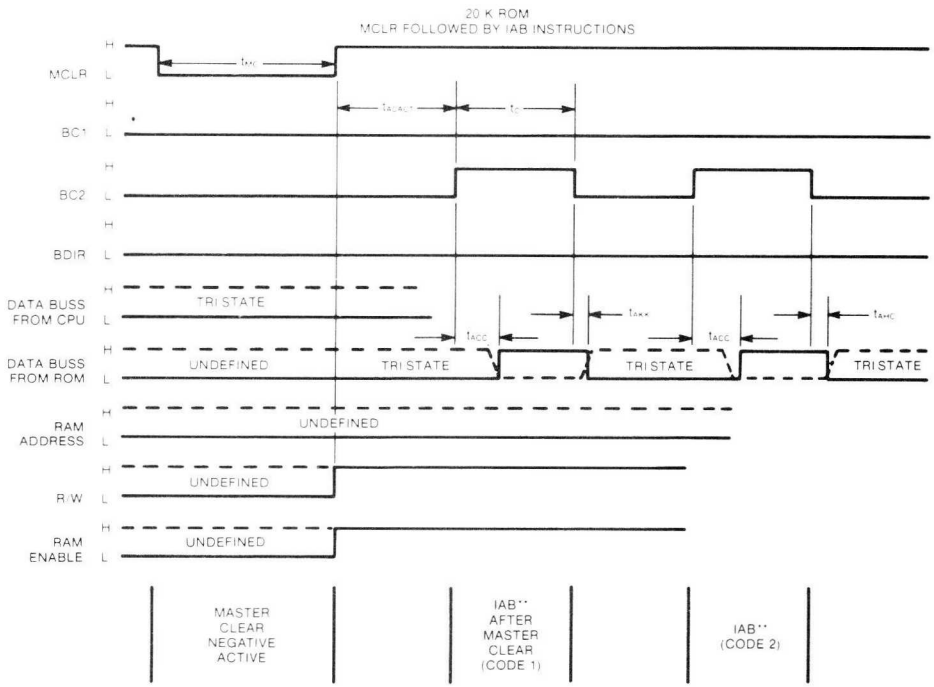


Fig. 3



* Maximum time to upper tri state condition
** RAM address has DB_{11} thru DB_{15} Logic '0'
*** BAR or ADAR can be used instead of INTAK to load RAM address. If ADAR is used remember RAM address will be provided from ROM output to data buss if chip previously enabled.
(All time in nSec)

Fig. 4



* Minimum hold time after IAB before going tri state. Maximum time to tri state = 300 ns.
** The first IAB after master clear will present a 16 bit programmable code to the data buss. Subsequent IAB instructions will output a second code that is gate programmable on ROM chip.
(All time in nsec)

Fig. 5

2112A

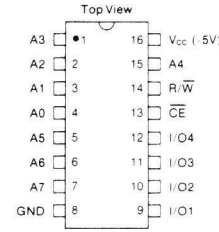
1024 Bit Static RAM

FEATURES

- 256 x 4 organization.
- 350 ns access time.
- TTL compatible.
- Fully static-no clocks required.
- Single +5V supply.

This circuit is not manufactured by General Instrument Microelectronics. The information is provided for reference only.

PIN CONFIGURATION
16 LEAD DUAL IN LINE



2114

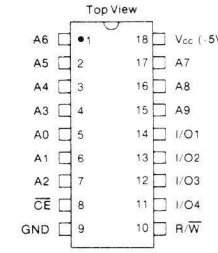
4096 Bit Static RAM

FEATURES

- 1024 x 4 organization.
- 450 ns access time.
- TTL compatible.
- Fully static-no clocks required.
- Single +5V supply.

This circuit is not manufactured by General Instrument Microelectronics. The information is provided for reference only.

PIN CONFIGURATION
18 LEAD DUAL IN LINE



PRELIMINARY INFORMATION

Programmable Sound Generator

FEATURES

- Full software control of sound generation.
- Interfaces to most 8-bit and 16-bit microprocessors.
- Three independently programmed analog outputs.
- Two 8-bit I/O ports for general use.
- Single +5 Volt supply.

DESCRIPTION

The AY-3-8910 is a Large Scale Integrated Circuit that can produce a wide variety of complex sounds under software control. It is easily interfaced to most 8 and 16-bit microprocessors; however, it is optimally designed to directly connect to the CP1600 series of microprocessors. The flexibility of the AY-3-8910 makes it useful in applications such as music synthesis, sound effects, audible alarms, and FSK modems. In addition, once interfaced, the AY-3-8910 provides the microprocessor with two parallel 8-bit bi-directional data ports that are TTL compatible. The analog sound outputs can each provide 4 bits of logarithmic D/A conversion.

The AY-3-8910 is manufactured in the N-Channel Ion Implant process. Operation requires a single 5V supply, a 2 MHz TTL clock and a microprocessor controller such as the 1600 series.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

HARDWARE ARCHITECTURE

The AY-3-8910 is designed to interface directly to the GI CP1600/1610 microprocessor as well as all one-chip microcomputers with 11 or more programmable I/O lines, such as:

GI PIC Series
TI TMS 1000 Series
Intel 8000 Series

The 11 I/O lines used by the one-chip processors to interface to the AY-3-8910 are returned as 16 programmable TTL compatible I/O lines on the AY-3-8910.

Commands are issued to the AY-3-8910 thru the use of memory operations at the appropriate address. Sixteen registers within the AY-3-8910 control the analog outputs and parallel I/O ports. Each of these registers correspond to a memory location displaced from the AY-3-8910 Base Address by the register number.

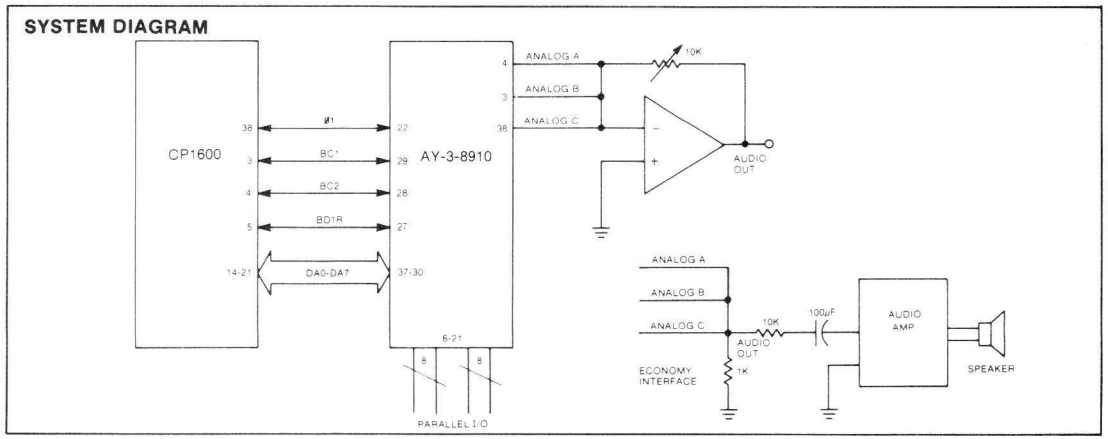
SOFTWARE ARCHITECTURE

Communication between the controller and the AY-3-8910 is based on the concept of memory mapped I/O. With a controller such as the CP 1600 the AY-3-8910 looks like a block of memory. Parallel input and output, as well as programming the three analog outputs for complex sounds is accomplished by performing memory operations on the appropriate memory location.

The AY-3-8910 memory block is organized as 16 consecutive memory locations starting at the base address which is decoded by the chip select lines. (CS0-CS2).

All of the registers are readable so that the controller can determine the present state of the AY-3-8910.

SYSTEM DIAGRAM



PIN FUNCTIONS

Signal	Functional Description
Clock (input)	2MHz Clock—this input is a reference for timing within the AY-3-8910.
DA0-DA7 (input/output)	Data/Address Bus Bits 0-7 — this 8-bit bus passes all data and address information between the AY-3-8910 and the controller.
CS0-CS2 (input)	Chip Select Lines—a three bit code on these lines selects the AY-3-8910 for sound programming or parallel input/output.
BC1, BC2, BD1R (input)	Bus Control Signals (ref. Fig. 7) — generated by the controller these lines decoded within the AY-3-8910 to control all bus operations.
$\overline{\text{RESET}}$ (input)	Reset — clears the AY-3-8910 on power up.
IOA0-IOA7 (input/output) IOB0-IOB7 (input/output)	Parallel Input/Output Ports—each of these ports provide 8 bits of parallel data for use by the external world. These ports are each programmable for either input or output and are TTL compatible.
ANALOG A, B, C (outputs)	Analog Outputs — each of these outputs are independently programmable to produce complex sounds.
TEST	For GI test-normally not connected.

16 REGISTER MEMORY MAP FOR AY-3-8910

REGISTER		B7	B6	B5	B4	B3	B2	B1	B0
R0	Channel A Period	8-BIT Fine Tune							
R1	Channel B Period	8-BIT Fine Tune							
R2	Channel C Period	8-BIT Fine Tune							
R3	Envelope Period	8-BIT Fine Tune							
R4	Channel A Period	4-BIT Course Tune							
R5	Channel B Period	4-BIT Course Tune							
R6	Channel C Period	4-BIT Course Tune							
R7	Envelope Period	8-BIT Course Tune							
R10	Enable	IOB OUT	IOA OUT	Noise $\overline{C}$	Noise $\overline{B}$	Noise $\overline{A}$	Tone $\overline{C}$	Tone $\overline{B}$	Tone $\overline{A}$
R11	Noise Gen. Clock				5-BIT Period Control				
R12	Envelope Control					CON.	ATT.	ALT.	HOLD
R13	Channel A								
R14	Channel B			C1	C0	D3	D2	D1	D0
R15	Channel C								
R16	IOA	8-BIT PARALLEL I/O on Port A							
R17	IOB	8-BIT PARALLEL I/O on Port B							

NOTE: For Registers 13, 14, 15

C1	C0	Expected Output (LOG AMPLITUDE)				
1	1	E3	E2	E1	E0	(Ref. Figs. 1 and 2)
1	0	0	E3	E2	E1	
0	1	0	0	E3	E2	
0	0	D3	D2	D1	D0	

WHERE: E3 E2 E1 E0 Come From the Envelope Generator
D3 D2 D1 D0 Are the Lower 4 BITS of R13, R14, R15
C1 C0 Are the Upper 2 BITS of R13, R14, R15

Channel A, B, C Is Shut off by Zeroing R13, R14, R15 Respectively.

REGISTER # (octal)	ADDRESS (octal)	BITS	FUNCTION NAME	DESCRIPTION
R0	Base	8	f0	Fine tunes frequency on channel A. 8 bits are proportional to period.
R1	Base + 1	8	f1	Similar to f0 but channel B.
R2	Base + 2	8	f2	Similar to f0 but channel C.
R3	Base + 3	8	fE	Fine tunes envelope period.
R4	Base + 4	4	P0	Coarse tunes channel A (high four bits).
R5	Base + 5	4	P1	Coarse tunes channel B (high four bits).
R6	Base + 6	4	P2	Coarse tunes channel C (high four bits).
R7	Base + 7	8	PE	Coarse tunes the envelope period.
R10	Base + 10	8	$\overline{\text{Enable}}$	Each bit controls a unique function (active low): Bit 0: Tone on channel A. Bit 1: Tone on channel B. Bit 2: Tone on channel C. Bit 3: Noise on channel A. Bit 4: Noise on channel B. Bit 5: Noise on channel C. Bit 6: IOA, 0 for input, 1 for ouput. Bit 7: IOB, 0 for input, 1 for output.
R11	Base + 11	5	N Clock	Varies the frequency of the clock for the noise generator.
R12	Base + 12	4	Envelope Control	Each bit controls a function in the envelope generator: Bit 0: Hold. Holds the last count of the specified envelope. Bit 1: Alternate. The amplitude of the envelope generator cycles up and then down. Bit 2: Attack. When high, the envelope will attack. When low, the envelope will decay. Bit 3: Continue. When high, the analog output will not shut off after one cycle. When low, the analog output shuts off after one cycle.
R13	Base + 13	6	Envelope A	Each of these registers controls its respective envelope in the following way (also refer to Note in memory map above): Bit D0 - Bit D3 - These bits directly control the amplitude of each analog output when bits 4 and 5 are low.
R14	Base + 14	6	Envelope B	
R15	Base + 15	6	Envelope C	
R16	Base + 16	8	IOA	With the control bits of R10 set for the output mode, data can be written to these ports from the CPU, and latched. With the control bits set for input, data can be read into the CPU. Each port is independently programmable.
R17	Base + 17	8	IOB	

TV GAMES

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other input and output voltages with respect to V_{SS} ..... −0.3°C to +8.0V

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

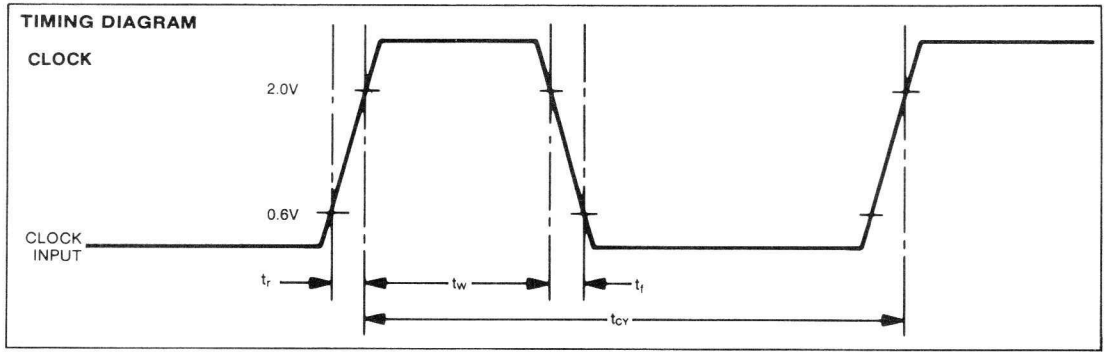
STANDARD CONDITIONS (unless otherwise noted)

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature: 0°C to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Units	Conditions
DC CHARACTERISTICS						
Power Supply Current	I_{CC}	–	45	75	mA	
Logic Inputs (all inputs)						
Low	V_{IL}	0	–	.6	V	
High	V_{IH}	2.4	–	V_{CC}	V	
Logic Outputs (all outputs except Analog outputs)						
Low	V_{OL}	0	–	.55	V	I_{OL} = 1.6 mA
High	V_{OH}	2.4	–	V_{CC}	V	I_{OH} = 100 μA
Leakage (A0-A7, B0-B7, DA0-DA7)	I_{OH}	–	TBD	–	μA	
Logic Outputs (Analog Outputs)						
Low	V_{OL}	–	TBD	–	V	
High	V_{OH}	–	TBD	–	V	
AC CHARACTERISTICS						
Clock Input						
Period	t_{CY}	500	–	750	ns	
Rise time	t_r	–	–	50	ns	
Fall time	t_f	–	–	50	ns	
Pulse width	t_W	–	–	150	ns	
DA0-7 Bus Signals						
Output delay from bus control (tristate to output)	t_{DA}	–	–	250	ns	
Output delay from bus control (output to tristate)	t_{OH}	20	–	100	ns	
Input hold time after BDIR	t_{IH}	100	–	–	ns	
Input Pulse width	t_{IW}	300	–	–	ns	
Input Setup time	t_{IA}	–	TBD	750	ns	
Data Input Setup time	t_{DI}	–	–	750	ns	
Data Input Hold time	t_{DH}	100	–	–	ns	
Data Write Pulse	t_{DW}	1.5	–	–	μs	
Analog Outputs	–	–	TBD	–	–	

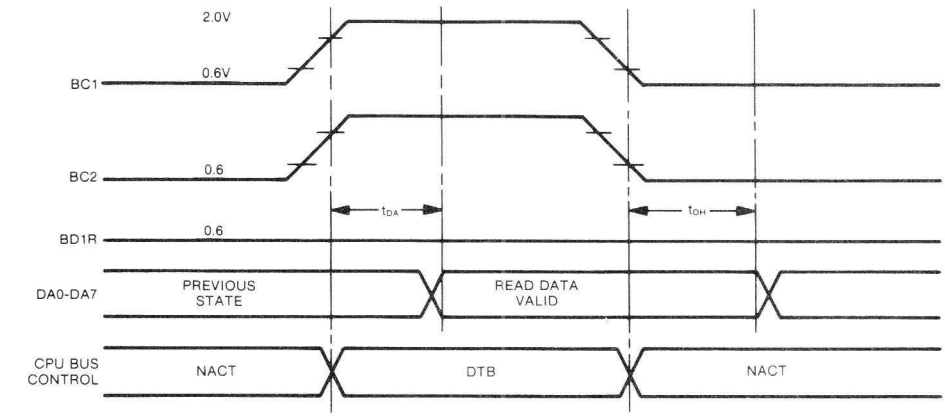
**Typical values are at 25°C and nominal voltages.

TIMING DIAGRAM

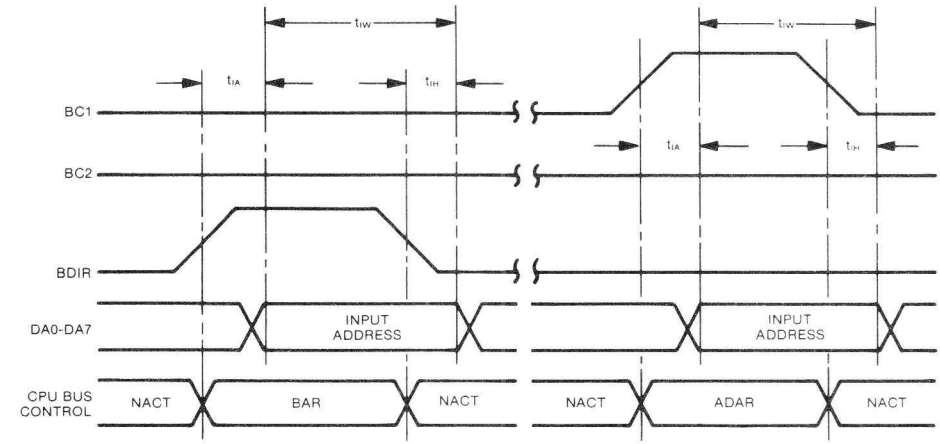


TIMING DIAGRAMS

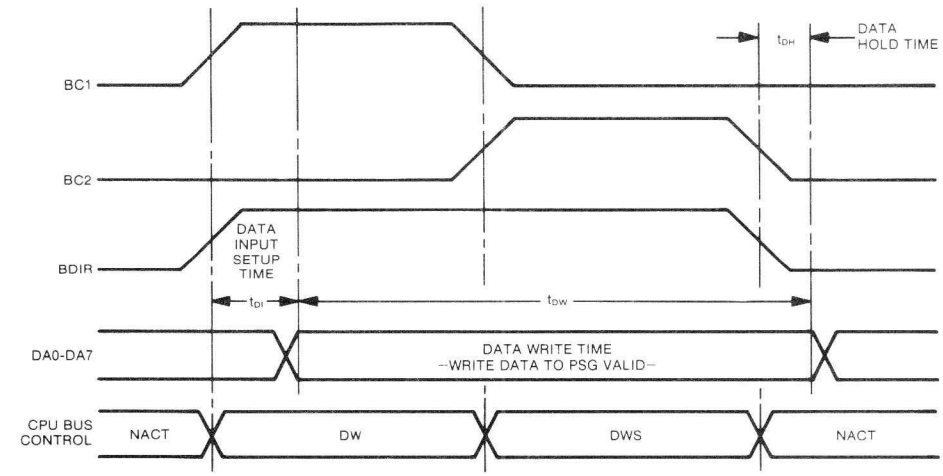
READ BUS TIMING



ADDRESS BUS TIMING



DATA WRITE TIMING



TV GAMES

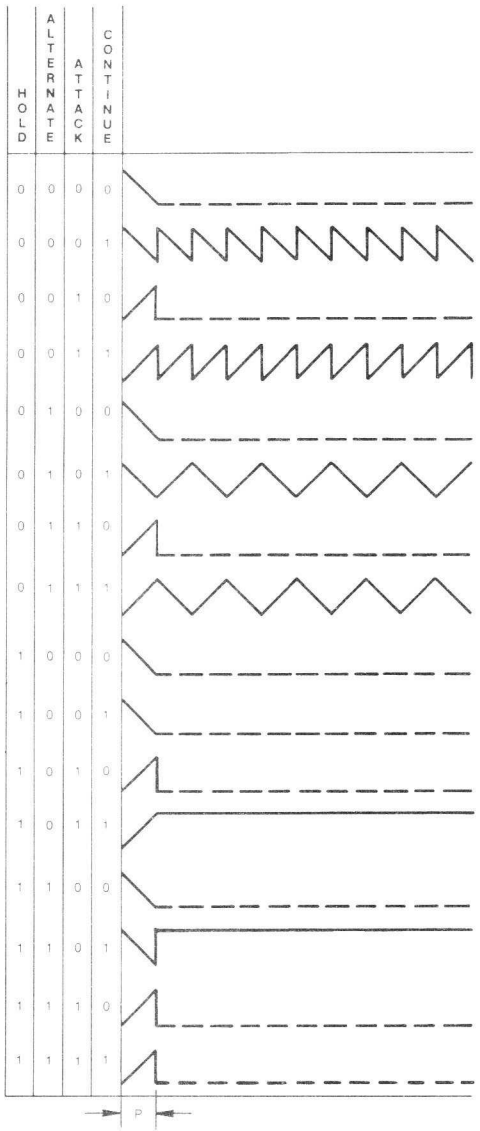


Fig.1 SAMPLE OF SOME WAVEFORMS AVAILABLE FROM THE ENVELOPE GENERATOR.

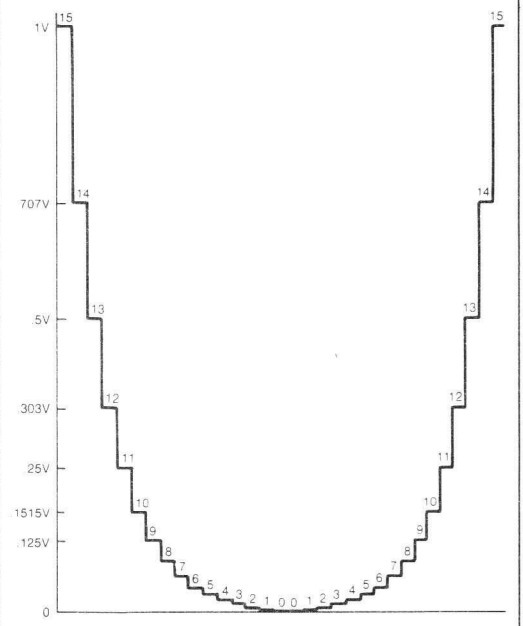


Fig.2 IDEAL LOGARITHMIC OUTPUT OF D/A CONVERTER WITH NO MUTING

TYPICAL OUTPUT WAVEFORMS

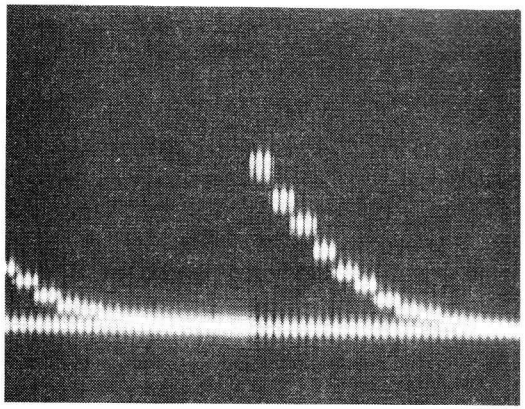


Fig. 3 $R0_8 = 14_8$, $R3_8 = 37_8$, $R12_8 = 10_8$, $R13_8 = 77_8$, ALL OTHER REGISTERS = 0.

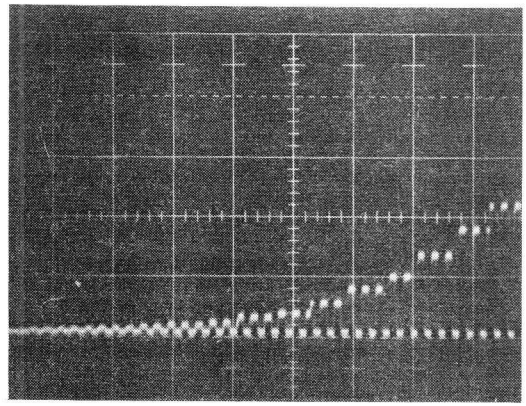


Fig. 4 $R12_8 = 14_8$, ALL OTHER REGISTERS SAME AS Fig. 3.

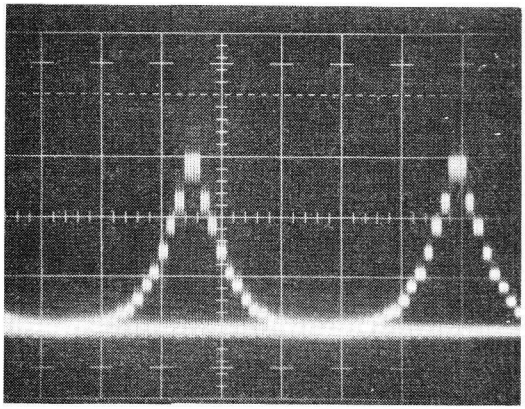


Fig. 5 $R12_8 = 12_8$, ALL OTHER REGISTERS SAME AS Fig. 3.

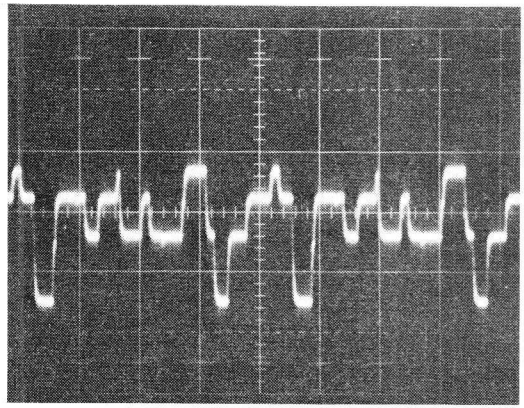


Fig. 6 MIXTURE OF 3 FREQUENCIES WITH PRESET AMPLITUDES.

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion.
0	0	1	IAB	Interrupt Address to Bus.
0	1	0	ADAR	Address Data to Address Register.
0	1	1	DTB	Data to Bus.
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

Fig. 7 BUS CONTROL SIGNALS

GIMINI Deluxe "8900" Programmable Game System

FEATURES

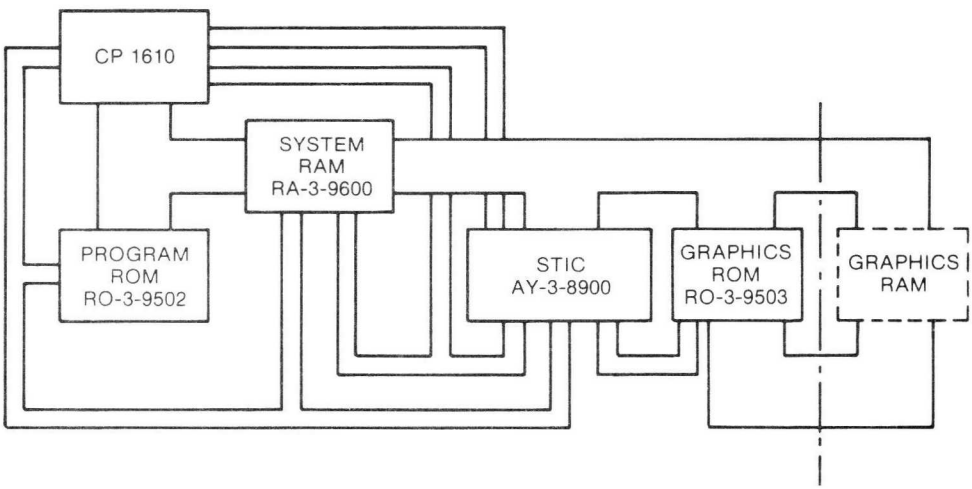
- Infinite game selection
- Lowest cost expandable system
- Uses programmable 20K ROMs
- Eight color selectable, coordinate addressable game objects on a grid of 160H by 96V.
- Resident library of 256 complex game objects, including full 64 character alpha numerics
- Shape library extenable by a further 256 objects using graphics RAM.
- Full multicolor background capability
- Sixteen selectable color tones
- Program controllable moving background
- Two hundred and forty independently programmable background locations

DESCRIPTION

The GIMINI 8900 system is based on two processors; one computes the game action against the stored program rules; and the second interprets a condensed memory area and uses this to generate the T.V. raster display. The second processor fetches moving and background pictures from the graphic picture storage and presents the data as a video output.

The set consists of five General Instrument supplied N-Channel circuits. The AY-3-8900 Standard Television Interface Circuit (STIC); the CP1610 GIMINI Microprocessor; an RO-3-9502 20K program ROM; a similar RO-3-9503 graphics picture ROM and an RA-3-9600 RAM. To complete the system the user supplies clocking and modulation circuitry plus any other peripheral control requirements.

8900 SYSTEM DIAGRAM



8900 SYSTEM COMPONENTS

DESCRIPTION	PART NUMBER	GAME FUNCTION	PACKAGE	FEATURES
BASIC COMPONENTS: A complete microprocessor programmable game with only 5 LSI chips, the GIMINI Deluxe "8900" offers the capability for maximum game flexibility with detailed graphics definition and manipulation.	**CP1610**	MICROPROCESSOR	40 DIP	A full 16-bit microprocessor for processing all game data.
	AY-3-8900	TV INTERFACE	40 DIP	Processes graphics data and generates all video signals.
	AY-3-8900-1			
	RO-3-9502	PROGRAM ROM	40 DIP	A 2048 x 10 ROM which contains the executive program.
	RO-3-9503	GRAPHICS ROM	40 DIP	A 2048 x 8 ROM which stores 256 - 8 x 8 graphics characters.
	RA-3-9600	SYSTEM RAM	40 DIP	Contains a 352 x 16 memory plus a 20 word "current line" buffer.
OPTIONAL COMPONENTS: The basic "8900" system can easily be expanded to include additional games plus software-controlled graphics interaction, complex sound generation, and supplementary peripherals.	**RO-3-9500**	CARTRIDGE ROM	28 DIP	A 2048 x 10 ROM which contains additional game programs.
	2112A/2114	PROGRAM/ GRAPHICS RAM	16/18 DIP	Customer-supplied 256 x 4 or 1K x 4 RAMs to increase system capabilities.
	AY-3-8910	SOUND GENERATOR	40 DIP	Provides programmed generation of complex sound effects.
	AY-3-8915	COLOR PROCESSOR	16 DIP	Generates a single composite color signal from AY-3-8900-1 digital input.
	AY-3-8920	TAPE CASSETTE INTERFACE	40 DIP	Interfaces system to standard audio cassette decks.
	IOB 1680	INPUT/OUTPUT BUFFER	40 DIP	General purpose buffer for keyboards, displays etc.

BASIC COMPONENTS

A. CP1610: 16-Bit Single-Chip Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 87 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory access using all address modes
- TTL compatible/simple bus structure
- 1 μs cycle time, 2 MHz 2-phase clock

DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories, and Random Access Read/Write Memories are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/ home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program, memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

B. AY-3-8900/AY-3-8900-1: Standard Television Interface

FEATURES: FOREGROUND OBJECTS

- Eight truly general purpose objects
- Coordinate positioned 160 H by 96V
- Object drawn from programmable library (32 angles)
- Zoom facilities in X and Y
- Priority draw feature
- Full interaction logic

FEATURES: BACKGROUND OBJECTS

- 20 × 12 background matrix of 8 × 8 squares
- All 240 locations drawn from library
- Grouping facility for large objects
- Moving effect in X and Y to full resolution
- Background may be changed by microprocessor during draw sequence
- Colored squares feature 960 independently colored areas

DESCRIPTION

The STIC circuit is the video processor which fetches, decodes and displays moving and background characters stored in the library for T.V. presentation under program control. During active picture time, interactions between shapes are recorded for interrogation by the CP1610 on completion of the current frame. The picture generation of the STIC can be separated into the two areas of background objects and moving objects. In operation, the 240 words of background RAM are loaded as required during the active period of picture time and a special buffer area allows both the STIC and the CP1610 to run together. The control data for the eight moving objects is stored within the STIC itself and it is accessed by the CP1610 only during the frame flyback period. All data is statically held and only needs to be updated on a picture change. In addition to the moving object data, the STIC also stores the border color, the background offset for moving background effects and a four-deep cyclic stack of background colors. If the optional graphics RAM is also wired into the system, the CP1610 can access this area during the vertical retrace period via the system bus and some special STIC connections. An additional control code can extend the CPU time for system access as the program demands.

C. RO-3-9502: Program ROM

FEATURES

- 2048 × 10 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 65K of external RAM
- Internal address status and data bits latched
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION

The 20K program ROM is organized into 2048 10 bit words to control the CP1610 operation. In addition to the stored program function, the circuit contains a 16 bit latched output port which supplies an address bus to any standard memory circuits which may be added by the user. An example of this addition would be a buffer store for a cassette tape reader. The program also supplies enable and read/write signals for the standard memory.

On master reset or for the end of active picture interrupt, the program ROM supplies the interrupt address to the CP1610.

D. RO-3-9503: Graphics ROM

FEATURES

- 2048 × 8 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Output address latches and control signals generated for controlling up to 2K of external RAM
- Internal address status and data bits latched
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

DESCRIPTION

The 16K graphics ROM is a similar device to the program ROM, but is organized into 256 8×8 bit characters which are the dot patterns for background and moving objects. The set contains the full 64 character alpha-numeric and the other characters may be grouped by the user to have some program significance, although any character can be drawn in any mode.

The graphics ROM is accessed under two conditions, moving objects and background objects. For backgrounds, the RAM device sequentially outputs 14 bit words and 8 bits of this word defines one of the 256 stored characters. The STIC outputs a further 3 bits to define which line of the 8×8 bit matrix is being accessed. This 11 bit address is latched into the graphics ROM including a higher order bit which signifies if graphics ROM or RAM is to be accessed.

E. RA-3-9600: System RAM

FEATURES

- Sufficient memory storage to hold complete STIC background display (240 words of 14 bits).
- Sufficient memory storage to provide useful Scratch pad area for CP1610 microprocessor (112 words of 16 bits).
- Address latch for CP1610.
- Control decoder for CP1610.
- Address latch for STIC.
- Current line buffer for 8900 game system (20 words of 14 bits).

DESCRIPTION

The system RAM is an optimized structure device which allows maximum processor time for both game and graphics processors and it allows the user to run operational programs with only a single RAM package in the system. The RAM contains its own control decoding and address latch for both the CP1610 and the STIC. The two processors run on a semi-time shared basis with the RAM providing the data buffer.

The RAM is organized with 240 words holding the background picture data and 112 words being available to the CP1610 for general purpose scratchpad. The background storage area may be accessed by the CP1610 during the active picture time, which allows the user to run very complex, high density background displays.

OPTIONAL COMPONENTS

A. RO-3-9500: Cartridge ROM

The RO-3-9500 is a similar device to the RO-3-9502 Program ROM except that facilites for the control of external RAM are not provided. This allows for the packaging of this 20K ROM in a 28 pin DIP for use as a "satellite" or cartridge ROM for expansion of the 8900 system functions. A 40 lead 9502 may also be used in the "satellite" position if desired.

B. 2112/2114: Program/Graphics RAM

User-supplied standard RAMs, such as the 2112A (256 × 4) or 2114 (1K × 4), may be added to the 8900 system for use as either additional Program storage or Graphics RAM.

A typical use of expanded Program RAM would consist of the requirement for buffer memory for a tape cassette reader.

By adding RAM area to the graphics picture storage of the GIMINI 8900 system, this will allow the user to load and modify the dot pattern of the pictures under program control. Effects such as large background objects covering several 8 × 8 bit squares and individual background movement may be achieved with a graphics RAM system.

C. AY-3-8910: Programmable Sound Generator

The AY-3-8910 is a Large Scale Integrated Circuit that can produce a wide variety of complex sounds under software control. It is easily interfaced to most 8 and 16-bit microprocessors; however, it is optimally designed to directly connect to the CP1600 series of microprocessors. The flexibility of the AY-3-8910 makes it useful in applications such as music synthesis, sound effects, audible alarms, and FSK modems. In addition, once interfaced, the AY-3-8910 provides the microprocessor with two parallel 8-bit bi-directional data ports that are TTL compatible. The analog sound outputs can each provide 4 bits of logarithmic D/A conversion.

The AY-3-8910 is manufactured in the N-Channel Ion Implant process. Operation requires a single 5V supply, a 2 MHz TTL clock and a microprocessor controller such as the 1600 series.

D. AY-3-8915: Color Processor

The AY-3-8915 color processor is intended to be interfaced with the 8900 game system. The interface control is carried on a five wire bus where one line performs an option switch relative to the operation of the other four lines. The 8915 also provides a 3.58 MHz clock to the 8900 chip.

The effect of this "control" line is to produce two distinct operating modes. In mode one, the 8900 chip will be in the active line condition and attempting to draw some combination of background and foreground objects onto the telvision screen. The required color to be displayed is output from the 8900 on a four-line binary coded bus. This selects one from sixteen colors as defined by the game program being excecuted within the 8900 system.

With the control line in the mode two position, the four line bus is used to carry synchronizing infromation from the 8900 to the 8915. The four wires carry composite sync, color burst, line blanking and frame blanking. The operation of the 8915 driving mode two is such that the lines are decoded by the hardwired logic and then presented to a small ROM, which programs the correct level for each of the signals.

E. AY-3-8920: Tape Cassette Interface

The AY-3-8920 is intended to provide full interface and control signals between the 8900 system and a standard cassette drive.

F. IOB 1680: Input/Output Buffer

The IOB1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing facilities for the 8900 system with a minimum of additional components. The circuit is fabricated in General Instrument N-Channel Ion Implant GIANT II process insuring high performance, with proven reliability and production history.

The IOB1680 enables efficient interfacing between a peripheral and the CP1610 by the use of six 8-bit registers and a 16-bit programmable timer. Two of the 8-bit registers are a buffer store between the CP1610 and the bidirectional I/O lines to peripheral, latching any data sent to them from the CP1610. Three other 8-bit registers hold the Interrupt Vector Addresses associated with I/O, Error Status and the Timer. The Control Register governs the operation and characteristics of the IOB1680 and provides a convenient means for the CP1610 to monitor I/O status information. The 16-bit timer gives the IOB1680 a real time capability which is suitable for confirming system security and for timing peripheral activites. These registers are initialized after power clear by the CP1610 program writing the required Interrupt vector addresses into the appropriate registers. The interrupt vectors may also be altered at any time by program.

CONSUMER 8

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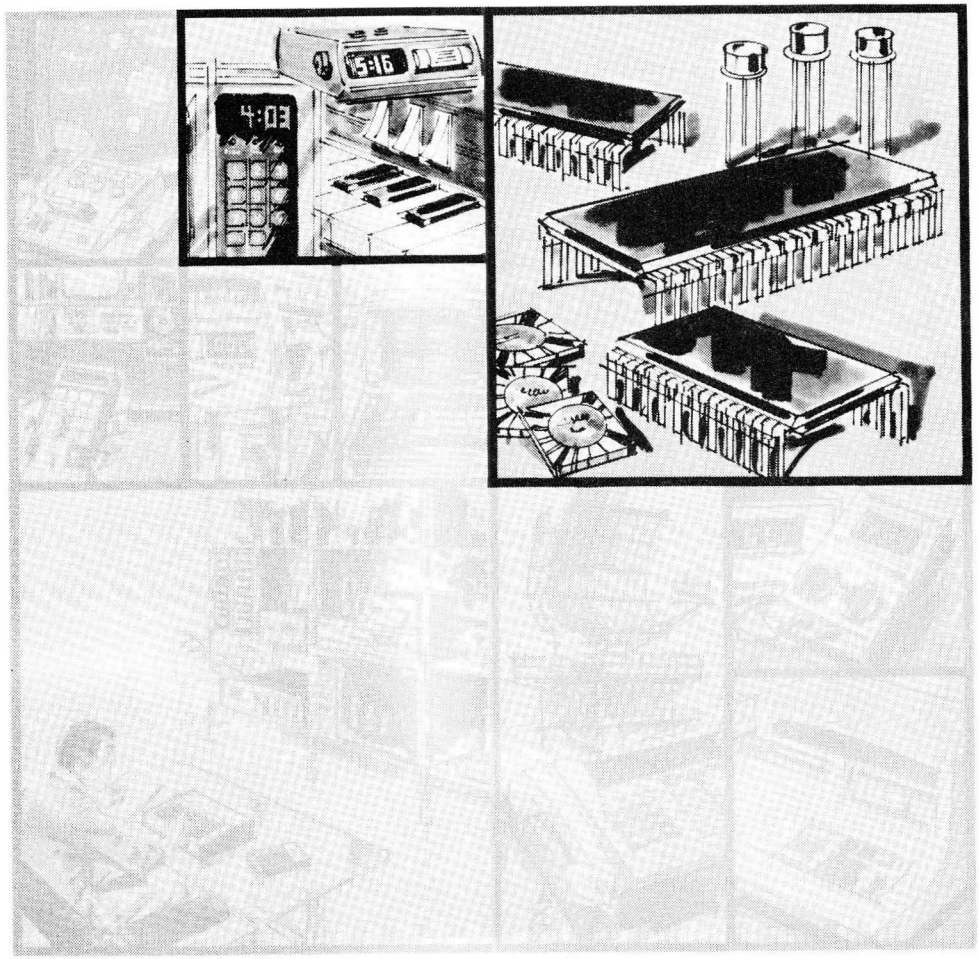


CALCULATORS

FUNCTION	DESCRIPTION	PART NUMBER		PAGE NO.
		$6\frac{1}{2}$-$9\frac{1}{2}$V LED	7-9V LED	
8 DIGIT BASIC	Basic 4 functions and %.	C-683D	C-1683D	8-16
		C-685D	C-1685D	8-16
8 DIGIT ALGEBRA	Basic 4 functions, % x^2 $\sqrt{x}$, 1/x, +/-, memory.	C-687D	C-1687D	8-16
		C-689D	C-1689D	8-16
9 DIGIT SCIENTIFIC	Full 21 function calculator circuit for 15V fluorescent fluorescent displays.	CF-599	—	8-15
12 DIGIT PRINTING	Basic 4 functions and %, decimal select mode, memory-in-use indicator, rounding options, non- and (#)/ date key, and other features.	C-717X	—	8-18
		C-718	—	8-19
		C-1720	—	8-20
DISPLAY INTERFACE	Adds display capability to above printing calculators.	C-719	—	8-21

Display Calculator Circuits

FEATURES

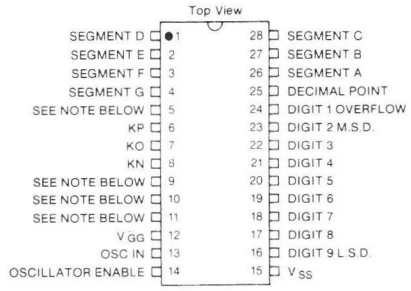
- Printed circuit board compatibility of circuits.
- Direct segment drive for LED displays (C-XXX)
- Direct fluorescent display drive (CF-XXX)
- Direct segment and digit drive for LED display (C-6XXD and C-16XXD)
- Algebraic operation
- Automatic constant
- Floating point operation
- Constant or chain operation (no switch required)
- Leading zero suppression
- Automatic power-on clear
- Internal clock (on-chip oscillator)
- Internal keyboard debounce logic

DESCRIPTION

General Instrument's broad line of display calculator circuits, the C/CF-500 Series and the C/CF-600 Series, consists of pin-for-pin compatible circuits (except C-6XXD and C-16XXD series) designed to fit in the same basic PC board. This provides a high degree of flexibility in calculator models manufactured while minimizing the tooling required.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



NOTE:
All Display Calculator circuits offered by General Instrument (except C-6XXD and C-16XXD series) have identical pin functions on all pins except pins 5, 9, 10 and 11. These pins are utilized for the distinctive functions of each calculator circuit model as described on the following pages of this section.

FUNCTION	DESCRIPTION	9V LED	9V FLUOR.	9V LED DIRECT DRIVE		15V FLUOR.	15V LED
8 DIGIT BASIC	4 functions and percent key.	C-683	CF-683	C-683D	C-1683D	CF-583	C-583
	4 functions, percent key, one-key or multi-key memory.	C-685	CF-685	C-685D	C-1685D	CF-585	C-585
8 DIGIT ALGEBRA	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/−, one-key or multi-key memory, choice of 20 to 29 keys.		CF-687	C-687D	C-1687D	CF-589	C-589
	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/−, one-key or multi-key memory, brackets, inch-centimeter conversion, choice of 24 to 30 keys.		CF-689	C-689D	C-1689D	CF-689HV	—
9 DIGIT BASIC	4 functions and percent key.					CF-593	C-593
	4 functions, percent key, one-key memory.					CF-594	C-594
	4 functions, percent key, multi-key memory.					CF-595	C-595
9 DIGIT SCIENTIFIC	Basic 4 functions, scientific notation, sin, cos, tan, arc sin, arc cos, arc tan, memory, square root, pi, natural logs, 1/x, e^x, memory exchange, degrees and radians, exponent range ± 99, choice of 19 to 35 keys.					CF-596	C-596
	All the above plus: 0 to 10^{99} degree trig range, $\log_{10}$, y^x, extended digit accuracy of transcendentals, choice of 21 to 38 keys.					CF-598	C-598
	All the above plus: two levels of parenthesis, x^2, %, +/−, choice of 24 to 41 keys.					CF-599	C-599

I THE FOLLOWING APPLY AS NOTED:

A. AUTOMATIC CONSTANT (All circuits)

The answer from any operation is entered automatically as a Constant by the = key without a constant switch. The Constant may then be used with all five functions and the answer from any Constant calculation can be used for further calculations without re-entry. This provides an extremely powerful facility for solving many complex equations without the need for writing down or remembering intermediate results. It is particularly useful for raising to a power, compound interest calculations, nth roots, depreciation calculations, etc. In constant multiplication, the constant is the first entered number (constant multiplicand). In division, addition and subtraction, the constant is the second entered number. The completion of the first operation with the depression of the = key initiates the storage of the constant number. For subsequent operations it is only necessary to enter a number and depress the = key.

B. DECIMAL ALIGNMENT (C/CF-593, C/CF-594, C/CF-595)

The results of addition or subtraction will remain aligned to the preceding number having the most decimal places. This feature allows computation in the dollar and cents mode without suppression of the zeros to the right of the decimal point. If a right shift is needed to keep the eight most significant digits, the least significant digits are lost. The results of multiplication and division will be completely right adjusted such that only the most significant digits are displayed except during overflow.

C. CAPACITY (All except Scientific Circuits)

For the C/CF-580 Series and the C/CF-680 Series, in the case of overflow, the eight most significant digits are displayed (seven digits and minus sign for negative answers) all decimal points are lit and the keyboard is locked out. Only the operation of the clear key will allow continued operation. On depression of the clear key, the decimal point is shifted eight places to the left of its actual position.

For the C/CF-593, 594 and 595, in the case of overflow, the overflow symbol is displayed, and the decimal point shifted eight places to the left of its actual position. Under these conditions, the keyboard is locked out such that only the operation of the clear key will allow continued operation.

In all cases, for an attempted entry requiring more than eight display digits, the most significant digits are protected upon the attempted entry of another digit. The keyboard is not locked out and operations are still able to be performed.

When division by zero is attempted, an overflow condition results and a zero is displayed.

D. PERCENT KEY (all except C/CF-596 and 598)

Multiplies the two preceding entries and divides by 100, and when followed by = gives add-on and discount: A+B% yields (AB/100); A+B%=yields A+(AB/100). A−B% yields (AB/100), A−B%=yields A−(AB/100).

E. CHANGE NOTATION KEY (Scientific Circuits)

Depression of the CHG NOT key will convert the displayed number to scientific notation, if it is in the "normal" mode, or it will display the 8 most significant digits of a scientific mantissa with the decimal point correctly located (even if it falls beyond the display area) and trailing zeroes shall be blanked. In addition, for numbers less than one, the digits are left shifted until all leading zeroes have been eliminated.

F. EXPONENT KEY (Scientific Circuits)

EEX: This key operates as follows: The EEX key sets the two right most digits to zero, the third digit from the right is blanked and the calculator is conditioned to accept sign and numeral keys to define the exponent value of the number entry. If the mantissa had numbers in any of the last three digit positions, these are retained but not displayed.

G. FUNCTION KEY OPERATIONS (Used only with dual-function keys)

Depression of the F key sets the calculator in the "Function" mode and the F indicator is lit. The dual function keys will then function as indicated by their upper case designation. Single function keys directly perform the indicated function.

Depression of the second key of the sequence resets the "Function" mode and the F indicator is turned off when the answer is displayed. The "Function" mode can also be reset by a second depression of the F key.

II THE FOLLOWING APPLY AS NOTED TO CIRCUITS WITH MEMORY:

A. MEMORY DESCRIPTION: One-Key memory as provided in C/CF-585, 589, 594, 685, C-685D, 687D, 689D, 1685D, 1687D, 1689D, and CF-689.

M: The Memory key is used in conjunction with other function keys to define a two key sequence which sets a mode of operation associated with the memory register and terminates any immediately preceding entry.

Operation of the M key followed by + adds the contents of the display register to the memory register without altering the contents of the display register.

Operation of the M key followed by − subtracts the contents of the display register without altering the contents of the display register.

Operation of the M key followed by = transfers the contents of the memory register into the display register without altering the contents of the memory register.

Operation of the M key followed by C/CE clears the contents of the memory register.

Operation of the M key followed by the X key performs a memory-display exchange function. The contents of the memory register are brought out to the display register and the contents of the display register are written into the memory register, replacing the previous contents of the memory register.

Operation of the M key followed by any key other than +, −, X, =, or C/CE shall reset the M condition and act upon the subsequent entry as if the M had not been entered.

In addition, two optional keys are provided with the C/CF-594 for operation as follows:

MR, MEMORY READ: Functions identically to the M = sequence above.

MC, MEMORY CLEAR: Functions identically to the M C/CE sequence above.

B. MEMORY DESCRIPTION: Multi-key memory as provided in all algebra, scientific circuits, and C-685D.

MR, MEMORY READ: Functions identically to the M = sequence above.

MC, MEMORY CLEAR: Functions identically to the M C/E sequence above.

M+, MEMORY PLUS: Functions identically to the M+ sequence above.

M−, MEMORY MINUS: Functions identically to the M− sequence above.

MEX, MEMORY EXCHANGE: Functions identically to the MX sequence above.

In addition, the C/CF-589 are provided with a STORE key which transfers the contents of the display to memory without changing the display.

C. MEMORY DESCRIPTION: Multi-key memory as provided in C/CF-585, 595 and 685.

MC, MEMORY CLEAR: clears the memory while leaving the display intact.

MR, MEMORY READ: transfers the data in memory to the display without changing the memory.

M∓, MEMORY EQUALS/PLUS: completes the preceding operation, displays the result, and adds the result to the memory.

M=, MEMORY EQUALS/MINUS: completes the preceding operation, displays the result and subtracts the result from the memory.

In addition, the C/CF-585 and C/CF-685 are provided with a MEX (Memory Exchange) Key which functions as previously described.

The C/CF-595 is provided with the following additional memory keys:

MR/MC, MEMORY READ/MEMORY CLEAR: this single key operation transfers the memory data to the display on the first depression. When depressed two successive times, the memory data is transferred to the display and the memory cleared.

Σ, SUM KEY: when connected to V_{SS}, this accumulate switch, independent of the keyboard, adds the contents of the display to memory with each depression of the equals key.

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*	Fluorescent Display CF-5XX Series	LED Display C-5XX Series	Fluorescent Display CF-6XX Series	LED Display C-6XX/ C-6XXD/C-16XXD Series
V_{GG} supply voltage range[1]	−20V to +0.3V	−20V to +0.3V	−15V to +0.3V	−15V to +0.3V
Clock input voltage range[1]	−20V to +0.3V	−20V to +0.3V	−15V to +0.3V	−15V to +0.3V
Data input voltage range[1]	−32V to +0.3V	−20V to +0.3V	−30V to +0.3V	−15V to +0.3V
Applied output voltage range[1]	−32V to +0.3V	−20V to +0.3V	−30V to +0.3V	−15V to +0.3V
Maximum power dissipation at +25° C[2]	500 mW			
Storage temperature range	−20° C to +70° C			
Operating free-air temperature range	0° C to +40° C			
Relative humidity range (no condensation)	0 to 95%			

All inputs and outputs are internally protected against static charge damage during handling consistent with standard industry practices.

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

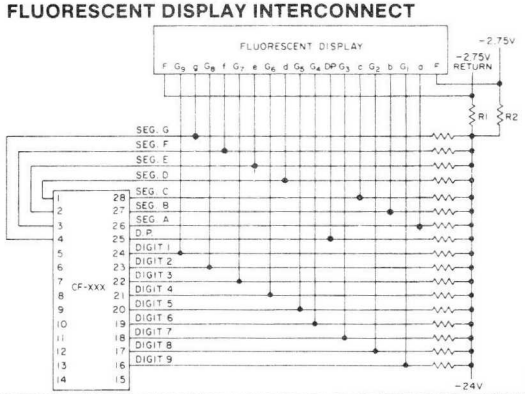
[1] Measured with respect to V_{SS}.
[2] Derate at 10mW/° C.

Operating Conditions	CF-5XX Series Range	C-5XX Series Range	C/CF-6XX Series Min.	Typ.*	Max.	C-6XXD/C-16XXD Series Min.	Typ.*	Max.
V_{SS}, substrate supply	0V	0V		0V			0V	
V_{GG}, gate supply: C/CF-5XXA	−15.0V±5%	−15.0V±5%		—			—	
C/CF-5XXB	−16.0V±5%	−16.0V±5%		—			—	
C/CF-5XXC	−17.0V±5%	−17.0V±5%		—			—	
C/CF-6XXA	—	—	−10.3V	−7.5V	−6.5V			
C/CF-6XXB, C-6XXD	—	—	−9.5V	−7.5V	−6.5V	−9.5V	−7.5V	−6.5V
C-16XXD						−9.0V	−7.5V	−7.0V

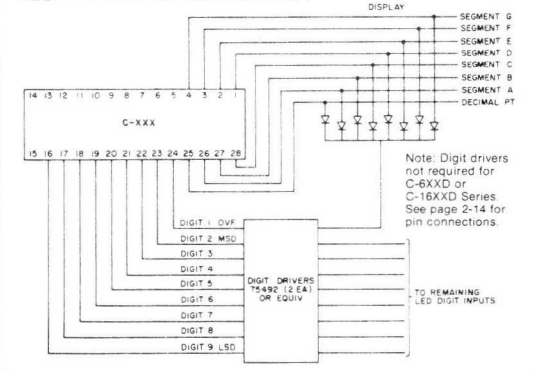
Characteristics- at typical operating conditions over a 0° C to +40° C range.	CF-5XX/6XX Series Min.	Typ.*	Max.	C-5XX Series Min.	Typ.*	Max.	C-6XX Series Min.	Typ.*	Max.	C-6XXD/C-16XXD Series Min.	Typ.*	Max.
Keyboard input characteristics-												
Input signal levels: Logic 0	−1.5V	—	0V	−1.5V	—	0V	−0.5V	—	0V	−0.5V	—	0V
Logic 1	V_{GG}	—	−6.0V	V_{GG}	—	−6.0V	V_{GG}	—	−4.0V	V_{GG}	—	−4.0V
Keyboard resistance	—	—	1K	—	—	1K	—	—	1K	—	—	1K
Output buffer characteristics-[3]												
Segment output on-resistance: at −0.5V V_{OUT}	—	—	—	—	—	—	—	200Ω	300Ω	—	1K	1.3K[4]
at −1.5V V_{OUT}	—	200Ω	600Ω	—	200Ω	300Ω	—	—	—	—	—	—
Digit output on-resistance at −1.5V V_{OUT}	—	200Ω	300Ω	—	200Ω	300Ω	—	200Ω	300Ω	—	30Ω	50Ω[5]
Digit and segment off-leakage: at V_{OUT}=−9V	—	—	—	—	—	18μA	—	—	18μA	—	—	100μA[6]
at V_{OUT}=−27V (CF-590, CF-680 Series) or V_{OUT}=−30V (CF-580 Series).	—	—	18μA	—	—	—	—	—	—	—	—	—
Anode and grid supply voltage through 200K resistor: CF-580 Series	−30V	−24V	—	—	—	—	—	—	—	—	—	—
CF-590, CF-680 Series	−27V	−24V	—	—	—	—	—	—	—	—	—	—
Power (all outputs off)-												
at V_{GG}=−16.0V, C/CF-580 Series	—	75mW	100mW	—	75mW	100mW	—	—	—	—	—	—
at V_{GG}=−16.0V, C/CF-590 Series	—	100mW	125mW	—	100mW	125mW	—	—	—	—	—	—
at V_{GG}=−7.5V, C-680 Series	—	—	—	—	—	—	—	15mW	30mW	—	15mW	30mW

[3] All output buffers are open-drain to V_{SS}.
* Typical values are at +25° C and nominal voltages.
[4] At 4mA.
[5] At 36mA.
[6] At −9V

FLUORESCENT DISPLAY INTERCONNECT



LED DISPLAY INTERCONNECT



8 Digit / 5 Function Basic Calculator Circuits

FEATURES

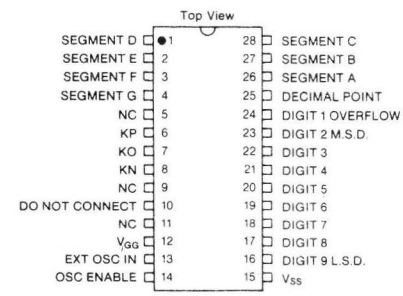
- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- C-583 and C-683: direct LED segment drive.
  CF-583 and CF-683: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-583 and C/CF-683 circuits are basic five-function circuits which may be used with either eight or nine digit LED or fluorescent displays. They compute and display the results of calculations with numbers up to eight digits (seven for negative). On overflow, the keyboard is locked and all decimal points are lighted. In addition, an overflow symbol will appear in the ninth digit position for those calculators having nine digit displays.

PIN CONFIGURATION

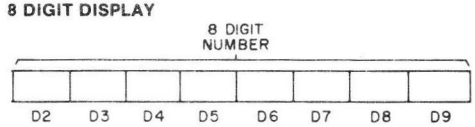
28 LEAD DUAL IN LINE



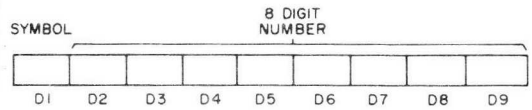
NOTE:
The oscillator is enabled by connecting a resistor from V_{GG} to pin 14 (150K±10% for C/CF-583, 470K±10% for C/CF-683).

DISPLAY

8 DIGIT DISPLAY

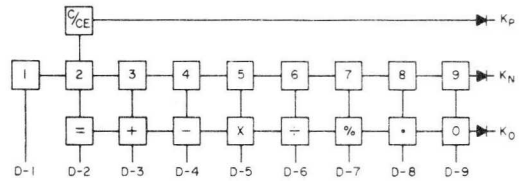


OPTIONAL 9 DIGIT DISPLAY



DISPLAY FONT

KEY MATRIX



Note: Diodes used only for CF-583 and CF-683.

CONSUMER

C-585 C-685
CF-585 CF-685

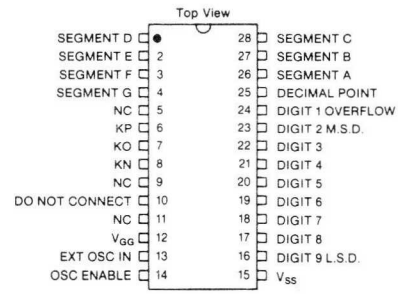
8 Digit / 5 Function Basic Calculator Circuits With One-Key or Multi-Key Memory

FEATURES

- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- One-key or multi-key memory function (refer to the description at the beginning of this section.)
- C-585 and C-685: direct LED segment drive.
  CF-585 and CF-685: direct fluorescent display drive.
- All other features listed on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



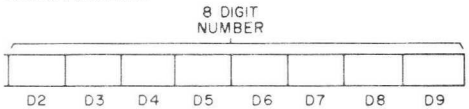
NOTE:
The oscillator is enabled by connecting a resistor from V_{GG} to pin 14 (150K ±10% for C/CF-585, 470K ±10% for C/CF-685).

DESCRIPTION

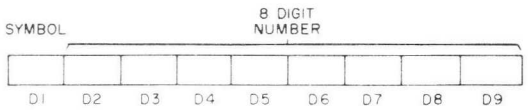
The C/CF-585 and C/CF-685 circuits are basic five-function memory circuits which offer the user the highest degree of functional flexibility in implementing a memory calculator. The circuits include all the features of the C/CF-583 and C/CF-683 circuits with the addition of the memory function.

DISPLAY

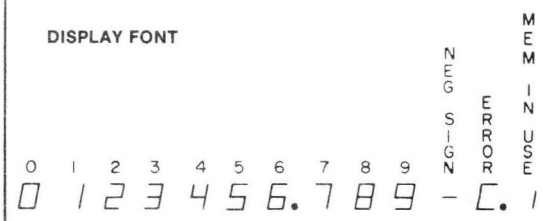
8 DIGIT DISPLAY



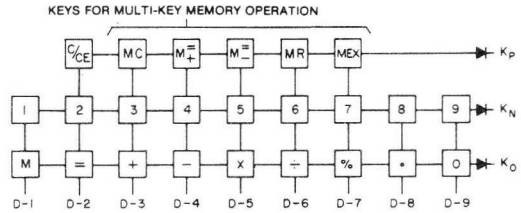
OPTIONAL 9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-585 and CF-685

8 Digit / 9 Function Algebra Calculator Circuits With One-Key or Multi-Key Memory

FEATURES

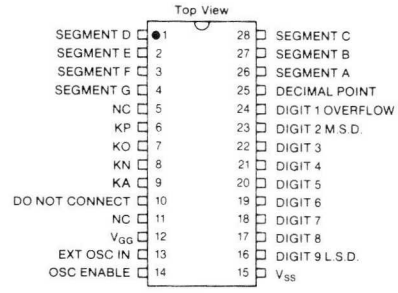
- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Convenience functions (x^2, $\sqrt{x}$, 1/x, +/-)
- Floating negative sign.
- Right-justified entry and result.
- One-key or multi-key memory function (refer to the description at the beginning of this section.)
- C-589: direct LED segment drive.
  CF-589: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-589 circuits are basic eight-function memory circuits which offer the user the highest degree of functional flexibility in implementing a memory calculator. The circuits include all the features of the C/CF-585 circuits with the addition of the functions x^2, $\sqrt{x}$, 1/x and +/-. The C/CF-589 circuits may be operated with either single or dual function keys with a keyboard configuration of from 20 to 29 keys.

PIN CONFIGURATION

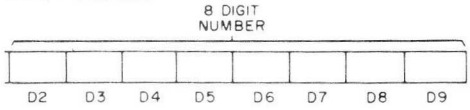
28 LEAD DUAL IN LINE



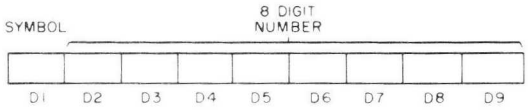
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DISPLAY

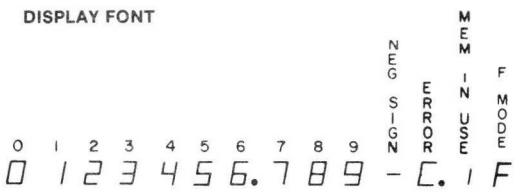
8 DIGIT DISPLAY



OPTIONAL 9 DIGIT DISPLAY

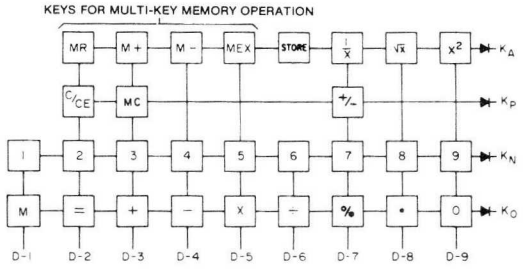


DISPLAY FONT

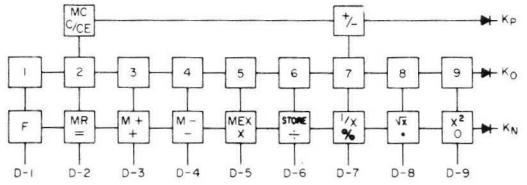


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-589.

CONSUMER

9 Digit / 5 Function Basic Calculator Circuits

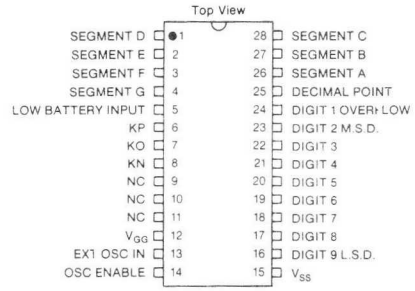
FEATURES

- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- C-593: direct LED segment drive.
  CF-593: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-593 circuits are basic five-function circuits for use with nine digit LED or fluorescent displays. These circuits enter and compute both positive and negative numbers to an eight digit resolution. On overflow, the overflow symbol is displayed in the ninth digit position, the decimal point is automatically shifted eight positions to the left of its computed position and the keyboard is locked.

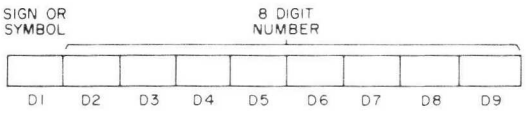
PIN CONFIGURATION
28 LEAD DUAL IN LINE



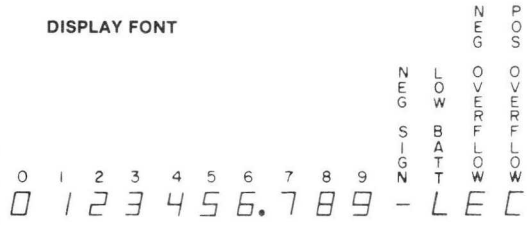
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DISPLAY

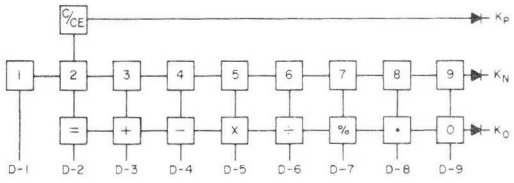
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-593.

9 Digit / 5 Function Basic Calculator Circuits With One-Key Memory

FEATURES

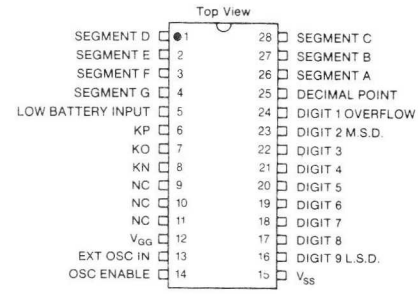
- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- One-key memory operation, with option for two additional memory function keys (refer to the description at the beginning of this section).
- C-594: direct LED segment drive.
  CF-594: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-594 circuits enable a manufacturer to add a memory calculator to his line with the simple inclusion of one additional memory key in the matrix of the C/CF-593 keyboard. All other operations are identical to the C/CF-593.

PIN CONFIGURATION

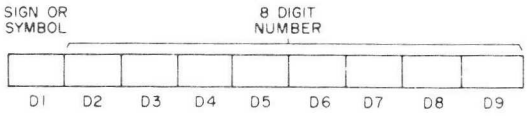
28 LEAD DUAL IN LINE



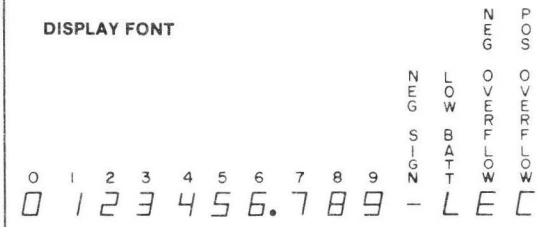
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DISPLAY

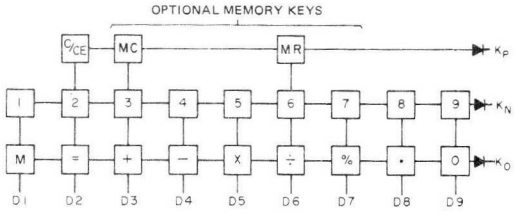
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-594.

CONSUMER

9 Digit / 5 Function Basic Calculator Circuits With Multi-Key Memory

FEATURES

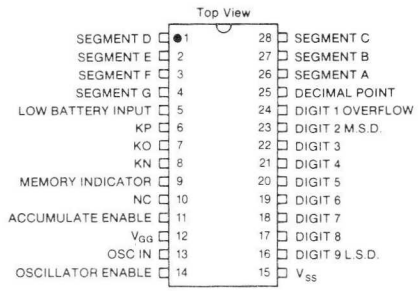
- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- Multi-key memory operation and automatic accumulating memory (refer to the description at the beginning of this section.)
- C-595: direct LED segment drive.
  CF-595: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-595 circuits add a variety of memory options to the basic C/CF-593 functions. While the basic pin configuration is identical to the C/CF-593, two additional connections are provided for a selectable "memory accumulate" switch and a "memory in use" indicator output.

PIN CONFIGURATION

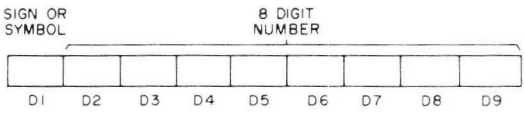
28 LEAD DUAL IN LINE



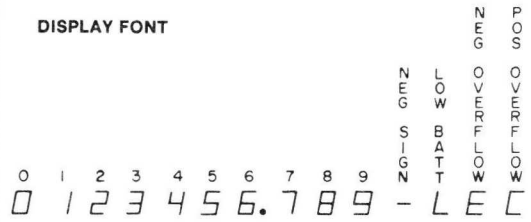
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DISPLAY

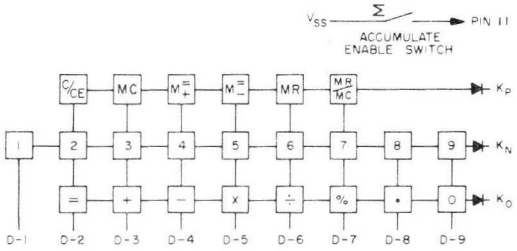
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-595.

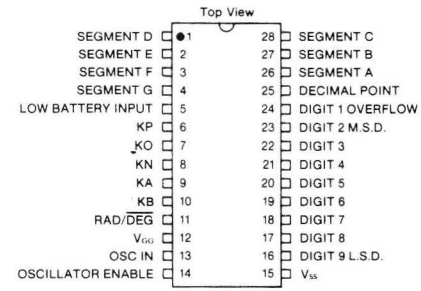
9 Digit / 15 Function Scientific Calculator Circuits

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
  8 digit display and sign for numbers not requiring scientific notation or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x and e^x).
- Convenience functions ($\sqrt{x}$, 1/x).
- A separate memory register (refer to the description at the beginning of this section).
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-596: direct LED segment drive.
  CF-596: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



NOTE:
The oscillator is enabled by connecting a 470K ±10% resistor from V_{GG} to pin 14.

DESCRIPTION

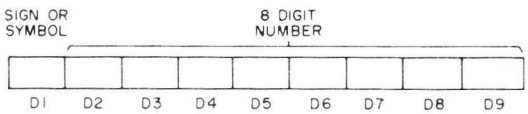
The C/CF-596 circuits are fifteen function circuits which offer trigonometric and inverse trigonometric functions, natural logs, e^x, $\sqrt{x}$, 1/x and π as well as the basic four functions and memory.

The circuit operates in the normal 8 digit mode until the display capacity is exceeded at which time it converts to the scientific mode of operation.

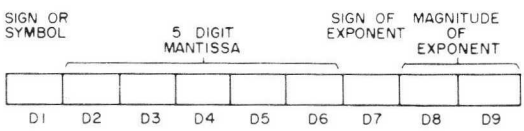
The C/CF-596 features single or dual function key operation for a keyboard configuration of from 19 to 35 keys.

DISPLAY

NORMAL MODE



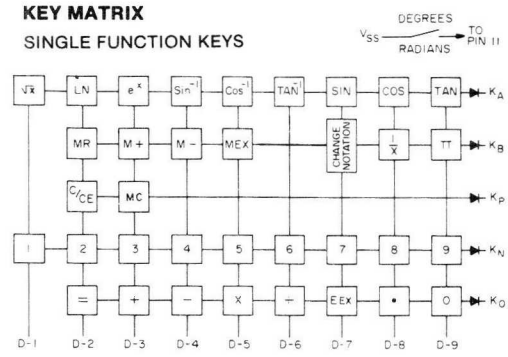
SCIENTIFIC NOTATION



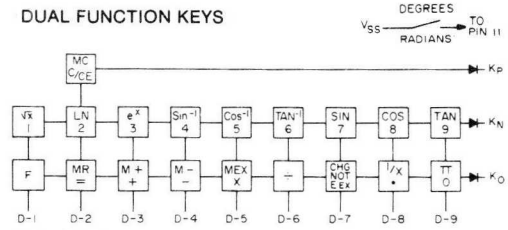
DISPLAY FONT

KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-596.

CONSUMER

9 Digit / 18 Function Scientific Calculator Circuits

FEATURES

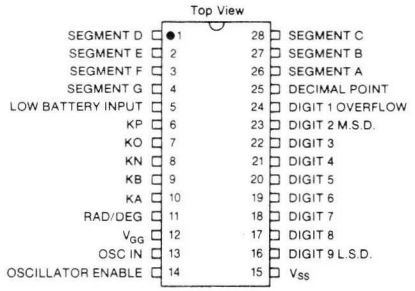
- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
- 8 digit display and sign for numbers not requiring scientific notation or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x, e^x, $\log_{10}$ and 10^x).
- Convenience functions ($\sqrt{x}$, 1/x, y^x).
- A separate memory register (refer to the description at the beginning of this section).
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-598: direct LED segment drive.
  CF-598: direct fluorescent display drive.
- All other features described on the first page of this section.

DESCRIPTION

The C/CF-598 circuits are eighteen function circuits whose operations are identical to the C/CF-596 with the addition of three functions: $\log_{10}$, 10^x and Y^x. Single or dual function key operation is optional with keyboard configurations of from 21 to 38 keys.

PIN CONFIGURATION

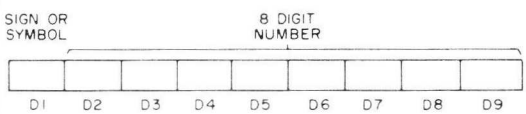
28 LEAD DUAL IN LINE



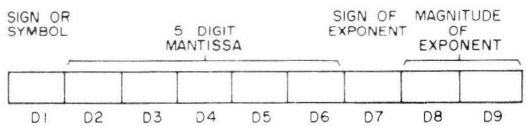
NOTE:
The oscillator is enabled by connecting a 470K ±10% resistor from V_{GG} to pin 14.

DISPLAY

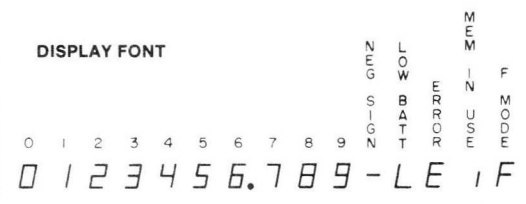
NORMAL MODE



SCIENTIFIC NOTATION

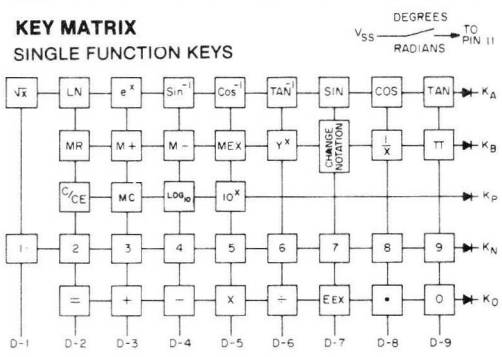


DISPLAY FONT

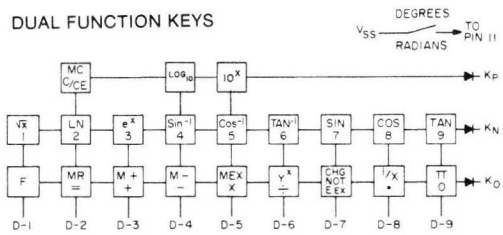


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-598.

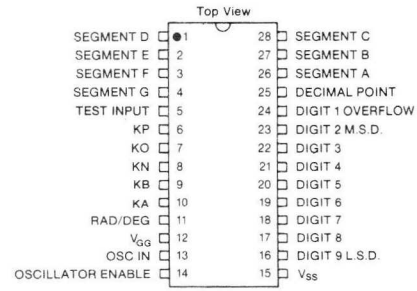
9 Digit / 21 Function Scientific Calculator Circuits

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
- 8 digit display and sign for numbers not requiring scientific notation, or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount)
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x, e^x, $\log_{10}$ and 10^x).
- Convenience functions ($\sqrt{x}$, $^1/x$, y^x, x^2, +/-).
- A separate memory function (refer to the description at the beginning of this section).
- Two levels of parentheses.
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-599: direct LED segment drive.
  CF-599: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



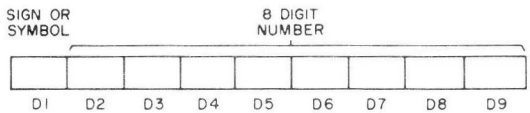
NOTE:
The oscillator is enabled by connecting a 150K ± 10% resistor from V_{GG} to pin 14.

DESCRIPTION

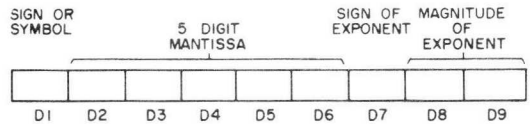
The C/CF-599 circuits are twenty-one function circuits whose operations are identical to the C/CF-598 with the addition of two levels of parentheses and three functions: x^2, % and +/-. Single or dual function key operation is optional with keyboard configurations of from 24 to 41 keys.

DISPLAY

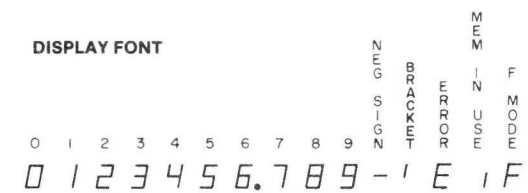
NORMAL MODE



SCIENTIFIC NOTATION

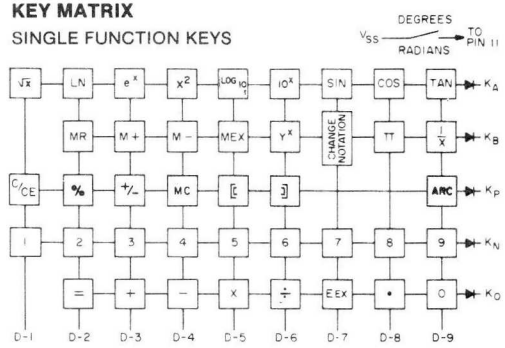


DISPLAY FONT

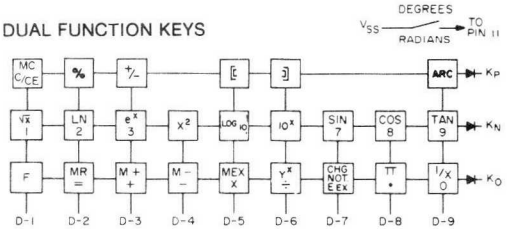


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-599.

CONSUMER

8 Digit Direct Drive Algebra Calculator Circuits

FEATURES

- Direct LED segment and digit drive (except CF-687/689/689HV)
- 8 digit, 7 segment display outputs.
- Floating negative sign.
- Right-justified entry and result.
- All other features listed on the first page of this section.

C-683D/1683D: 5 Function
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).

C-685D/1685D: 5 Function with Memory
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- One-key or multi-key memory function (refer to the description at the beginning of this section).

C-687D/1687D: 11 Function with Memory
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- One-key or multi-key memory function (refer to the description at the beginning of this section).
- Convenience functions (x^2, $\sqrt{x}$ 1/x, +/−, x-y exchange)
- π key to display the value of π.
- User option for single or dual function key operation.

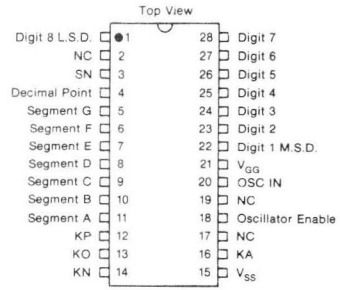
C-689D/1689D: 13 Function with Memory
- All features of the C-687D plus linear metric conversion (inch-cm, cm-inch) and one level of parenthesis.

CF-687: 11 Function with Memory
- Same as C-687D except direct fluorescent display drive.

CF-689/CF-689HV 13 Function with Memory
- Same as C-689D except direct fluorescent display drive. Supply voltage: 9V for CF-689, 15V for CF-689HV.

PIN CONFIGURATION

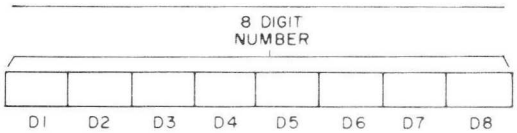
28 LEAD DUAL IN LINE
(Also available in a 28 Lead Mini-Pak)



NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 18.

DISPLAY

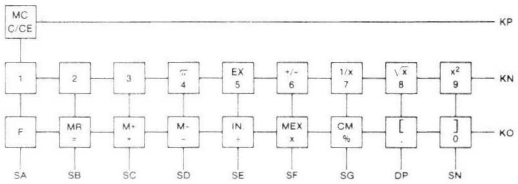
8 DIGIT DISPLAY



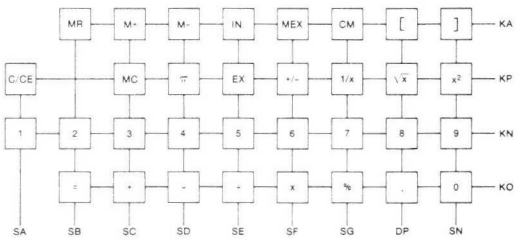
DISPLAY FONT

KEY MATRIX (C-689D/1689D shown)

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Printer Calculator Circuits

FEATURES

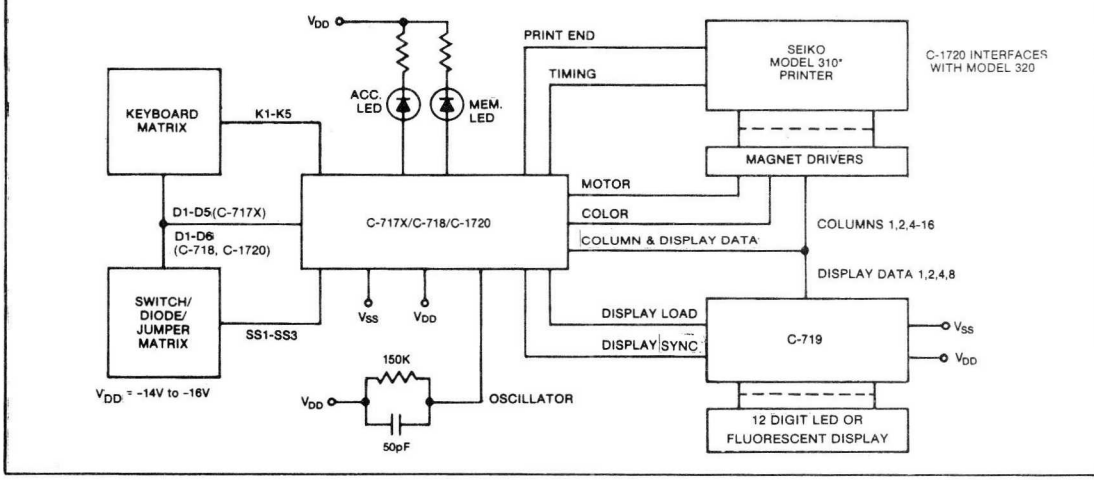
- 5 functions (+, −, x, ÷, %)
- Chain calculations.
- Repeat add/subtract.
- Automatic underflow and reverse underflow.
- Non-add (#)/date key.
- Memory non-zero indicators.
- Overflow indication.
- Automatic constant in multiply or divide.
- Right-justified entries and results.
- Leading zero suppression.
- 2 key rollover operation.
- Internal oscillator and power-on clear.

DESCRIPTION

The C-700 Series is a growing family of circuits for the printing calculator manufacturer which provide the capability for a broad-based, multi-feature business calculator product offering. The C-700 Series currently includes three different calculator circuits (the C-717X, C-718 and C-1720) and a printer-display interface circuit (C-719), each described on the following pages of this section.

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES
12 DIGIT PRINTING	Basic 4 functions and percent, automatic constant in multiply and divide, repeat add/subtract, decimal select mode, memory-in-use indicator, rounding options, non-add (#) date key, and other features. Interfaces with the Seiko Model 310 impact printer.	C-717X	40 DIP	Accumulator and Grand Total Memories.
		C-718		Accumulator, item counter, and four-key independent memory.
	All features described above, except interfaces with Seiko Model 320 impact printer.	C-1720	40 DIP	Accumulator, item counter, and four-key independent memory.
PRINTER-DISPLAY INTERFACE	Adds display capability to the C-717X, C-718 and C-1720 printing calculator circuits.	C-719	28 DIP	For both LED and fluorescent displays.

IMPACT PRINTER SYSTEM DIAGRAM



CONSUMER

12 Digit / 5 Function Impact Printer Calculator Circuit with Accumulator and Grand Total Memory

FEATURES

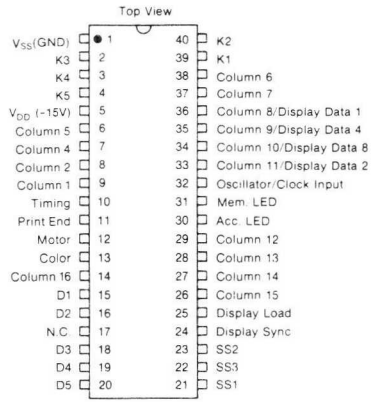
- 12 digit printout plus 2 full right-hand justified audit trail columns.
- Automatic accumulating memory (stores group totals).
- Grand total memory.
- Selectable memory modes: normal (last entry printed); (running subtotal printed); GT (grand total memory access).
- Fully arithmetic operation.
- Decimal select modes: full floating; fixed point (0-6); add mode (with hardwired secondary add mode option for quantity × dollars).
- Rounding options (truncate, 5/4 round off, 1/0 round up).
- Multistage keyboard buffer stores up to 8 keyed entries to allow uninterrupted operation during print.
- Printer and display capability (with the C-719 interface chip).
- All other features listed on the General Information page.

DESCRIPTION

The C-717X is a single MOS/LSI circuit containing all the logic functions required to implement a five-function, two memory general purpose business calculator using a Seiko Model 310 impact printer. The C-717X additionally provides signals for use with the C-719 printer-display interface chip. This allows the addition of a 12-digit fluorescent or LED display to the basic printer.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5
K1	0	5	00	.	=
K2	1	6	000	+	%
K3	2	7	=+	−	*
K4	3	8	=−	×	◊
K5	4	9	# DATE	÷	C/CE

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5
SS1	DECIMAL SELECT - SEE BELOW				
SS2			ADD MODE OPTION		PRINTER ON/OFF
SS3	◊ MODE	GT MODE	PAPER ADVANCE	TRUNCATE	ROUND OFF

DECIMAL SELECT CHART

The decimal select switch is a four-pole switch with encoded outputs during D1 thru D4 strobe periods. In the chart below, a '1' denotes a switch closure.

DECIMAL POSITION	D1	D2	D3	D4
+	1	1	0	1
F	1	0	0	1
0	1	0	0	0
1	0	1	0	0
2	1	1	0	0
3	0	0	1	0
4	1	0	1	0
5	0	1	1	0
6	1	1	1	0

12 Digit / 5 Function Impact Printer Calculator Circuit with Accumulator, Item Counter and Independent Memory

FEATURES

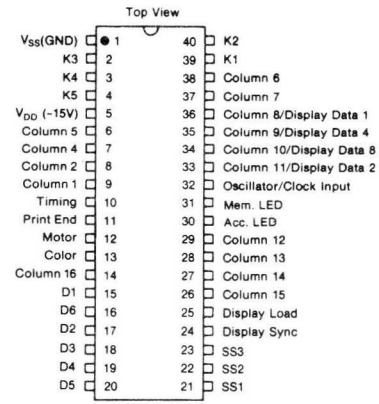
- 12 digit printout plus 2 full right-hand justified audit trail columns.
- Switch-selectable automatic accumulation.
- Three digit item counter.
- Four-key independent memory.
- Arithmetic operation in add/subtract sequences, algebraic in multiply/divide (business logic).
- Decimal select modes: full floating; fixed point (0-6, excluding 5); add mode (automatic decimal 2 in + and −, unit/price mode in ×).
- Non-coded decimal select switch input.
- Rounding options (truncate, 5/4 round off, 1/0 round up).
- Separate clear-all key.
- Full floating accuracy on intermediate results in chain operation.
- Multistage keyboard buffer stores up to 6 keyed entries to allow uninterrupted operation during print.
- Display capability (with the C-719 interface chip).
- All other features listed on the General Information page.

DESCRIPTION

The C-718 is a single MOS/LSI circuit containing all the logic functions required to implement a five-function general purpose consumer calculator with an accumulator, item counter and four-key independent memory. The C-718 has been designed to operate with a Seiko Model 320 16 column impact printer. When used with the C-719 printer-display interface, the C-1720 also provides a 12-digit display capability, using either fluorescent or LED displays.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



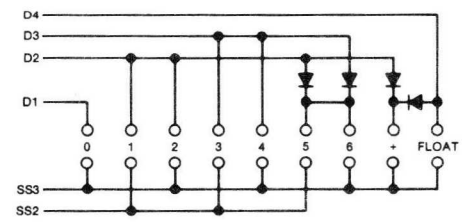
KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
K1	0	5	00	N	=	C/CE
K2	1	6	.	+	%	M+
K3	2	7	=+	−	*	M−
K4	3	8	=−	×	◊	M*
K5	4	9	# DATE	÷	CA	M◊

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
SS1	Σ		PAPER ADVANCE	TRUNCATE	5/4 1/0	PRINTER ON/OFF
SS2	DECIMAL SELECT - SEE BELOW					EXT. P.O.C.
SS3						

DECIMAL SELECTION



CONSUMER

C-1720

12 Digit / 5 Function Impact Printer Calculator Circuit with Accumulator, Item Counter and Independent Memory

FEATURES

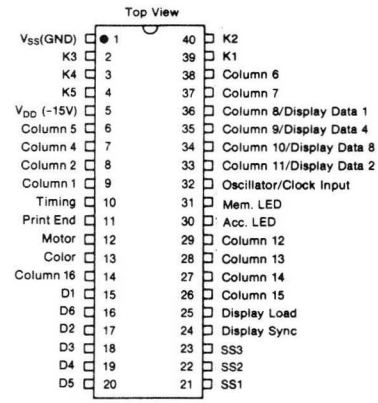
- 12 digit printout plus 2 full right-hand justified audit trail columns.
- Switch-selectable automatic accumulation.
- Three digit item counter.
- Four-key independent memory.
- Arithmetic operation in add/subtract sequences, algebraic in multiply/divide (business logic).
- Decimal select modes: full floating; fixed point (0-6, excluding 5); add mode (automatic decimal 2 in + and –, unit/price mode in ×).
- Non-coded decimal select switch input.
- Rounding options (truncate, 5/4 round off, 1/0 round up).
- Separate clear-all key.
- Full floating accuracy on intermediate results in chain operation.
- Multistage keyboard buffer stores up to 6 keyed entries to allow uninterrupted operation during print.
- Display capability (with the C-719 interface chip).
- All other features listed on the General Information page.

DESCRIPTION

The C-1720 is a single MOS/LSI circuit containing all the logic functions required to implement a five-function general purpose consumer calculator with an accumulator, item counter and four-key independent memory. The C-1720 has been designed to operate with a Seiko Model 320 16 column impact printer. When used with the C-719 printer-display interface, the C-1720 also provides a 12-digit display capability, using either fluorescent or LED displays.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



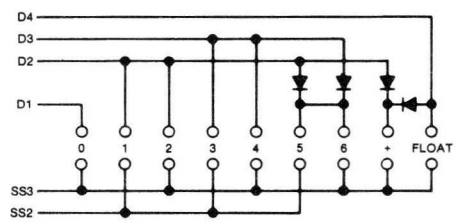
KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
K1	0	5	00	N	=	C/CE
K2	1	6	.	+	%	M+
K3	2	7	=+	−	*	M−
K4	3	8	=−	×	◊	M*
K5	4	9	# DATE	÷	CA	M◊

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
SS1	Σ		PAPER ADVANCE	TRUNCATE	5/4 1/0	PRINTER ON/OFF
SS2						EXT. P.O.C.
SS3	DECIMAL SELECT - SEE BELOW					

DECIMAL SELECTION



Printer-Display Interface Circuit

FEATURES

- Adds display capability to C-717X and C-718 printer chips.
- Full 12 digit display capability.
- Drives LED or fluorescent displays.

DESCRIPTION

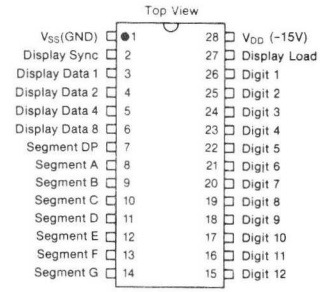
The C-719 is a single MOS/LSI circuit designed to add a 12 digit display capability to General Instrument's C-717X and C-718 printer calculator circuits. Data from the printer calculator chips is transferred to the C-719 interface chip serially and re-formulated to drive seven segment multiplexed common cathode displays.

The segment and digit outputs of the C-719 are open-drain and have a breakdown voltage of −30 Volts to enable the driving of fluorescent displays with a minimum of interface components. LED displays may also be driven by the C-719 with direct drive of the segments and the addition of digit-drive buffers.

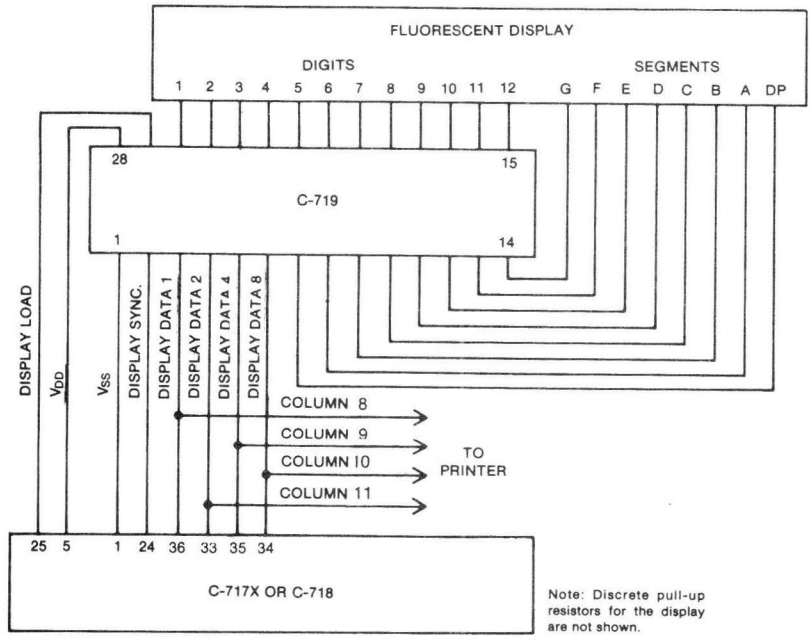
In the display, leading zeroes are suppressed and entries and results are right-justified.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



Note: Discrete pull-up resistors for the display are not shown.

CONSUMER

MICRO ELECTRONICS

CLOCKS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
4 DIGIT	12/24 hour clocks with features for most clock/timing applications.	AY-5-1200A	8-24
		AY-5-1202A	8-24
		AY-5-1203A	8-24
		AY-5-1204A	8-24
		AY-5-1224A	8-27
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	8-29
4 DIGIT AUTO CLOCK	12 hour clock, timing derived from 3.58MHz TV crystal.	CK3500	8-41
		CK3500F	8-41

AY-5-1200A AY-5-1203A
AY-5-1202A AY-5-1204A

4 Digit Clock Circuits

FEATURES

- Hours and minutes display.
- 12/24 hour operation.
- 50/60Hz operation.
- High voltage direct Fluorescent drive Outputs.
- Flashing seconds output (option).
- BCD output (option).
- Leading Zero Blanking (option).
- Power-On Reset to zero.
  (Counting does not start until time is set.)
- Options:

	7 Seg	BCD	Zero Blank	Flashing Sec
AY-5-1200A	Yes	No	Yes	No
AY-5-1202A	Yes	No	Yes	Yes
AY-5-1203A	No	Yes	No	Yes
AY-5-1204A	Yes	No	No	Yes

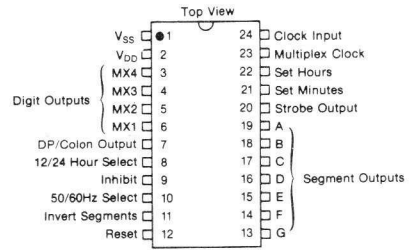
DESCRIPTION

The AY-5-1200A Series are P-Channel MOS integrated circuits, containing all the logic necessary to make a 4 digit, 12 or 24 hour clock, operating from 50 or 60Hz. High voltage output stages capable of driving fluorescent displays are provided.

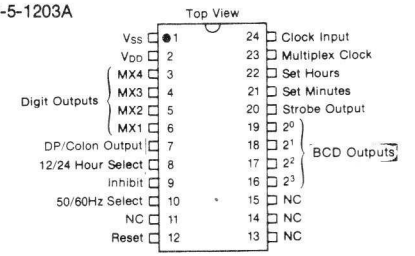
PIN CONFIGURATION

24 LEAD DUAL IN LINE

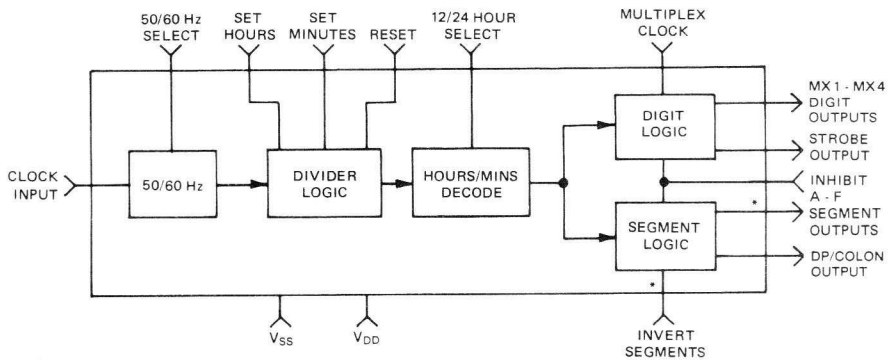
AY-5-1200A/AY-5-1202A/AY-5-1204A



AY-5-1203A



BLOCK DIAGRAM



* Not included in the AY-5-1203A. Four BCD outputs are provided in place of the seven segment outputs.

PIN FUNCTIONS

Name	Function
Segment Outputs A—F	In 7 segment mode the digits are multiplexed on to these pins. These outputs are at logic '0' to display (positive) and will drive Fluorescent displays directly. In BCD mode outputs A to D are used, the code for 0 being 0000.
DP/Colon Output	This is a high voltage output intended to drive a decimal point or colon. It is enabled during the MX3 time slot and can flash once per second if required.
Multiplex Outputs MX1—MX4	These outputs select the display digits sequentially, they will drive Fluorescent displays directly. Five multiplex time slots are generated the fifth one being blank. Minutes are output in MX1 time, 10's of hours in MX4 time.
Reset Input	When taken to logic '0' the clock is reset to zero.
Set Minutes Input	When taken to logic '0' the minutes counter is advanced at the rate of 2 min. per sec. and the hours counter at the rate of 2 hours per minute.
Set Hours Input	When taken to logic '0' the hours counter is advanced at the rate of 2 hours per second.
50/60Hz Select Input	When taken to logic '0', 60Hz operation will result.
12/24 Hours Select Input	When taken to logic '0', 12 hour operation will result.
Invert Segments Input	When taken to logic '0' the segment outputs will be inverted.
Multiplex Oscillator	An external capacitor is used to select the multiplex frequency. If required the pin can be driven by an external oscillator.
50/60Hz Input	The master clock is input to the pin. Hysteresis is provided so that the input waveform is not critical.
V_{SS}	Positive Supply.
V_{DD}	Negative Supply.
Inhibit Input	When taken to logic '0' all outputs are switched OFF.
Strobe Output	This is a short pulse occurring during the middle of each multiplex period.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Multiplex outputs) . . . . . +0.3 to -35V
Operating Temperature Range. . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation at +70°C Ambient—Total 500mW
Per Output. 50mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = - 0V
V_{DD} = -17V ± 10% (AY-5-1200A/1202A/1204A)
V_{DD} = -11.4V to -19V (AY-5-1203A)
Operating Temperature (T_A) = 0°C to +70°C

NOTE:
In the chart below, numbers in ( ) refer only to the AY-5-1203A.

Characteristic	Min.	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	
Clock input logic '0'	+0.5	—	-2(-1)	Volts	Note 1
Clock input logic '1'	-8	—	V_{DD}	Volts	
Multiplex clock frequency	DC	—	50	kHz	Note 2
Control inputs logic '0'	+0.3	—	-1.5(-1)	Volts	
Control inputs, current logic '0'	—	100	—	μA	Note 3
Control inputs logic '1'	-6	—	$-V_{DD}$	Volts	
Segment Outputs					
ON current	2(1.3)	—	—	mA	V_{OUT} = -2V
OFF leakage	—	—	5(10)	μA	V_{OUT} = -25V(-19V)
	—	—	10	μA	V_{OUT} = -35V
Multiplex Outputs					
ON current	5(3.3)	—	—	mA	V_{OUT} = -2V
OFF leakage	—	—	5(10)	μA	V_{OUT} = -25V(-19V)
	—	—	10	μA	V_{OUT} = -35V
Supply Current	—	8.5(6.5)	14	mA	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken positive with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. These inputs have a 170Kohm pull up resistor to V_{DD}.

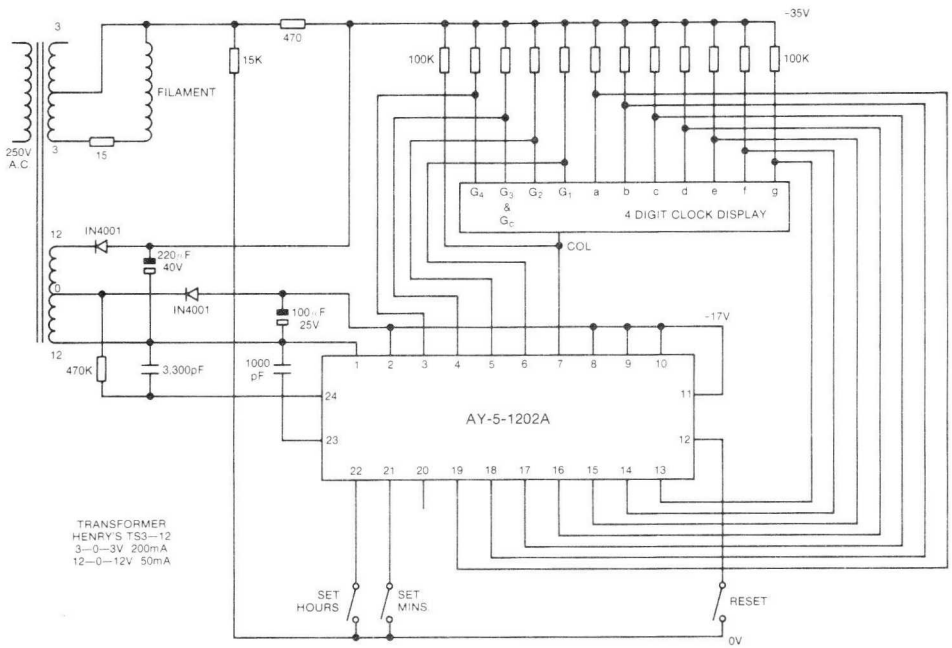


Fig.1. DIGITAL CLOCK CIRCUIT USING AY-5-1202A WITH FUTABA FLUORESCENT DISPLAY 5-LT-01

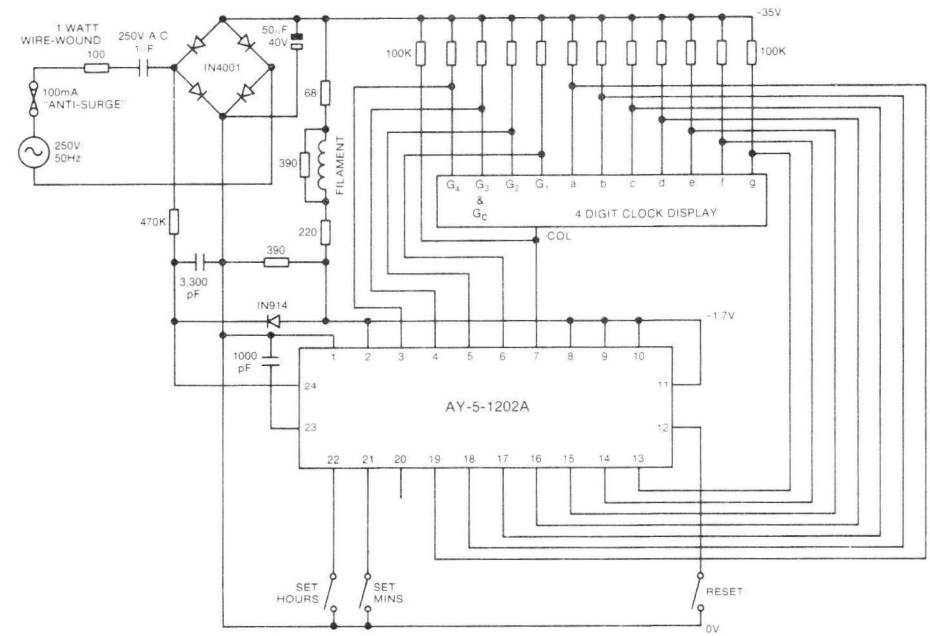


Fig. 2. DIGITAL CLOCK CIRCUIT USING AY-5-1202A WITH FUTABA FLUORESCENT DISPLAY 5-LT-01 AND CAPACITIVE POWER SUPPLY

4 Digit Clock Circuit

FEATURES

- 12/24 hour operation.
- Leading zero blanking in 12 hour mode.
- 50 or 60 Hz clock input.
- Hours and minutes display (4 digits).
- 7 segment outputs direct LED drive or TTL compatible BCD outputs.
- Complement control for segment outputs.
- Interdigit blanking for gas discharge displays.
- On chip multiplex oscillator.
- Single 15V supply.
- Power-On Reset to zero. (Counting does not start until time is set.)

DESCRIPTION

The AY-5-1224A is a P channel MOS integrated circuit containing all the logic necessary to make a 4 digit, 12 or 24 hour clock operating from a 50 or 60Hz input. It has multiplexed BCD or 7-segment outputs and will drive LED, Fluorescent and Gas discharge displays with the minimum of interfacing.

PIN FUNCTIONS

Pins 1 and 11 are multifunction. During multiplex times 1 to 4 they function as data outputs, either 7 segment code or BCD according to the display mode selected. During multiplex time 5 (Strobe) they function as inputs.

Segment Outputs A-G (Pins 1 and 11 to 16)
In 7 segment mode the digits are multiplexed out on to these pins. Normally the outputs are at logic '0' (positive to display). Interdigit blanking for ¼ the digit time is incorporated for gas discharge displays.

BCD Outputs 2^0—2^3 (Pins 1, 16, 15, 14)
In BCD mode the digits are multiplexed on to these pins in BCD code. Normally the outputs are at logic '0' (positive), i.e. code 0=0000.

Multiplex Outputs 1-4 (Pins 10, 9, 8, 7)
These pins are successively switched to logic '0' to select appropriate digit display. A fifth multiplex time (Strobe) is used to enable the control inputs. These outputs have interdigit blanking. The multiplex rate is 1/20th the multiplex clock frequency.

Strobe Output (Pin 6)
This pin is used to enable the control input keyboard, it goes to logic '0' to enable.

Set Hours Input (Pin 1)
When taken to logic '0' during strobe time this input causes the hours counter to advance at the rate of 1 hour per second.

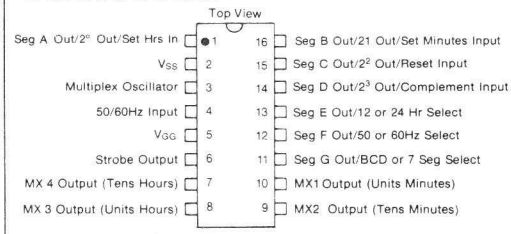
Set Min Input (Pin 16)
When taken to logic '0' during strobe time this input causes the minutes counter to advance at the rate of 1 per second and the hours counter to advance at the rate of 1 hour per minute.

Reset Input (Pin 15)
When taken to logic '0' during strobe time this input causes the clock to reset to zero.

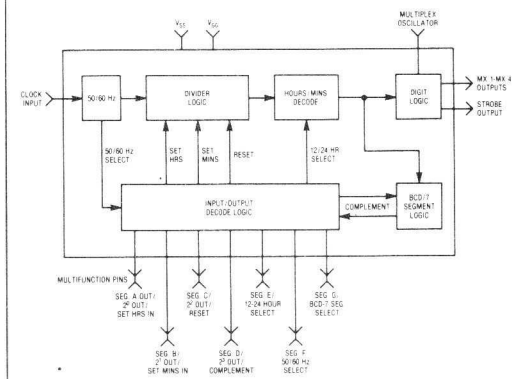
Complement Input (Pin 14)
When left open the segments and BCD outputs will have normal polarity. When connected to Strobe output via a diode the 7 segment and BCD outputs will be inverted.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



12/24 Hour Select (Pin 13)
When left open the clock will run in the 12 hour mode, when connected to strobe via a diode 24 hour operation will result.

50/60Hz Select (Pin 12)
When left open a 50Hz clock will be accepted. When connected to strobe via a diode 60Hz operation will result.

BCD/7 Segment Select (Pin 11)
When left open 7 segment outputs will be provided, when connected to strobe via a diode BCD outputs will be provided.

50/60Hz Input (Pin 4)
The master clock (50 or 60Hz) is input to this pin. Hysteresis is provided on the input so that the input wave form is not critical.

Multiplex Oscillator (Pin 3)
An external capacitor is used to set the multiplex frequency. If required this input can be driven by an external oscillator.

V_{SS} (Pin 2)
Positive supply line nominally OV.

V_{GG} (Pin 5)
Negative supply line nominally -15V.

Power-On Reset
At power-on the chip is reset to zero. Counters will not start until Set Hours or Set Minutes has been activated.

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . +0.3 to −20V
Operating Temperature Range . . . . . 0° to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation at 70°C Ambient—Total 500mW
Per Output. 50mW

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

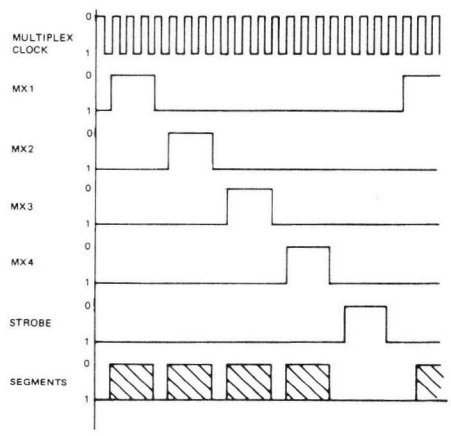
V_{SS} = 0V
V_{GG} = −12 to −18V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	—
Clock input logic '0'	+0.5	—	−2	Volts	Note 1
Clock input logic '1'	−8	—	V_{DD}	Volts	—
Multiplex Clock Frequency	DC	—	50	kHz	Note 2
Interdigit Blanking	—	150	—	μs	at 6.67kHz Note 3
Control inputs logic '0'	+0.3	—	−1.5	Volts	—
Control inputs logic '1'	−6	—	V_{DD}	Volts	—
Outputs Logic '0'	—	—	500	Ω	V_{OUT} = -2V, I_{OUT} = 4mA
Outputs Logic '1' (Leakage)	—	—	10	μA	V_{OUT} = −18V
Supply Current	—	—	10	mA	V_{GG} = -15V

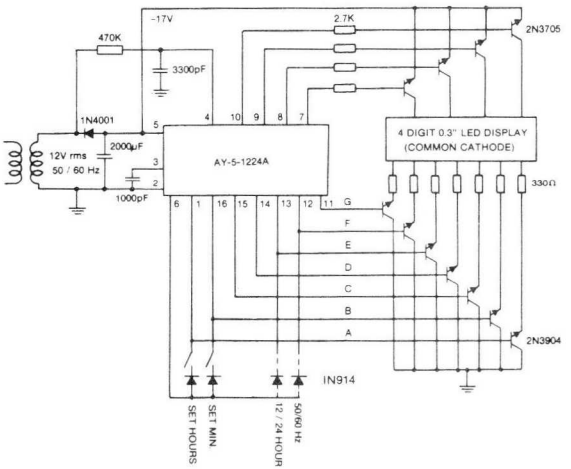
**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken position with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. At 6.67KHz multiplex frequency the digit ON time is 450μS and the OFF time is 150μS.

TIMING DIAGRAMS



AY-5-1224A WITH 0.3" LED DISPLAY



4 Digit Clock Radio Circuit

FEATURES

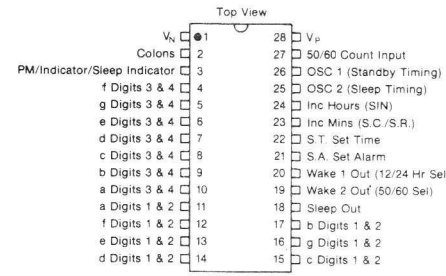
- 4 Digits plus colons
- LED direct duplex drive
- No display-IC interface components
- No radio frequency interference problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- On-chip oscillator for standby operation with battery during line Failure
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation (under 30 mW)

CLOCK RADIO FEATURES

- Simple support electronics
- Analog sleep setting (user controlled 5 to 120 mins with 1 minute resolution). No necessity for daily adjustment
- Totally independent sleep and wake timing
- Independent volume of music during sleep and wake
- Radio sound muting during normal radio listening
- Wake to music or alarm tone
- Self-cancelling alarm after 80 minutes of wake
- 5 minute repeating snooze with radio and/or alarm
- Sleep override or sleep repeat
- Wake to alarm tone with quiet radio override (every 5 minutes) during snooze time (repeatable)
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propagation suppressed)
- 5 minute pre-alarm appliance switching
- Automatic tape recorder control (record your favorite program automatically 0-120 minutes—starting from the exact second)

PIN CONFIGURATION

28 LEAD DUAL IN LINE



DESCRIPTION

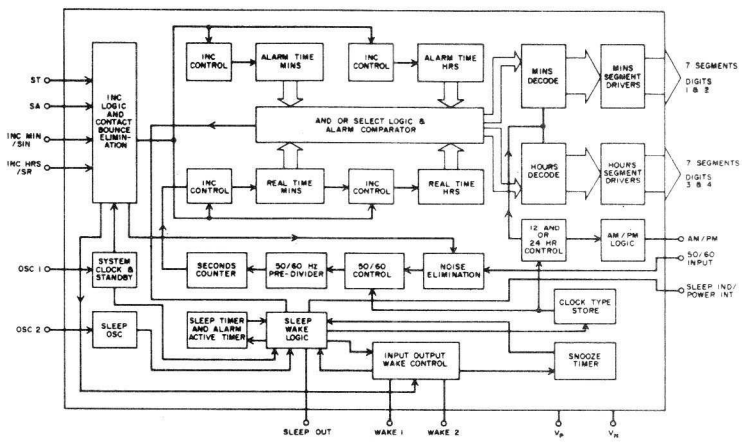
The CK3300 N-Channel MOS I.C. contains all the necessary logic, contact noise elimination circuits, control switching, segment drivers and timing circuits to implement simple-to-use, low cost, multi-featured clock radios.

Due to the extreme difficulties in eliminating R.F.I. in radios when used in conjunction with digital electronics a great deal of care has gone into the design of the L.S.I. to ensure that little or no R.F.I. problems are met by the clock radio designer. The largest R.F.I. problem in Display Driving has been solved using a novel technique—that of half-line cycle anode duplexing using the half-sine waves produced by two diodes, and ensuring that all segment data changes occur at the zero crossings of the line cycle. This technique allows brightness control to be achieved simply by resistively dividing down the line voltage with a potentiometer, or a simple two level scheme using a transformer tap.

Segment driving of the two groups is directly from the I.C. through 50 ohm switches which allow the high current peaks required of LEDs, up to one inch in size, while keeping the I.C. Power dissipation, for reliability, down to the 200 to 250 mW level.

The I.C. also contains many unique features which enable the equipment designer to put into the clock radio his company's own product image.

BLOCK DIAGRAM



CONSUMER

PIN FUNCTIONS

V_N - (Pin 1)
Is the most negative power supply to the chip (0 volts).

Segment Drivers (Pins 2-17)
These outputs are 50 Ω switches which drive the segments of common anode LED's directly. Their use and operation is as follows:

To use the CK3300 with LEDs, the LEDs must be of the COMMON ANODE TYPE, and connected in the following manner.

segment a digit 1 connected to segment a digit 2
segment b digit 1 connected to segment b digit 2
segment c digit 1 connected to segment c digit 2
segment d digit 1 connected to segment d digit 2
segment e digit 1 connected to segment e digit 2
segment f digit 1 connected to segment f digit 2
segment g digit 1 connected to segment g digit 2

segment a digit 3 connected to segment a digit 4
segment b digit 3 connected to segment b digit 4
segment c digit 3 connected to segment c digit 4
segment d digit 3 connected to segment d digit 4
segment e digit 3 connected to segment e digit 4
segment f digit 3 connected to segment f digit 4
segment g digit 3 connected to segment g digit 4

Colon 1 segment connected to colon 2 segment
PM indicator segment connected to sleep/power down indicator segment
Anode digit 1 to anode digit 3
Anode PM indicator to anode digit 4
Anode sleep indicator to anode digit 1
Anode colon upper to anode digit 3
Anode digit 2 to anode digit 4
Anode colon lower to anode digit 2

The anodes can then be selected by the application of alternate half-cycle sine waves derived from a transformer from the line. The phase of the incoming 50/60Hz count to IC will then automatically deliver the correct segment data to the display.

Anode phasing: 50/60 high = digit (1 & 3) selected
low = digit (2 & 4) selected

Sleep Output (Pin 18)
This output turns on while the sleep counter is running and is indicated as active by an indicator in the display (Pin 3). This output turns on immediately following a sleep initiate and is cancelled either by sleep time being complete, a sleep cancel, an alarm comparison taking place, or an end of snooze period. This pin is also used as an input during circuit test to speed up testing.

Wake 2 Output/50-60 Hz Mode Select (Pin 19)
This output turns on at alarm compare time and stays on unless either an alarm cancel or a snooze repeat is activated.

If snooze repeat is activated this pin will go off until the next 5 minute period elapses when it will again turn on.

The snooze can be repeated indefinitely.

If the alarm is not cancelled this output will turn off 80 mins after the last snooze repeat re-triggering alarm for the next 24 hour period.

This pin is also the 50/60 Hz Select input during the time at which Set Time and Set Alarm are at a logic '1' (last data on this input when either Set Time or Set Alarm changes state is stored in an internal latch).

Wake 1 Output/12 Or 24 Hour Select (Pin 20)
This output turns on at alarm compare time and stays on uninterrupted until either:

a. An alarm cancel
b. 80 continuous minutes from alarm time
c. 80 continuous minutes from last snooze repeat

During the time that Set Time and Set Alarm are at a logic '1' together, this pin is the 12/24 hour select input.

The last data on this pin before a data change on Set Time or Set Alarm is stored internally in a latch, and defines 12 or 24 hour operation.

Set Alarm (Pin 21)
This pin, held at zero while Set Time is at a logic '1', enables the Increment Minutes and Increment Hours inputs to the alarm counter, such that each change of state (1→0) of the increment inputs will advance the appropriate counter by one unit.

Set Time (Pin 22)
Is identical in operation to the Set Alarm pin, but in this instance allows the counts to be entered into the time counter.

Taking both Set Time and Set Alarm to a logic '0' allows the Wake outputs to become active when the time reaches the alarm time. Returning either Set Time or Set Alarm to a logic '1' will cancel the alarm.

Increment Mins/Sleep Cancel/Snooze Repeat (Pin 23)
If Set Time or Set Alarm is at zero, this input provides one unit of increment for each logic transition from one to zero. (This input is de-bounced against switch noise). If both Set Time and Set Alarm are at a logic '1' or logic '0' and the sleep timer is running, a logic zero on this input will cancel sleep.

If both Set Time and Set Alarm are at a zero and the Wake outputs are active (i.e., post alarm time), then Wake 2 will be cancelled for a period of up to 5 mins when Pin 23 is taken to logic '0'. If this input is at zero when the alarm comparison takes place, then Wake 2 will stay off until 5 minutes have passed.

Increment Hours/Sleep Initiate (Pin 24)
If either Set Time or Set Alarm is at logic '0', this input provides one unit of increment to the required counter for each logic transition from 1 to 0. (This input is de-bounced against switch noise). If both Set Alarm and Set Time are at logic '1' or logic '0', this input will cause Sleep output to become active for the time resulting from current sleep oscillator frequency.

OSC 2 (Pin 25)
This pin produces a triangular wave oscillation depending on the value of resistance and capacitance. This oscillator is used to produce the sleep period by being gated internally with 160th of Osc 1 frequency (i.e. 50/60Hz).

Additionally connected to this pin is a low level detect circuit used with oscillator 1 for re-setting all internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used to detect that standby operation is required.

OSC 1 (Pin 26)
This pin produces a triangular wave oscillation depending on the external value of resistance and capacitance. The signal is used during normal operation to provide internally to the I.C. -
a. the internal timing for a series of one-shot gates
b. After division, the frequency to de-bounce other external pins via D-type latches. This frequency is further divided down to 50/60Hz and is used as the source frequency during standby operation.
Connected internally to this pin is a low level voltage detector which is used in conjunction with a low level voltage detector on Osc. 2 (pin 25) to reset all the internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used for test purposes.

50/60 Hz In (Pin 27)
This input is the normal source of timing. This input drives both the internal count and the alternate half line selection of the segment outputs.
For equal brightness in the display this input must have a 1:1 mark space ratio (±20%).
There is no necessity for eliminating line noise externally when providing this input signal as an internal arrangement eliminates undesired counts.

V_P (Pin 28)
Is the most positive power supply to the chip (typically 10 volts)

FUNCTIONAL OPERATION

Pins 19, 20, 23 and 24 are dual function pins which operate as inputs or outputs dependent on the state of the Set Time and Set Alarm inputs:

S.T.	S.A.	INC MIN	INC HR	SC/ SR	SIN	Wake 1	Wake 2	50/ 60	12/ 24
1	1	-	-	*	*	-	-	*	*
1	0	*	*	-	-	-	-	-	-
0	1	*	*	-	-	-	-	-	-
0	0	-	-	*	*	*	*	-	-

*Operable - Not Operable

Set time (S.T.)	Pin 22
Set alarm (S.A.)	Pin 21
Increment minutes (inc min)	Pin 23
Increment hours (inc hrs)	Pin 24
Sleep cancel (S.C.)	Pin 23
Snooze repeat (S.R.)	Pin 23
Sleep initiate (SIN)	Pin 24
Wake 1	Pin 20
Wake 2	Pin 19
50/60Hz Select	Pin 19
12/24Hr. Select	Pin 20

Using Wake 1 Or 2—Input/Output Functions

When the Set Time (S.T.) and Set Alarm (S.A.) inputs are at logic one, the IC outputs Wake 1 and Wake 2 become inputs to two bistable gates which store the logic conditions on those pins: 50/60Hz Select on the Wake 2 pin and 12/24Hr. Select on the Wake 1 pin.

50/60Hz Select

Set Time or Set Alarm must be at zero before data on Wake 2 changes, or clock can change its 50/60 pre-divide mode. To avoid this, the following circuit is recommended:

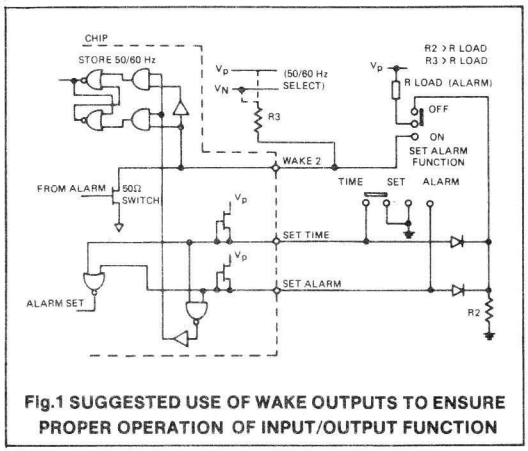


Fig.1 SUGGESTED USE OF WAKE OUTPUTS TO ENSURE PROPER OPERATION OF INPUT/OUTPUT FUNCTION

With the Set switch in the center position the set inputs are pulled up to a logic '1' by the IC, provided the Alarm switch is in the off position. The load (R load) will pull the junction of the two diodes and R2 to a logic '1'.

The output pin Wake 2 will either be pulled up or down depending on the connection of R3.

Changing of Set switch will pull down the appropriate input and not affect other external circuit conditions.

Change of position of alarm ON-OFF switch will allow R2 to pull down both Set inputs to zero before Wake 2 output is connected to load. This ensures that the internal IC latch is disconnected from wake line before data on wake line can influence stored data in latch.

12/24 Hr. Select

For the "Wake 1 output 12-24 hour select", changing the logic polarity will immediately change the displayed time from 12 hour mode to 24 hour mode or vice versa.

e.g. 21 : 56 becomes •9 : 56
or •9 : 56 becomes 21 : 56

No leading zero is shown in 24 hour mode:

12 : 32 in 12 hour time becomes 0 : 32 in 24 hour time

(Note: 12 to 24 hour displayed time change can only be achieved when the alarm is not requested and not in set mode)

For economy of LEDs a single dot is employed which is illuminated during the PM period in 12 hour time.

Time Setting

Four input pins (S.T., S.A., Inc Hr., Inc Mins.) are provided to enable the following four functions to be provided:

a. Setting the time
b. Setting the alarm
c. Stopping the clock
d. Starting the clock

For synchronizing purposes

S.T. = 0

Allows each depression of Inc Hrs to advance hrs by one count. Clock will stop on the first inc mins and will remain stopped until ST = 1, thus allowing synchronization. The device assumes that the hours may need to be changed without affecting mins, but assumes clock is incorrect if minutes are changed, thus stopping clock and re-setting internal seconds counter to zero.

S.A. = 0

Selects alarm time and, for each depression of Inc Hours, hours are advanced one and, for each depression of Inc Mins, minutes are advanced one.

NOTE:
No carries from minutes to hours occur during setting of time or alarm

Radio Control Inputs

The inputs S.T., S.A., Inc Min, Inc Hr, serve as radio control inputs under the following conditions.

S.T. And S.A.

At zero together - alarm is requested. S.T. and S.A. at logic one together - alarm not requested, but if taken to logic one during post alarm, alarm is cancelled.

S.T. and S.A. different will also cancel alarm if alarm is active.

S.T.	S.A.	Pre-Alarm	Post-alarm
1	1	Not required	Cancel
1	0	Not required	Cancel
0	1	Not required	Cancel
0	0	Requested	Alarm maintained for 80 mins

S.T., S.A. = 1

If S.T. and S.A. are at a logic 1 together during pre-alarm time, the following functions can be obtained using Inc Min - Inc Hrs inputs. Inc Hrs input going to logic zero for at least 20m secs will result in sleep output going to zero for the period of time set by sleep potentiometer.

At any time Inc Mins input (SC/SR) going to zero for at least 20m secs will cancel sleep timer if sleep output is active.

To reduce the number of knobs, switches, wiring etc., in the clock radio the following alternative feature is provided. If (S.C./S.R.) is wired to (SIN) a dual action is achieved, 1st depression of switch activates sleep, 2nd cancel sleep, 3rd re-activates etc. This allows features (a) if user decides he wishes radio off after he has been in bed for a few minutes, he pushes button, or (b) radio goes off automatically because sleep period has finished, but user is not asleep and would like radio to continue, so he presses button again.

S.T., S.A. = 0

In pre-alarm period the function performed when S.T., S.A. = 1 is identical. (When the alarm sounds at the requested alarm time the input (S.C./S.R.) (Inc Mins) becomes the 5 min snooze repeat input.)

At alarm, the effect of (S.C./S.R.) becoming zero for at least 20m secs is to turn Wake 2 output off until next 5 min interval, if again depressed, Wake 2 will turn off for a further 5 mins—this sequence will go indefinitely until S.T., or S.A. or both are returned to logic '1', cancelling alarm. If inputs to the device are left unchanged for 80 mins then alarm will re-set for 24 hours.

Again to improve the radio features and simplify radio operation the tied function of (S.C./S.R.) and (SIN) on one button performs the following three functions:

Initiate sleep (SIN)
Cancel sleep (S.C.)
Snooze repeat (S.R.)

Delaying Alarm by 5 Minutes

If, when Wake 1 ouput is capacitively coupled to (S.C./S.R.) input then at alarm time Wake 1 will turn on and stay on but Wake 2 will immediately become cancelled, hence no alarm will be heard from radio until 5 minutes later; this allows an electrical appliance to be turned on 5 minutes prior to alarm sounding.

Use of Sleep Timer for Tape Recorder Control

If sleep input (SIN) in directly coupled to Wake 1 output, then a tape recorder or any electrical equipment can be turned on at alarm time using sleep output for a period of time set on sleep potentiometer.

Radio Control Outputs

There are three radio control outputs:

a. Wake 1
b. Wake 2
c. Sleep output

Function

1. Wake 1—goes at zero; i.e. is on at alarm time for a period of 80 mins or until an alarm cancel.

2. Wake 2 goes to zero at alarm time, and stays at zero until a snooze repeat is activated then it will stay off until next 5 minute point then return to zero, for a period of 80 mins unless snooze repeat is re-activated. Snooze repeat can be used indefinitely, until either a continuous 80 mins occurs or alarm is cancelled.

Note: The 5 minute period is any 5 min interval from alarm time and not 5 min from each snooze repeat.

3. Sleep output goes low after a sleep initiate for the period of time set by sleep potentiometer. (Will be overridden by Wake if sooner.)

Colon Utilization

	COLON CONDITIONS	
FUNCTION	BOTTOM	TOP
Set time	on	off
Set alarm	off	on
Stopped (Sync)	off	off
Run (alarm not requested)	1Hz	off
Run (alarm requested)	1Kz	1Hz
Snooze period	1Hz	1Hz

Sleep dot is on for sleep timer running, flashing for post line interrupt (removed from flashing by movement of S.T. or S.A. to '0')

Stand-By Operation

If a circuit is employed to change the IC power source to battery during line failure, e.g. two diodes, then if the external timing components of oscillator 1 are set to give 8KHz (nominally R = 120K Ω = 2200pF), then the IC will maintain operation to an accuracy of one part in 120, i.e., 30 secs/hr, during the failure. On return to main power the sleep indicator will flash at 1Hz to notify user that indicated time could be in error.

The standby condition is detected by the failure of oscillator 2 to oscillate, therefore oscillator 2 is connected to the line-derived power source, not the battery.

It is assumed OSC 2 input has gone to zero volts.

To remove flash condition take S.T. or S.A. momentarily to zero.

Analog Sleep Control

A second oscillator is provided on IC whose frequency can be controlled by an RC network. The oscillator is identical to oscillator one (Standby oscillator) and occupies the same silicon real estate location ensuring that process variations, temperature variations and voltage variations have as nearly as possible identical effects on frequency stability. Oscillator 1, which is set to 8KHz is divided down to 50Hz (20.0 msecs) and is used as a gating time for oscillator 2 (Sleep Timer Source). The number of gated counts is loaded in the sleep timer (capacity 160 counts) and subsequently counted up at one per minute until 160 is reached.

The range of sleep time is controlled by varying OSC 2 resistance. At 4:1 change in resistance will give variation of 160 to 40 gated pulses, this giving a sleep time of 0 to 120 minutes.

NOTE:

Minimum sleep time to ensure correct snooze operation should be a minimum of 5 minutes.

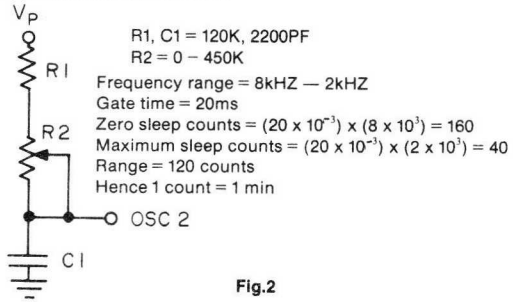


Fig.2

To initiate the sleep timer both S.T. and S.A. must logically be the same, and INC HR/SIN must be momentarily at zero. (See later section).

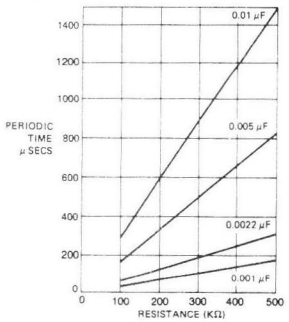


Fig.3 OSCILLATOR CHARACTERISTICS FOR V_P = 10V

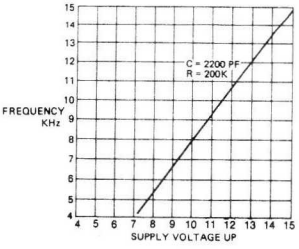


Fig.4 OSCILLATOR CHARACTERISTICS WITH VOLTAGE

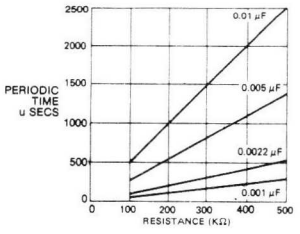


Fig.5 OSCILLATOR CHARACTERISTICS FOR V_P = 7.5V

Operation Clock Radio Example
(showing some features and their use) - ref Figs.21 and 22.

Start-Up
Radio is connected to line for 1st time, then battery is inserted.

Assume following switch position RADIO OFF, SET TIME SWITCH = RUN

Actions
Display will illuminate and read 12:00 sleep indicator will flash at 1Hz. Set clock as indicated previously (Flashing will cease).

In 24hr mode 0:00 will illuminate with flashing sleep indicator.

Snooze Bar Action
IN RADIO OFF POSITION

1st button depression	Low volume radio (set required volume)
2nd button depression	Radio off
3rd button depression	Radio on low volume
4th button depression	Radio off

etc. . . .

IN RADIO ON POSITION
Radio comes on high volume (set wake volume required)

1st button depression	Low volume radio (mute facility)
2nd button depression	High volume
3rd button depression	as 1
4th button depression	as 2

Radio Auto
In auto, alarm is requested at "set alarm" time. If sleep is desired press button. Subsequent button pushes will have same effect as in radio "off" position.

Select Wake to Alarm Tone or Radio
Assume radio selected

At alarm time radio will come on at wake volume setting.

1st button depression	Radio will switch to low volume
2nd button depression	Radio will switch off
3rd button depression	Radio back a low volume

If after first depression radio is left untouched, radio will return to wake volume after five minutes.

If after 2nd depression radio is left untouched, radio will stay off for five minutes then return to wake volume.

This wake volume, if left, will be maintained for 80 mins unless radio is returned to radio ON or radio OFF switch position, changing switch momentarily from auto to ON or OFF and back to auto will reset alarm and re-request for same time next day. The above, repeating snooze, can be maintained indefinitely if button is pushed before 80 mins elapses.

Note: 80 mins is timed either from alarm time, if untouched, or 80 mins from last button depression

Select Wake to Alarm Tone
The alarm tone or buzzer is obtained by placing positive feedback around the audio amplifier or radio in such a manner that the desired sound can be achieved and the feedback can be stopped by open circuit one point in the network.

At alarm time buzzer will sound:

On 1st button depression	Buzzer will cease and radio will switch to low volume
2nd button depression	Radio and buzzer will be off

If after first depression radio is left untouched, radio will return to buzzer after 5 mins.

If after 2nd depression radio is left untouched, radio and buzzer will be off and at 5 mins BUZZER WILL AGAIN SOUND.

As for radio position—radio will reset after 80 mins for 24 hrs. At any time in buzzer sequencing, buzzer radio select can be changed over to radio, then the radio will alternate high-low volume with button. Cancelling in buzzer mode is identical to radio mode.

Typical Application
To combine the S.A. and S.T. functions to provide simple and rapid clock setting. It is suggested that the follwing is incorporated in the clock radio.

Two toothed wheels are placed over two separate sprung contacts and coupled to two concentric rotating knobs, (say 12 teeth each) along side is a three position switch labeled 'set time, run, set alarm .

To set clock, select time or alarm and rotate Hrs knob, or mins knob, each click will result in one unit change of time, rapid rotation will result in 12 increments per revolution of knob.

The above procedure results in an easy to use system with the advantage over mechanical clocks of independent hrs and mins setting.

NOTE:
No carries from mins to hrs can occur during setting of time or alarm.

Use of Auto Tape
Fig.21 shows - the facility for automatically switching on an appliance (e.g. tape recorder) at a specific time and keeping appliance active for a period of time up to 120 mins. In this mode the wake output is made to start the sleep - timer at the wake time.

Use of 5 Min Delayed Alarm with Appliance Switching
In this mode of operation the wake 1 output is made to cancel the first alarm through the SC (inc hr) input such that radio or alarm time will only occur at the end of the first snooze period.

This result in appliance being activated at set alarm time and after 5 mins the alarm or radio will sound.

Fig.6 — shows a typical clock-radio block diagram
Fig.7 — shows the chip/display circuit.

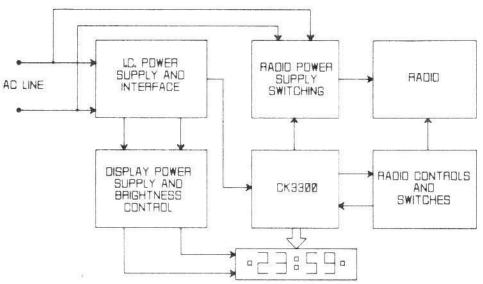


Fig.6

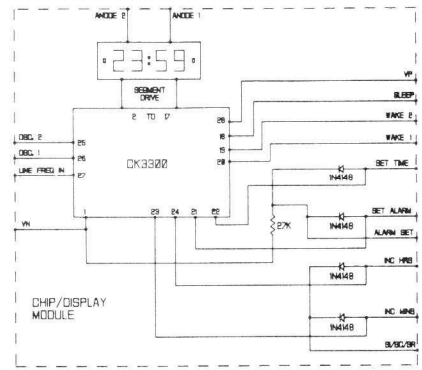


Fig.7

CONSUMER

Interface with a Radio

There are many possible configurations of clock radios in use today and a wide range of different radio chassis are employed in these units. It is necessary therefore that the clock radio I.C. be sufficiently flexible to allow simple interfacing to be accomplished.

The following section gives different options, features and interfacing to demonstrate some of the approaches possible with the CK3300.

Power Supply Interface

To enable any existing line operated radio chassis to be used with the minimum of changes it is suggested that the following power supply is used with the adoption of a 2nd line transformer. This will (a) reduce the need for a change at the existing transformer. (It is unlikely that the existing transformer will be capable of providing the additional power required of the display).

a. Allow the electronic clock movement to be self contained therefore, keeping the interface wiring to a minimum.

b. Allow the same electronic movement to be used with several radio chassis.

Options

1. Without battery standby facility Fig.8
2. With battery standby facility Fig.9

Display Interface and Power Source

Four options are shown

1. No brightness control Fig.10
2. Day/night brightness (two level) Fig.11
3. Manual brightness control Fig.12
4. Automatic brightness control Fig.13

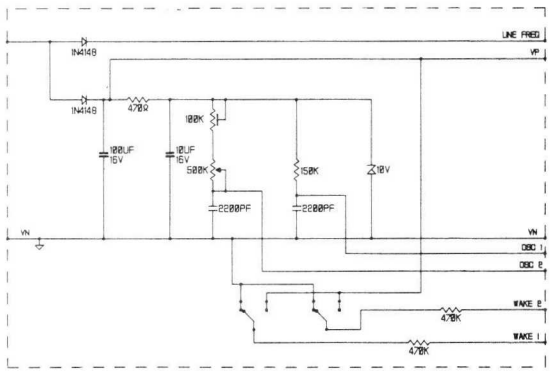


Fig.8 POWER SUPPLY INTERFACE WITHOUT STANDBY

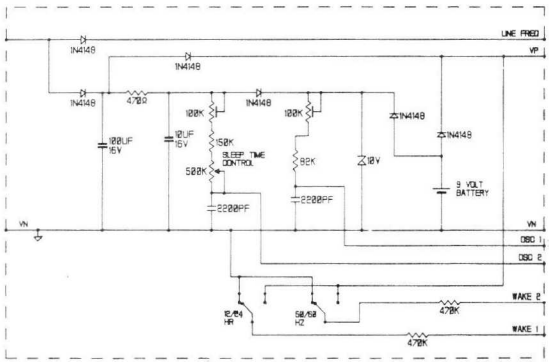


Fig.9 POWER SUPPLY INTERFACE WITH STANDBY OPTION

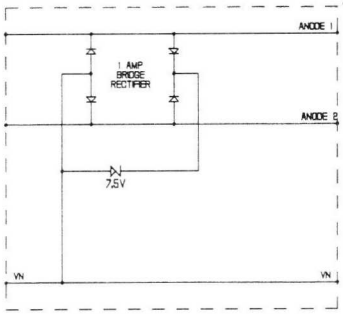


Fig.10 NO BRIGHTNESS CONTROL

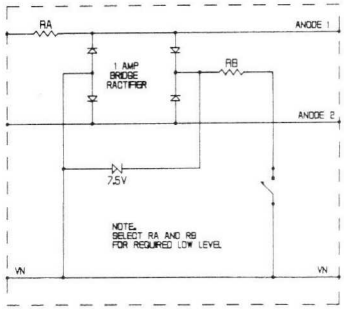


Fig.11 TWO LEVEL BRIGHTNESS CONTROL

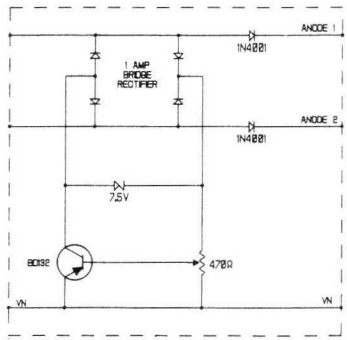


Fig.12 MANUAL BRIGHTNESS CONTROL

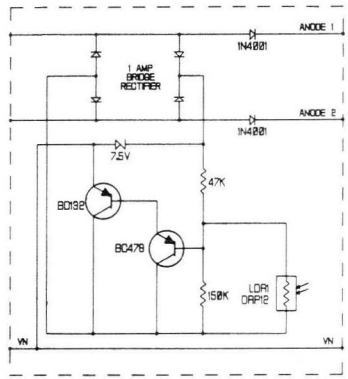


Fig.13 AUTOMATIC BRIGHTNESS CONTROL

Radio Switching

Option 1 Push button operation (Fig.14)
Option 2 Rotary switch operation (Fig.15)

Radio Powering

Option 1(Fig.16A, 16B) Direct audio amplifier control (no active components)
Option 2 (Fig.17) Power supply switching using Transistor
Option 3 (Fig.18) Power supply switching using a relay

Tone Generation

Option 1 (Fig.19) Saw tooth generation independent of radio
Option 2 (Fig.20) Sine wave generation independent of radio
Option 3 (Fig.15,16B) Sine wave using the existing radio audio amplifier

Additional Facilities

1. Automatic tape recording (Fig.21)
2. Appliance switching with delayed alarm (Fig.21)
3. Wake to normal radio with 5 minute alarm over-ride (Fig.21)
4. Wake to quiet radio with 5 minute alarm over-ride (Figs. 21 and/or 22)
5. Ratio muting during normal radio listening (Figs.21 and /or 22)

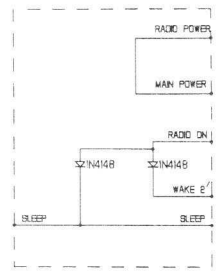


Fig.16a RADIO SWITCHING BY BIAS CHANGE

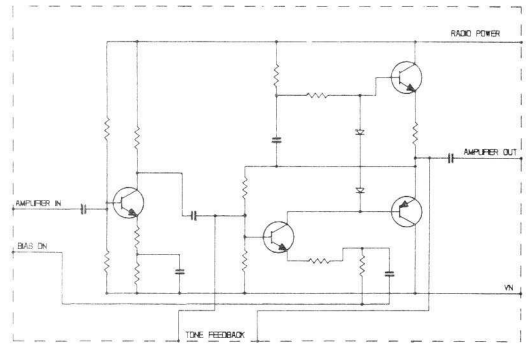


Fig.16b TYPICAL TRANSFORMERLESS AUDIO AMPLIFIER

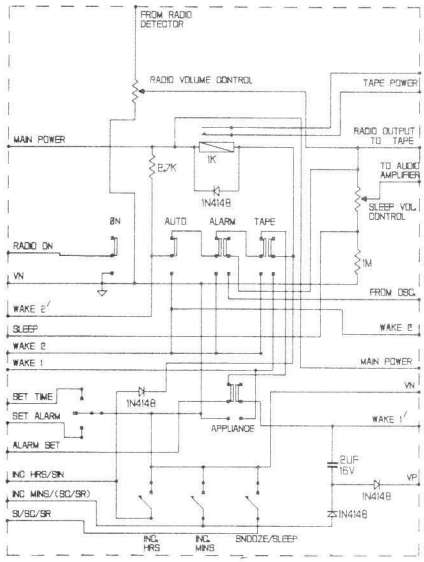


Fig.14 RADIO SWITCHING

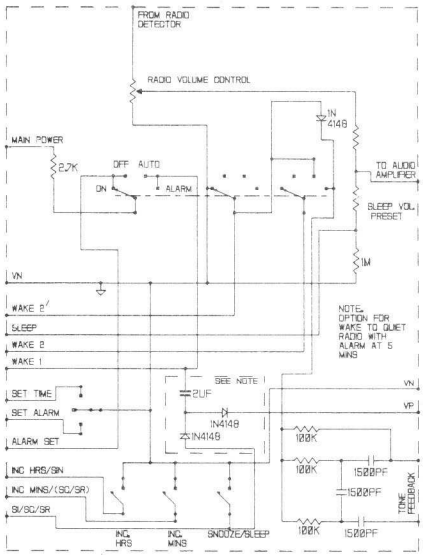


Fig.15 RADIO SWITCHING

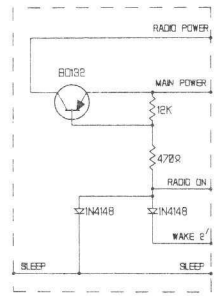


Fig.17 RADIO POWER SWITCHED BY TRANSISTOR

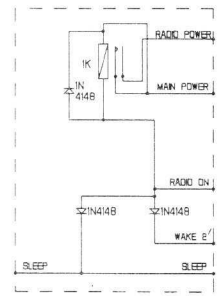


Fig.18 RADIO POWER SWITCHED BY RELAY

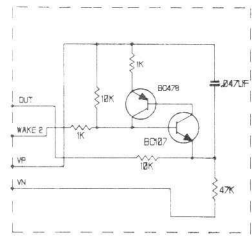


Fig.19 SAW TOOTH OSC

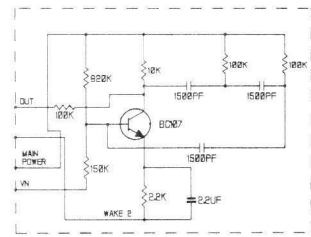


Fig. 20 SINE-WAVE OSC

CONSUMER

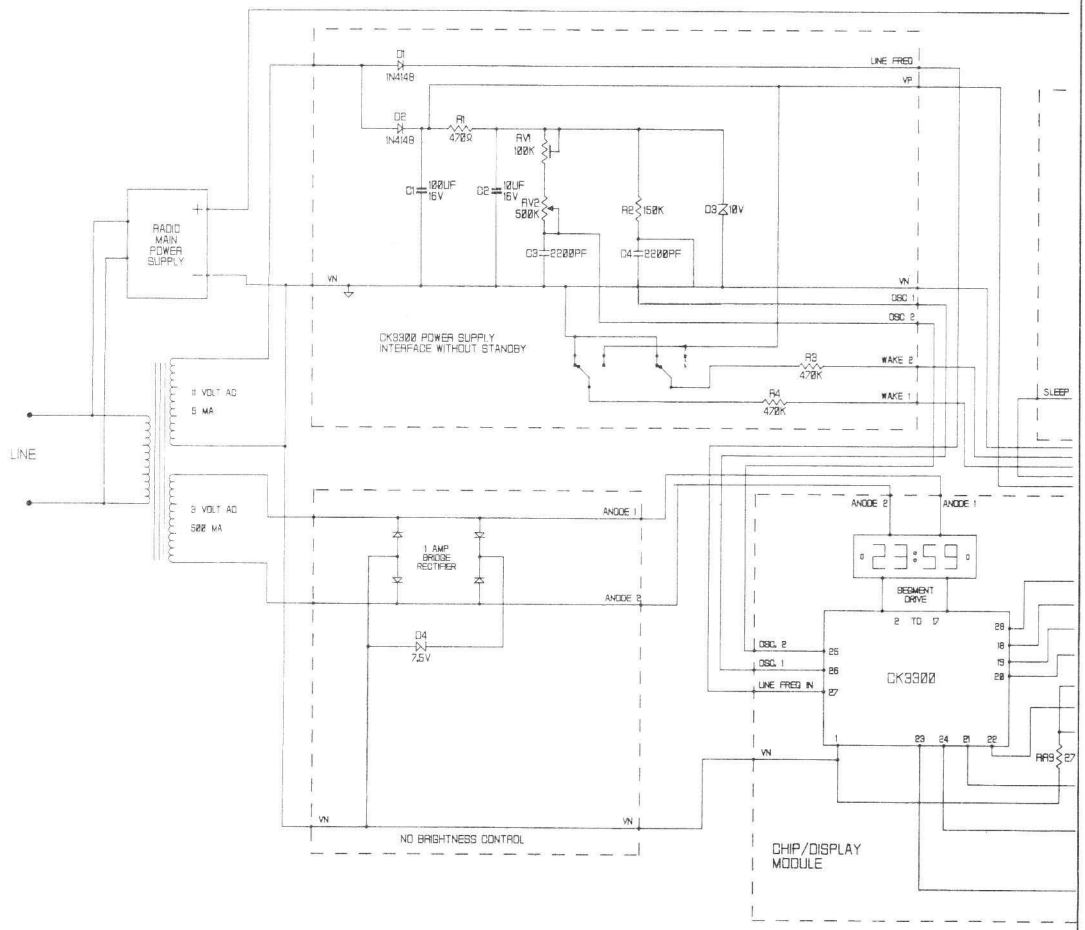


Fig.21(a) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

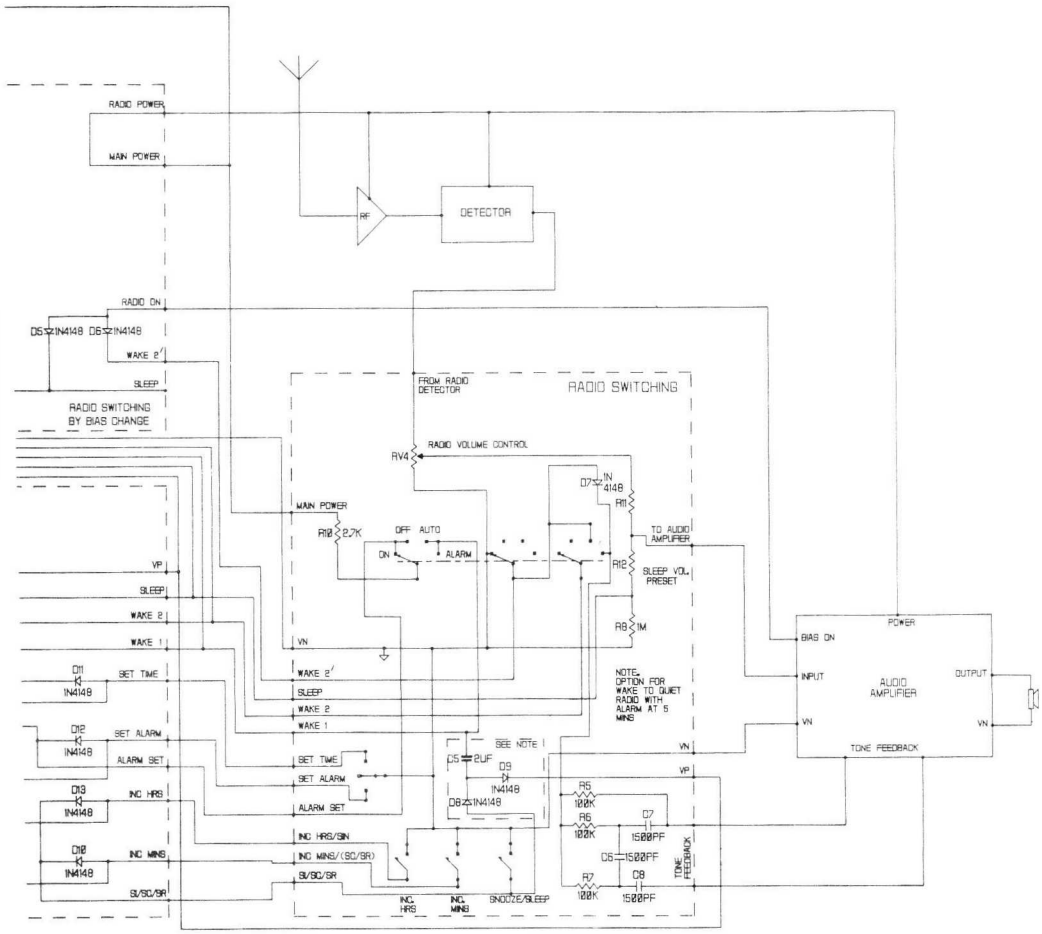


Fig.21(b) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

CONSUMER

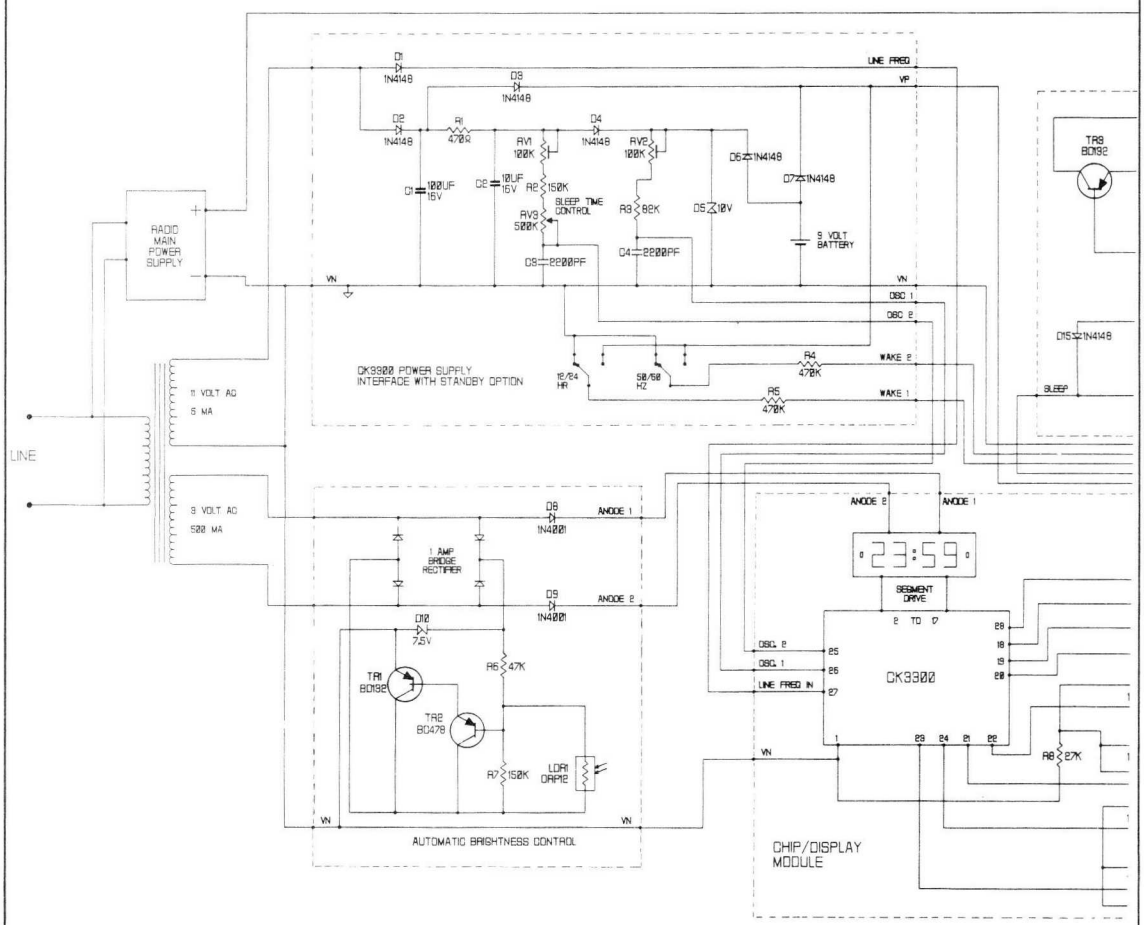


Fig. 22(a) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

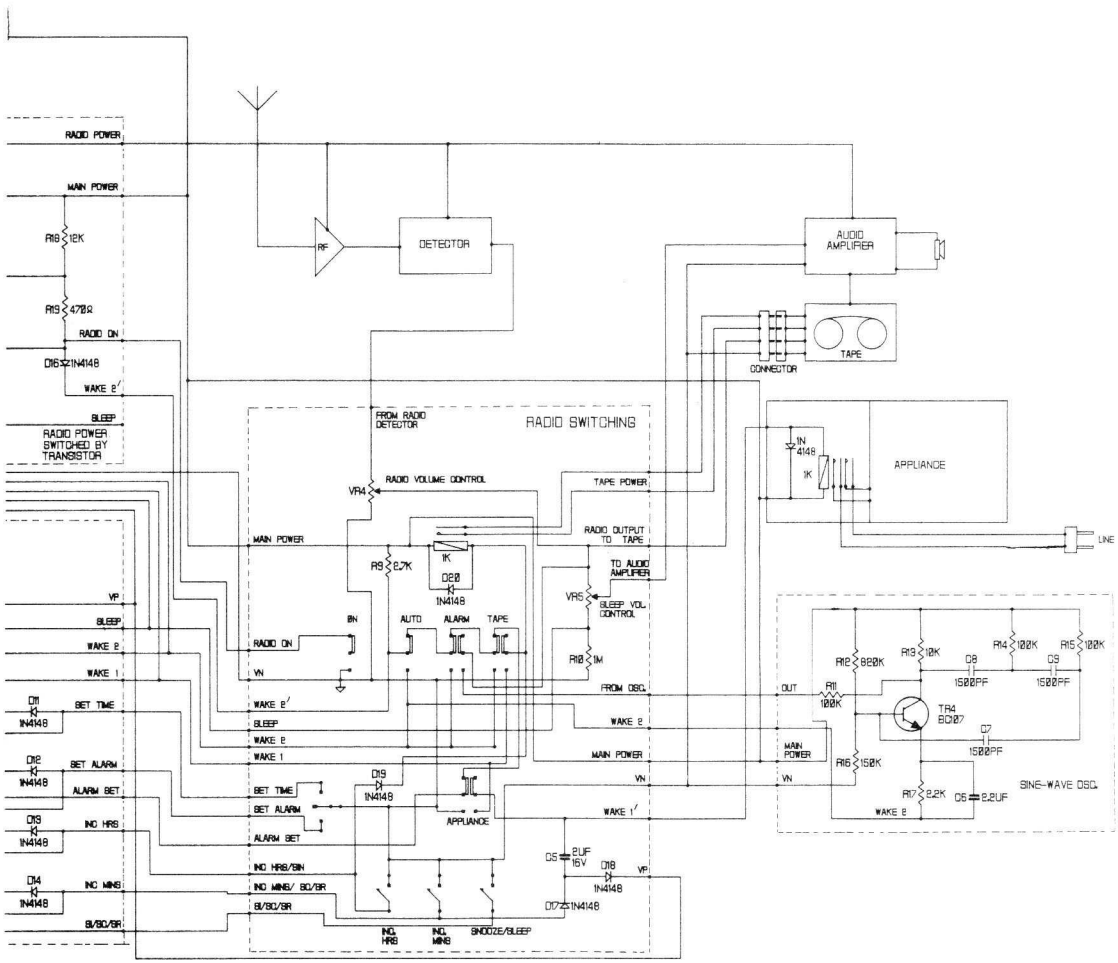


Fig.22(b) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage any pin with respect to V_n ..... +20V
Storage temperature ..... -65°C to +150°C
Operating temperature ..... -20°C to +70°C
Lead temperature (soldering 10 sec) ..... +300°C

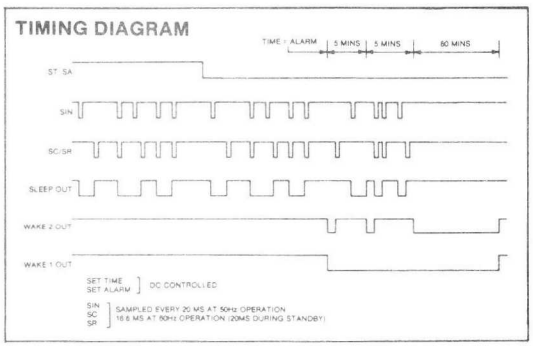
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Typ**	Max	Units	Conditions
Power Supply Voltage	7	10	15	Volts	$V_n = 0V$
Supply Current	—	2	—	mA	
50/60HZ Input					
Frequency (must be identical to anodes)	0	50/60	50,000	Hz	$V_p = 10V$
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Inputs (Excl Oscillators)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Segments Out (on)	—	30	—	mA	$V_{OUT} = 1.5V$
(off)	—	10	—	μA	
Wake 1, 2, Sleep Out (on)	—	30	—	mA	$V_{OUT} = 1.5V$
(off)	—	10	—	μA	
Wake 1, 2 (As Inputs)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Oscillators 1 and 2					
Hi level	—	5.5	—	Volts	Free run
Lo level	—	3.5	—	Volts	
Reset Level	—	—	0.7	Volts	

Unless specified otherwise, characteristics are defined with $V_p = 10V$ at $T_A = +25°C$.
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Under no circumstances during IC operation must any pin either input or output be taken to a voltage more negative than V_n or IC malfunction will occur.
2. No input or output must be taken to a positive voltage greater than 20 volts or permanent damage can result.
3. No output must be allowed to dissipate a continuous power in excess of 100mW.
4. Total chip continuous power dissipation must not exceed 500mW.
5. The total current being returned to V_n through all device pins must not exceed 1 amp.

TIMING DIAGRAM



Input and Output Characteristics

INPUTS
S.A.
S.T.
INC HR (SIN)
INC MIN (SC/SR)
} Active pull up's to V_p / Operate level logic '0' } 250KΩ

50/60HZ count input, active pull down
For correct operation duty cycle of 50/60Hz must be 1:1 ± 20%

OUTPUTS
Normally open circuit
Operate "on" (low impedance typically 50Ω)

INPUTS
Wake 1 - as input '1' = 12hr '0' = 24hr
Wake 2 - as input '1' = 60Hz '0' = 50Hz

CLOCK INPUT NOISE ELIMINATION TIMING
50/60Hz - strobed every 4ms internally for less than 1 μs

Testing I.C. Facilities
1. Master reset: This can be activated by pulling OSC1 (Pin 26) and OSC 2 (Pin 25) to zero volts together.
2. Internal debounce and predivider logic may be bypassed if OSC 1 is taken to zero volts while OSC 2 is left running.
a. Under this condition Inc Hrs and Inc Mins pins are not debounced to allow fast incrementing for test purposes.
b. Also in this mode the 50/60Hz input pin is directed straight to the main counters under control of the sleep pin. If Sleep pin at '0'—50/60Hz input clocks 120 minute sleep counter, and with Sleep at '1' it clocks the main minutes count by passing the debounce and divide by 50/60 counter. Under this condition it also clocks the 5 minute snooze counter.

4 Digit Automobile Clock Circuits

FEATURES

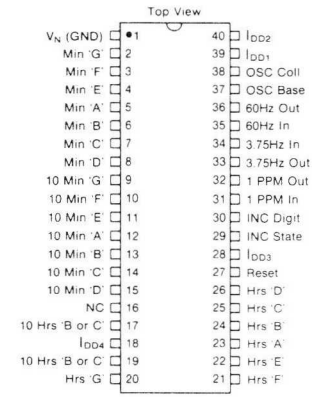
- Direct segment drive to 4 digits, two hours digits and two minutes digits:
  - —CK3500, 20mA/segment for LED displays.
  - —CK3500F, 300μA/segment for Fluorescent displays.
- Timing designed for 3.58MHz color TV crystal.
- Two button setting of the time:
  1) Increment clock state
  2) Increment selected digit
- Four clock states:
  1) Set hours
  2) Set tens of minutes
  3) Set units of minutes
  4) Run
- Selected digit for setting flashes at 3.75Hz rate.
- Internal switch debounce.
- Clock resettable to 1:00.
- May be operated from a wide range of power supplies (Device is powered from a current source.)
- Can be driven from a 60Hz signal.
- Low power consumption (display off).

DESCRIPTION

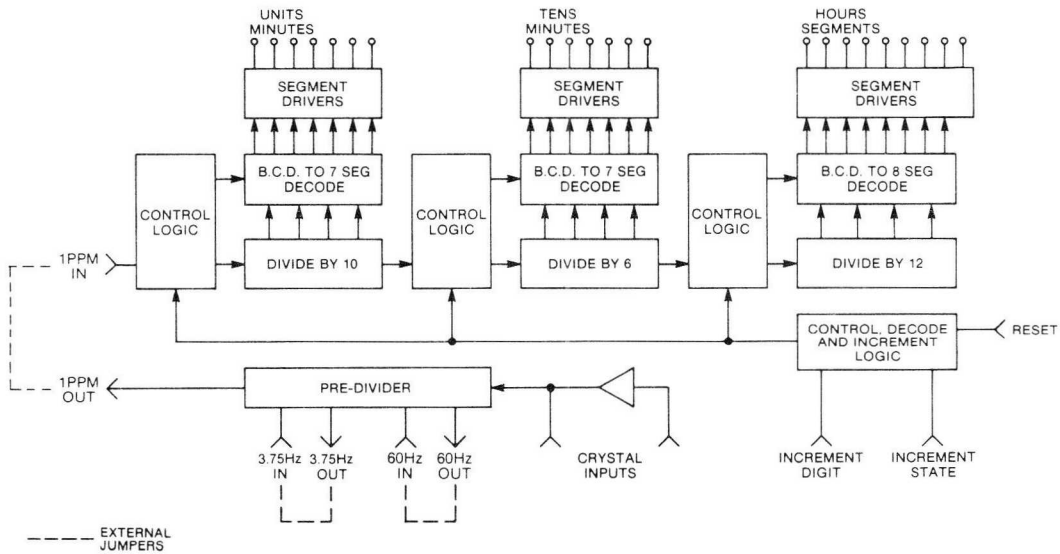
The CK3500/CK3500F are bipolar LSI circuits utilizing General Instruments' I^2L technology. Each circuit contains an on-chip crystal oscillator and the logic to display hours and minutes in a 12-hour format. The time is set with two internally debounced switches. Each chip also has direct segment drive capability, thus requiring a minimum of external components.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



CONSUMER

PIN FUNCTIONS

Segment Outputs (23 pins) The segments of each digit are driven separately. The outputs are open collector devices, and are "ON" when the segments to be displayed are selected.

I_{DD4} Positive supply currents to the decoders and segment drivers only (to conserve battery drain with ignition off).

I_{DD1}, I_{DD2}, I_{DD3} Positive supply currents to the oscillator and count down circuits.

V_N Negative supply (normally ground).

Crystal Inputs (2 pins) Connection of external crystal (frequency source).

Increment Digit This input increments the selected digit by one for each depression of the digit increment push-button (i.e. each time input is connected to V_{DD}).

Increment Clock State There are four clock states sequentially selectable for each consecutive depression of the increment state push-button (i.e. each time this input is connected to V_{DD}). The four clock states in order of access are as follows:

1. Set Hours
2. Set Tens of Minutes
3. Set Units of Minutes
4. Run

(NOTE: The sequence starts over with continued momentary connections of this input to V_{DD}).

Selected digits will flash at a 3.75Hz rate to indicate the clock state.

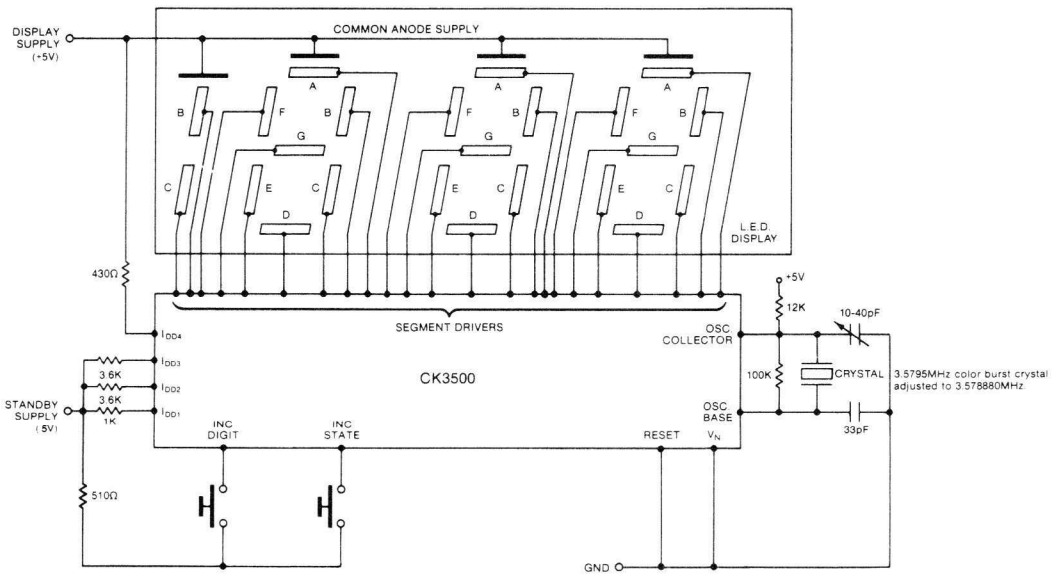
TIME SETTING OPERATION

Two switches are utilized for the time setting of the clock. They each apply a positive voltage to the appropriate pin on the chip. To describe their operation, suppose that the clock is running normally (in the RUN state). Closing the INC STATE switch causes the hours digit/digits to flash at a 3.75Hz rate. At this point, the INC DIGIT switch may be closed, causing the hours digits to increment one count each time the switch is closed. When the desired hours count is reached, the INC STATE switch is again closed, causing the tens of minutes digit to flash. Closing the INC DIGIT switch then increments the tens of minutes digit. When the desired digit is reached, the INC STATE switch is again closed, causing the units of minutes digit to flash. This digit is set as before, repeatedly closing the INC DIGIT switch. Finally, the INC STATE switch is again closed, placing the clock back in the RUN mode. When the RUN mode is entered and the units of minutes digit has been changed, the seconds are reset to zero, giving an exact minute count. In the RUN mode, closure of the INC DIGIT switch has no effect.

DISPLAY INTENSITY (CK3500)

When the LED is supplied from a voltage in the range of 2.5 to 5 Volts, the current into injector 4 serves as an intensity control. For voltage over about 3.5 Volts, a resistor should be included in series with the display anode. The value should be 2.5 (V-2.5) ohms and will dissipate a maximum of 0.4(V-2.5) watts. This resistor serves to limit the chip dissipation to acceptable values.

CK3500 CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (CK3500)

Maximum Ratings*

Injector Current (per injector)—pins 18, 28, 39, 40 ..... 20mA
Input Current—pins 31, 34, 35 ..... 10mA
Output Voltage ..... +3.0V
Output Current: Display Drivers 20mA
Frequency Points 1mA
Power Dissipation: Display Drivers ..... 20mW/seg.
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −40°C to +85°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Characteristics	Min	Typ	Max	Units	Conditions
Injector Voltage	0.5	0.7	1.0	V	
Injector Current:					
I_{DD1} (1st divider)	4.5	5.2	6.3	mA	
I_{DD2} (2nd divider)	0.75	0.85	1.0	mA	
I_{DD3} (clock)	1.75	2.0	2.25	mA	at I_L = 20mA max.
I_{DD4} (display driver)	5.4	6.0	6.6	mA	at I_L = 20mA max.
Oscillator Supply	2	2.5	5	V	
Output Current	—	—	20	mA	per segment
Segment Leakage	—	—	100	μA	at 3.0V
Switch debounce time	16	—	3.0V	ms	
Oscillator Frequency	—	3.578880	—	MHz	derived from crystal
Oscillator Beta	20	40	—	—	
Logic "1":					
Frequency Inputs	—	open	—	—	
Increment Digit/State	2	—	5	V	
Logic "0":					
Frequency Inputs	0	—	0.3	V	at 1mA
Increment Digit/State	—	open	—	—	
Input Impedance					
Increment Digit/State	500	600	700	Ω	

ELECTRICAL CHARACTERISTICS (CK3500F)

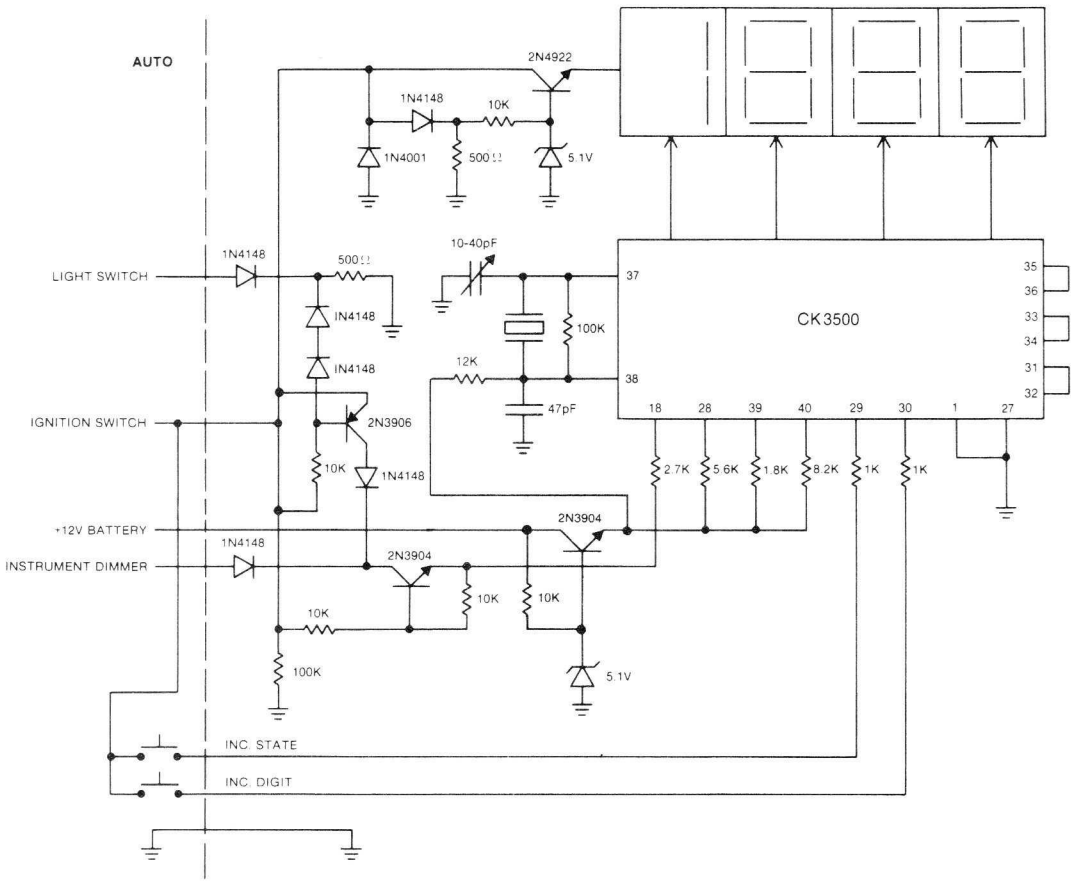
Injector Current (per injector)—pins 18, 28, 39, 40 ..... 20mA
Input current—pins 31, 34, 35 ..... 5mA
Output Voltage ..... −25V
Output Current: Display Drivers 300μA
Frequency Points 1mA
Power Dissipation: Display Drivers ..... 7mW/seg.
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... −40°C to +85°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

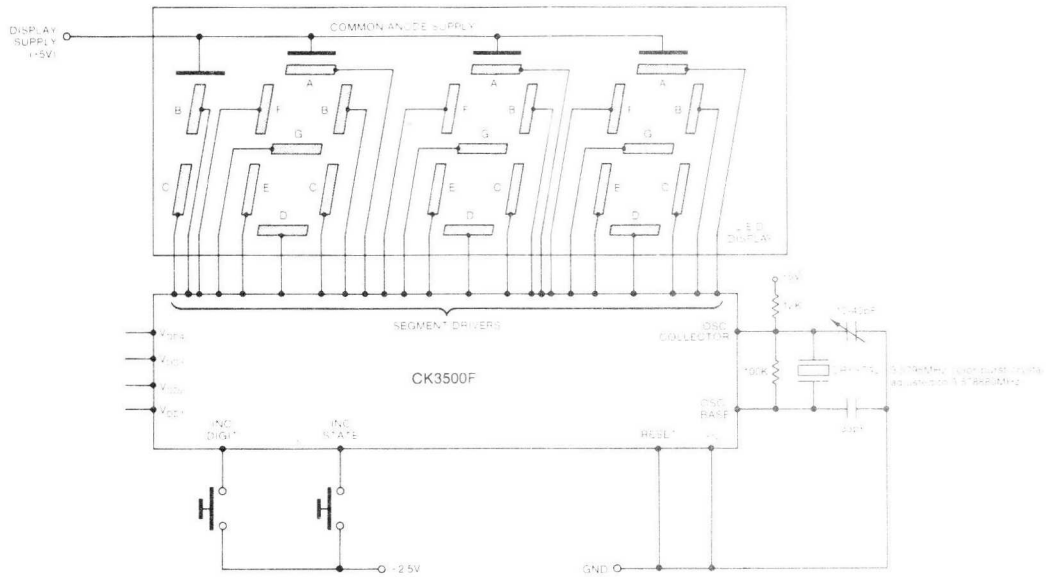
Characteristics	Min	Typ	Max	Units	Conditions
Injector Voltage	0.55V	0.7	1.0	V	
Injector Current:					
I_{DD1} (1st divider)	3.85	4.3	4.75	mA	
I_{DD2} (2nd divider)	0.75	0.85	1.0	mA	
I_{DD3} (clock)	1.75	2.0	2.25	mA	
I_{DD4} (display driver)	4.0	—	25	mA	
Oscillator Supply	2	2.5	5	V	
Output Source Current	—	—	300	μA	per segment at 1.5V
Switch debounce	—	16	—	ms	
Oscillator Frequency	—	3.578880	—	MHz	derived from crystal
Oscillator Beta	20	40	—	—	
Logic "1":					
Frequency Inputs	—	open	—	—	
Increment Digits/State 2	2	—	5	V	
Logic "0":					
Frequency Inputs	0	—	0.3	mA	at 0.2 mA
Increment Digits/State	—	open	—	—	
Input Impedance					
Increment Digit/State	2.4	3	3.6	kΩ	

CONSUMER

CK3500 AUTOMOBILE CLOCK SYSTEM DIAGRAM



CK3500F CONNECTION DIAGRAM



MICRO ELECTRONICS

MUSIC

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
TOP OCTAVE GENERATORS	Generates a complete octave of musical frequencies.	AY-1-0212	8-48
		AY-1-0212A	8-48
		AY-3-0214	8-50
		AY-3-0215	8-50
		AY-3-0216	8-50
LATCHING NETWORK	Establishes priority of 13 pedal latch inputs/outputs.	AY-1-1313	8-54
RHYTHM GENERATOR	Generates 6 rhythms, drives 8 instruments.	AY-5-1315	8-56
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass.	AY-5-1317A	8-58
PIANO KEYBOARD	Electronically simulates piano keyboard operation.	AY-1-1320	8-62
FREQUENCY DIVIDERS	4 stage divider.	AY-1-5051	8-66
	5 stage divider.	AY-1-6721/5	8-66
	6 stage divider.	AY-1-6721/6	8-66
	7 stage dividers.	AY-1-5050	8-66
		AY-1-1007B	8-52

Top Octave Generators

FEATURES

- Wide Input Frequency Range:
  1) AY-1-0212—250kHz to 1.5MHz
  2) AY-1-0212A—250kHz to 2.5MHz
- Low Impedance Push-Pull Outputs
- Full Musical Scale in One Chip
- Zener Protected Input

DESCRIPTION

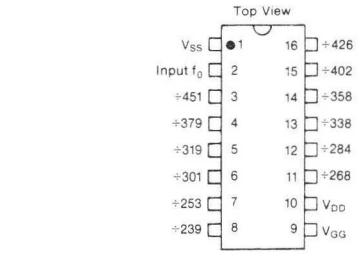
The AY-1-0212/0212A Top Octave Generators are digital tone generators which produce, from a single input frequency, a full octave of twelve frequencies on twelve separate output terminals.

The AY-1-0212/0212A each consist of twelve divider circuits which divide the input by an exact integer to produce a chromatic scale of twelve notes. When used in conjunction with an oscillator and frequency dividers, a system may be configured which generates all the frequencies required by an electronic music synthesizer.

The AY-1-0212 operates with input frequencies of up to 1.5MHz. The AY-1-0212A operates up to 2.5MHz.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



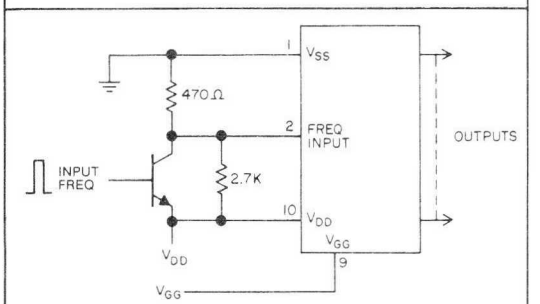
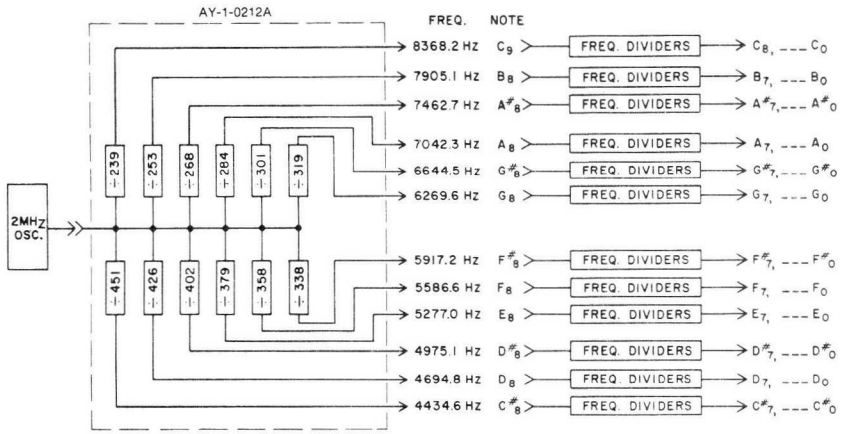


Fig. 1 TYPICAL INPUT BUFFER (IF REQUIRED)

BLOCK DIAGRAM / TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to Vss .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +70°C

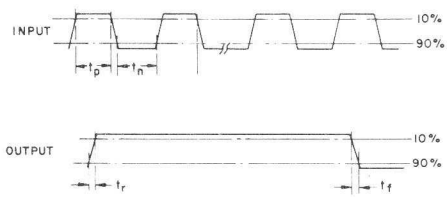
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

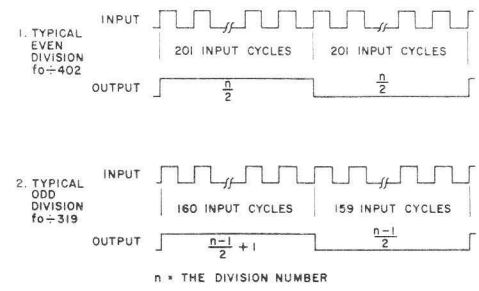
Standard Conditions (unless otherwise noted)
V_{SS} = GND
See Fig. 2 for V_{DD} and V_{GG} Operating Voltages

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	10	μA	at 27V
Input Positive Level	+0.3	—	−2.0	Volts	
Input Negative Level	−10.0	—	V_{DD}	Volts	
Output on Impedance to V_{DD}	—	—	3500	Ω	1.0V across the device with 17K load to −6V.
Output on Impedance to V_{SS}	—	—	3500	Ω	
I_{GG} Supply Current	—	—	16	mA	
I_{DD} Supply Current	—	—	20	mA	
AC CHARACTERISTICS					
AY-1-0212 Input Frequency f_o	.25	—	1.5	MHz	See Fig.3
AY-1-0212A Input Frequency f_o	.25	—	2.5	MHz	
Input Capacitance	—	5	10	pF	1 MHz
Input Positive Level Width t_p	.33	—	-	μs	AY-1-0212
Input Negative Level Width t_n	.33	—	—	μs	AY-1-0212
Input Positive Level Width t_p	.2	—	—	μs	AY-1-0212A
Input Negative Level Width t_n	.2	—	—	μs	AY-1-0212A
Output Rise Time t_r	—	1	—	μs	no load
Output Fall Time t_f	—	1	—	μs	no load

** Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





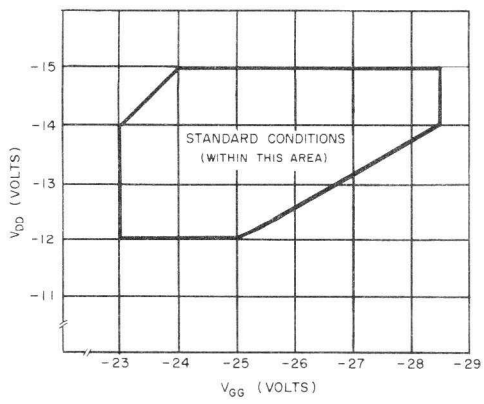


Fig. 2 OPERATING VOLTAGES

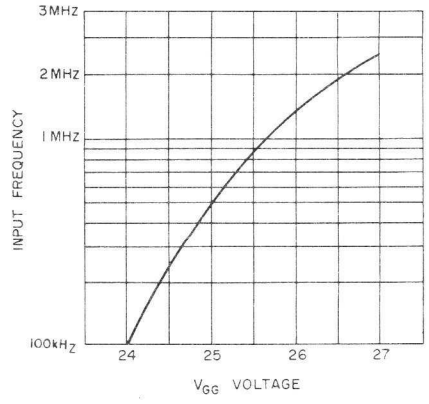


Fig. 3 TYPICAL FREQUENCY vs. V_{GG} VOLTAGE OPERATION

CONSUMER

Master Frequency Generator/Top Octave Generator

FEATURES

- Wide input frequency range: 100 kHz to 4.5 MHz
- Single power supply
- Full musical scale on one chip
- Low impedance push-pull outputs
- Zener protected input.
- AY-3-0214: 12 outputs — 50% Duty Cycle (Highest accuracy)
- AY-3-0215: 13 outputs — 50% Duty Cycle
- AY-3-0216: 13 outputs — 30% Duty Cycle

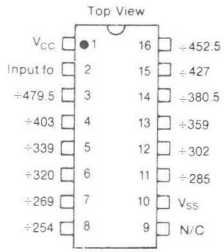
DESCRIPTION

The General Instrument M.F.G./T.O.G. is a digital tone generator which produces, from a single input frequency, 12 or 13 semitone outputs fully spanning the equal tempered scale. When used in conjunction with an oscillator and frequency dividers such as the G.I. AY-1-1007B, a system may be configured which generates all the frequencies required by an electronic music synthesizer.

PIN CONFIGURATION

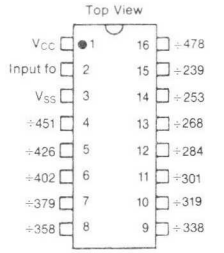
16 LEAD DUAL IN LINE

AY-3-0214

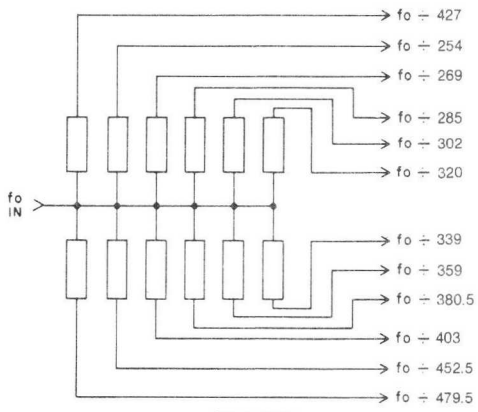


16 LEAD DUAL IN LINE

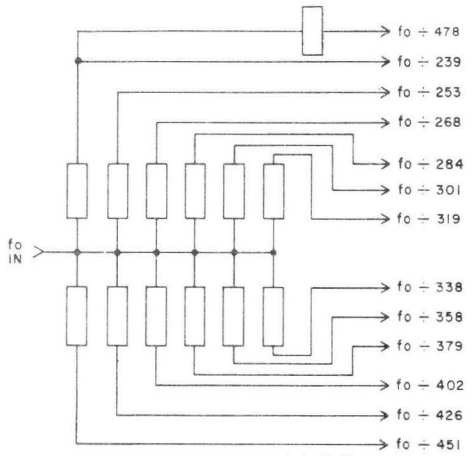
AY-3-0215/AY-3-0216



BLOCK DIAGRAMS



AY-3-0214



AY-3-0215/AY-3-0216

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3
Storage Temperature ..... -55°C to +150°C
Operating Temperature (T_A) ..... 0°C to +50°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +10V to +16V

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Low	0.0	—	0.8	V	
High	V_{CC} -3.0	V_{CC}	V_{CC}	V	
Frequency	100	—	4500	kHz	
Rise Time	—	—	30	ns	4.5 MHz
Fall Time	—	—	30	ns	4.5 MHz
Duty Cycle	40	50	60	%	
Capacitance	—	—	10	pF	
Outputs					
High	V_{CC} -1.5	—	V_{CC}	V	0.25 mA
Low	0.0	—	0.5	V	0.7 mA
Fall Time	—	—	2.5	μs	20K & 500 pF to 16V
Rise Time	—	—	2.5	μs	20K & 500 pF to V_{SS} when V_{CC}=16V
Duty Cycle	—	50	—	%	AY-3-0214/5
	—	30	—	%	AY-3-0216
Supply current	—	—	120	mA	16V, 4.5 MHz, 25°C

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

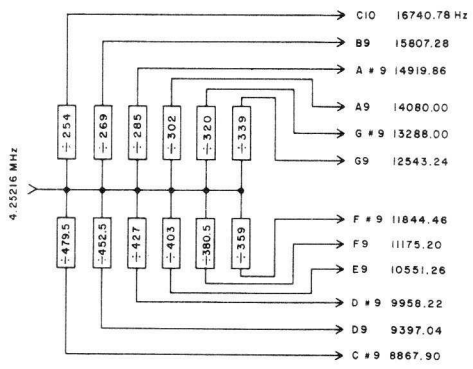
Fig.1 TYPICAL EVEN DIVISOR N = 404

Fig.2 TYPICAL ODD DIVISOR N = 403

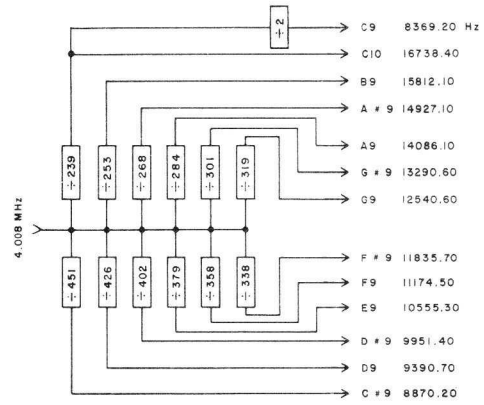
Fig.3 TYPICAL EVEN PLUS 0.5 DIVISOR N = 452.5

Fig.4 TYPICAL ODD PLUS 0.5 DIVISOR N = 479.5

TYPICAL APPLICATIONS



AY-3-0214



AY-3-0215/AY-3-0216

CONSUMER

7-Stage Frequency Divider

FEATURES

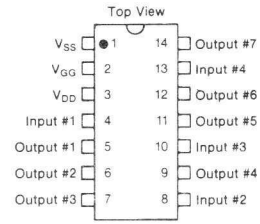
- Sine or Square Wave Input
- Low Impedance Push-Pull Outputs
- Seven Divider Stages
- Power-On-Reset

DESCRIPTION

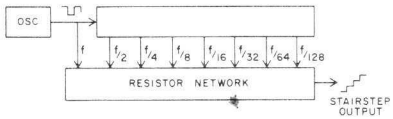
The AY-1-1007B is a monolithic frequency divider circuit which utilizes MOS technology. The divider circuit consists of seven flip-flops arranged in a 3-2-1-1 configuration and diffused into a single silicon substrate. The circuit can be driven from a sine or square wave input. Each flip-flop has a low impedance push-pull output which is capable of driving external circuitry as well as other flip-flops.

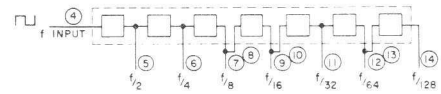
PIN CONFIGURATION

14 LEAD DUAL IN LINE

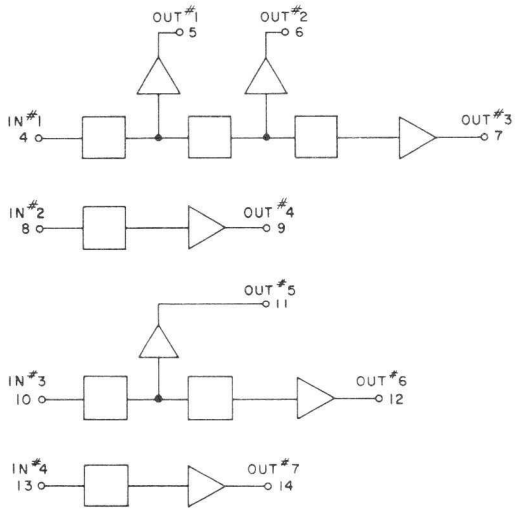


TYPICAL APPLICATIONS

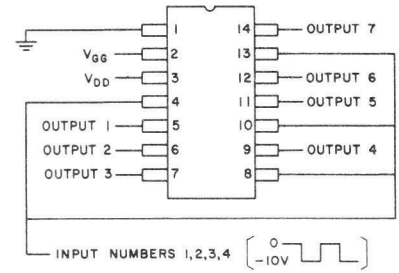




BLOCK DIAGRAM



CIRCUIT TEST CONFIGURATION



REFER TO TIMING DIAGRAM FOR OUTPUT PHASE AND FREQUENCY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{GG} = -27V ± 2V
$-14 < V_{DD} < +0.3V$

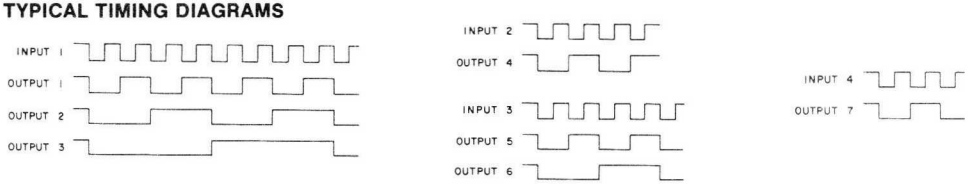
Characteristics	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	1	μA	$V_{IN} = -20V$
Input Positive Level	—	—	−2.0	Volts	
Input Negative Level	−9.0	—	—	Volts	
Output Positive Level	—	—	−1.0	Volts	$V_{GG} = -27V$, $V_{DD} = -12V$,
Output Negative Level	−11.0	—	—	Volts	$V_{GG} = -27V$, $V_{DD} = -12V$,
I_{GG} Supply Current	—	—	14.0	mA	$V_{GG} = -25V$,
D.C. Noise Immunity (Note 2)	+1.0	—	—	Volts	
AC CHARACTERISTICS					
Input Repetition Rate	D.C.	—	50	kHz	
Input Capacitance	—	—	5	pF	$V_{IN} = 0V$

**Typical values are at +25°C and nominal voltages.

Notes:

1. Outputs may be momentarily grounded (individually) without damage to the device.
2. D.C. noise immunity is defined as follows:
   "1" state N.I. = V_{OUT} "1" — V_{IN} "1" = [−10] −[−9] = 1V
   "0" state N.I. = V_{IN} "0" —V_{OUT} "0" = [−2] −[−1] = 1V
3. V_{DD} not used internally. Used for output negative supply only.
4. Typical output impedance to V_{SS} or V_{DD} is 1.2K

TYPICAL TIMING DIAGRAMS



CONSUMER

Priority Latching Network

FEATURES

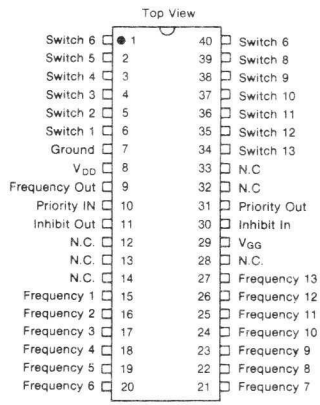
- Low Power Consumption
- Two or more units may be connected in tandem

DESCRIPTION

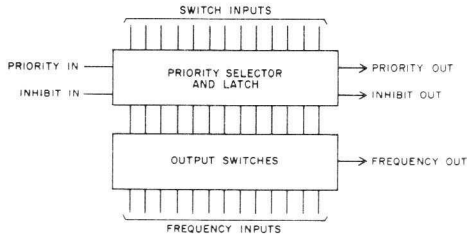
The AY-1-1313 Priority Latching Network is a LSI subsystem designed for use in electronic organ keyboard and pedal latching circuits. When any combination of one or more "switch" inputs is connected to logic "1" the output switch corresponding to the highest priority, or lowest number, input will close, connecting the selected frequency to the output frequency bus. The output switch will remain closed even if the input switch is released, and will remain closed until a new input switch closure occurs.

PIN CONFIGURATION

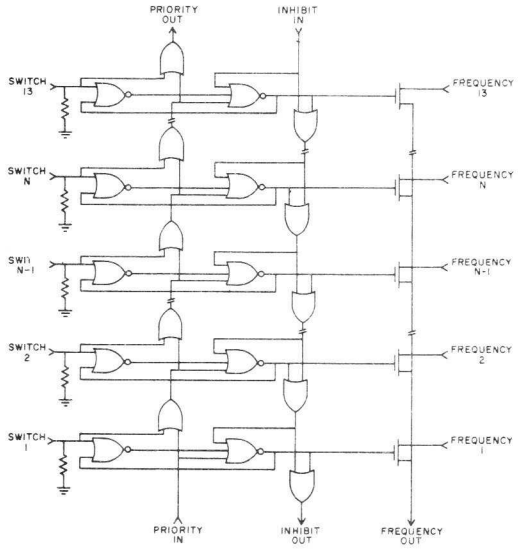
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} ..... -30V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature (T_A) ..... -20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

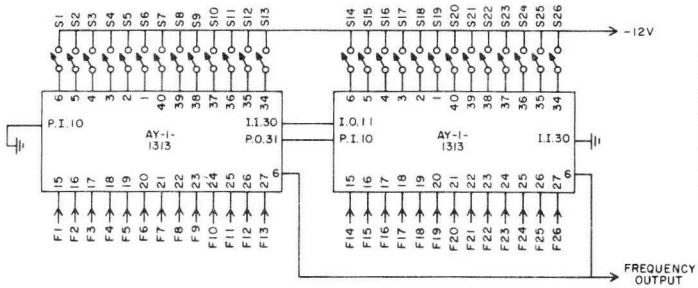
Standard Conditions (unless otherwise noted)

V_{DD} = -12±1V
V_{GG} = -27± 1.5V
V_{SS} = GND

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Switch Inputs Impedance	15	—	80	kΩ	Measured to Ground
Priority and Inhibit Inputs Impedance	1	—	—	MΩ	Measured to Ground
Input Logic "0"	—	—	-2	Volts	
Input Logic "1"	-9	—	—	Volts	
Output Logic "0"	—	—	-2	Volts	R_L = 47K to V_{DD}
Output Logic "1"	-9	—	—	Volts	R_L = 47K to V_{DD}
Frequency Output Switch					
Impedance — "ON"	—	—	20	kΩ	
"OFF"	5	—	—	MΩ	
I_{DD} Supply Current	—	—	8	mA	
I_{GG} Supply Current	—	—	1	mA	

**Typical values are at +25°C and nominal voltages.

TYPICAL APPLICATION



For multiple unit operation, the Priority Output of the higher priority unit is connected to the Priority Input of the lower, and the Inhibit Input of the higher priority unit is connected to the Inhibit Output of the lower. The Priority and Inhibit Inputs must be grounded when not in use.

CONSUMER

Rhythm Generator

FEATURES

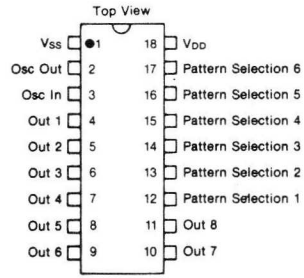
- Drives 8 instruments
- 32 beat long pattern
- 6 rhythm selections
- Internal oscillator
- Mask programmable rhythm pattern and pattern length
- Automatic reset for easy chord coupling

DESCRIPTION

The AY-5-1315 is a P-Channel MOS IC specifically designed for the Rhythm and Percussion section of an Electronic Organ and for Automatic Rhythmers. It contains all the logic circuits necessary to generate six sets of rhythm patterns driving eight instruments. The automatic reset feature allows it, when coupled with the chord section of the organ, to start on the downbeat every time a new chord is played. Selecting multiple patterns will result in a combination of the patterns selected. Tempo is externally adjustable from slower than largo to faster than presto. For added stability of the internal tempo oscillator a $\div 32$ circuit is provided. If an external tempo oscillator is used this circuit could be mask programmed out of the counter decoder chain. For added flexibility the output buffers could be mask programmed for either 100% or 50% duty cycle. The AY-5-1315 may be operated alone or in conjunction with the AY-5-1317A chord generator.

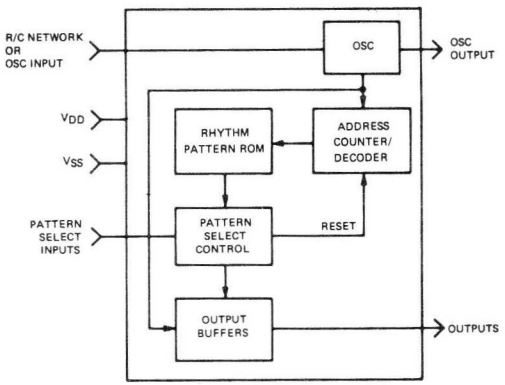
PIN CONFIGURATION

18 LEAD DUAL IN LINE

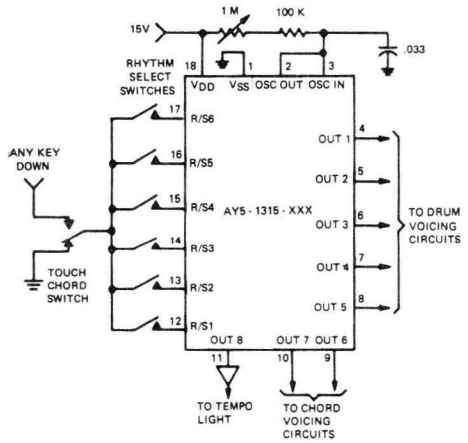


A separate publication, "AY-5-1315 Custom Coding Information", available from GI Sales Offices, describes the punched card and truth table format for custom programming of the AY-5-1315 memory.

BLOCK DIAGRAM



TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} .....-20V to +0.3V
Storage Temperature .....-65°C to +150°C
Operating Temperature (T_A) .....-25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = 0 Volts, V_{DD} = -12 to -18 V

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input					
Freq.	DC	100/1000	100k	Hz	with ÷32 circuit in
	DC	3/300	100k	Hz	with no ÷32 circuit
Logic '0'	V_{DD}-4.0	—	V_{DD}	V	
Logic '1'	+0.3	—	-1.0	V	
Internal osc. freq.	—	100/1000	—	Hz	Set by external resistor & capacitor
Rhythm select inputs					
Logic '0'	V_{DD}-4	—	V_{DD}	V	
Rhythm select inputs					
Logic '1'	+0.3	—	-1.0	V	
Rhythm select input					
Impedance	10	—	—	kΩ	Pulled to V_{DD}
Instrument & osc. output					
Logic '0' (Note 1)	V_{DD}-6.0	—	V_{DD}-4.0	V	with internal pull ups to V_{DD} (instrument outputs only) supplying 0.1 mA
Instrument & osc. output					
Logic '1'	—	—	-1.0	V	Sinking 1.0 mA
Power	—	—	300	mW	V_{DD} = 15 volts

**Typical values are at +25°C and nominal voltages.

NOTE: 1. Open ended devices have a minimum impedance of 500K to GND when in the off condition.

OPERATION

The AY-5-1315 Rhythm Generator contains an internal oscillator a clock generator circuit, a 5-bit synchronous resetable counter/decoder, and a ROM that drives 8 instruments and the reset circuit. By selecting one of the 6 available rhythm patterns, the appropriate section of the ROM is enabled.

If no pattern is selected the reset circuit is activated which stops the internal oscillator, inhibits the output drivers and resets the counter to count 1. When a selection is made, the outputs are enabled which brings out the program as stored in count 1- the down beat program.

The oscillator frequency determines the tempo of the rhythm pattern generated. The clock generator generates a 2 phase clock $\phi 1$ and $\phi 2$. If the internal divide by 32 option is selected $\phi 1$ is on for the first 16 count and $\phi 2$ is on between count 17 and 32, thus producing two non overlapping clocks. If the divide by 32 circuit is programmed out, the circuit $\phi 1$ and $\phi 2$ will be directly related to the ON (logic 1) and OFF (logic 0) time at the clock generator input as provided by an external oscillator. The $\phi 2$ clock drives the 5 bit counter/decoder which sequentially turns on one of the 32 lines of the ROM.

On the $\phi 1$ clock, the program out of the ROM is transferred to the output thus eliminating decoding spikes at the output. If the output of the ROM is a '1' the proper instrument will be turned on. The output drivers are programmed either for 100% duty cycle or 50% duty cycle. When programmed for 100% duty cycle the output turned on will remain on for an entire $\phi 1/\phi 2$ cycle. If the next bit in the program is a '1' again, the output will remain on for the next cycle without going to zero between cycles. When programmed for 50% duty cycle the output will be on during $\phi 1$ only and return to zero during $\phi 2$.

CONSUMER

Chord Generator

FEATURES

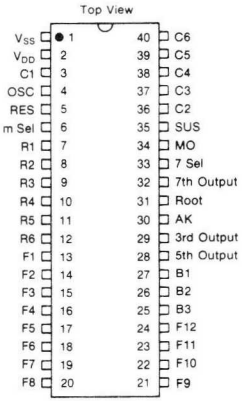
- ROOT, 3rd, 5th, 7th Chord Elements
- Additional output for special effects
- Sustain capability
- Top key priority
- Self-contained oscillator circuit
- Operated with single pole, single throw switch matrix

DESCRIPTION

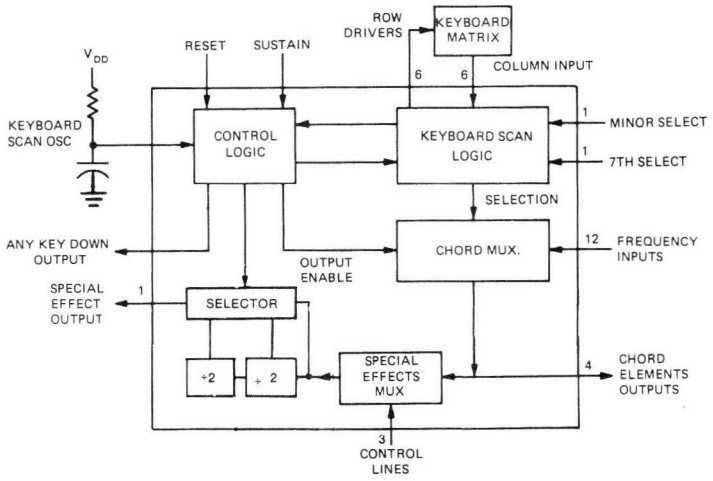
The AY-5-1317A is a P-Channel MOS IC which accepts twelve basic frequencies (one full octave) and outputs the notes necessary to form Major, Minor and Seventh chords. This is the only known standard chord generator IC that performs these functions. The chord elements (ROOT, 3rd, 4th, 5th, 6th, and 7th) can be multiplexed internally to perform special effects such as walking bass, rhythm arpegio, alternating bass, etc. The AY-5-1317A will operate in conjunction with and, through the KEY DOWN output, synchronize a rhythm generator such as the General Instrument AY-5-1315. The AY-5-1317A has a keyboard priority system with the C Major chord having the highest priority.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	Ground (Vss)	Ground
2	Power Supply (V_{DD})	Negative Supply
3, 36-40	Column Inputs (CI-C6)	Column inputs from Keyboard Matrix
4	Oscillator Input (OSC)	R/C network connection for keyboard scan oscillator
5	Reset (RES)	A logic '1' (ground) will reset the keyboard scanner, and the memorized key
6	Minor Select (m Sel)	A Ground on this line changes the 3rd output from Major to Minor
7-12	Row Outputs (R1-R6)	Row outputs to Keyboard Matrix
13-24	Frequency Inputs (F1-F12)	These are the input lines for the 12 frequencies (one full octave B thru C) used to generate the chords.
25-27	Control Inputs (B3-B1)	These 3 lines will be internally latched and decoded to select either the ROOT, 3rd, 4th, 5th, 6th, or 7th frequency as the special effect output.
28	5th Output (5th)	This line will output the 5th frequency element of the selected chord.
29	3rd Output (3rd)	This line will output the 3rd frequency element of the selected chord. Minor 3rd will be provided if a Minor chord is selected. Major 3rd will be provided if a Major or 7th chord is selected.
30	Any Key Down (AK)	This line goes to a logic '1' whenever a chord selection key is depressed.
31	Root Output (Root)	This line will output the ROOT frequency element of the selected chord.
32	7th Output (7th)	This line will output the 7th frequency element of the selected chord if a 7th chord is selected otherwise the output is logic '0' (voltage).
33	7th Select (7 Sel)	A ground on this line turns the 7th output on.
34	Special Effect Output (MO)	This line will output one of the six frequency elements as programmed by the control lines B1-B3. The 7th chord element frequency will be provided independently of the chord selection.
35	Sustain (SUS)	A logic '1' on this line will activate the memory circuit which memorizes the last key played.

B1	B2	B3	Selection
0	0	0	No change from last selection.
0	0	1	ROOT
0	1	0	5th
0	1	1	3rd
1	1	1	7th
1	1	0	4th
1	0	1	6th

TRUTH TABLE FOR SPECIAL EFFECT OUTPUT

FREQUENCY OUTPUTS

Chord Selection	Root	3rd Minor	3rd Major	4th	5th	6th	7th
C	C (÷2)	D# (÷2)	E (÷2)	F (÷2)	G (÷2)	A (÷2)	A# (÷2)
C#	C# (÷2)	E (÷2)	F (÷2)	F# (÷2)	G# (÷2)	A# (÷2)	B (÷2)
D	D (÷2)	F (÷2)	F# (÷2)	G (÷2)	A (÷2)	B (÷2)	C (÷1)
D#	D# (÷2)	F# (÷2)	G (÷2)	G# (÷2)	A# (÷2)	C (÷1)	C# (÷1)
E	E (÷2)	G (÷2)	G# (÷2)	A (÷2)	B (÷2)	C# (÷1)	D (÷1)
F	F (÷2)	G# (÷2)	A (÷2)	A# (÷2)	C (÷1)	D (÷1)	D# (÷1)
F#	F# (÷4)	A (÷4)	A# (÷4)	B (÷4)	C# (÷2)	D# (÷2)	E (÷2)
G	G (÷4)	A# (÷4)	B (÷4)	C (÷2)	D (÷2)	E (÷2)	F (÷2)
G#	G# (÷4)	B (÷4)	C (÷2)	C# (÷2)	D# (÷2)	F (÷2)	F# (÷2)
A	A (÷4)	C (÷2)	C# (÷2)	D (÷2)	E (÷2)	F# (÷2)	G (÷2)
A#	A# (÷4)	C# (÷2)	D (÷2)	D# (÷2)	F (÷2)	G (÷2)	G# (÷2)
B	B (÷4)	D (÷2)	D# (÷2)	E (÷2)	F# (÷2)	G# (÷2)	A (÷2)

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} with respect to V_{SS} . . . . . −20V to +0.3V
Logic Input Voltages with respect to V_{SS} . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied —operating ranges are specified below.

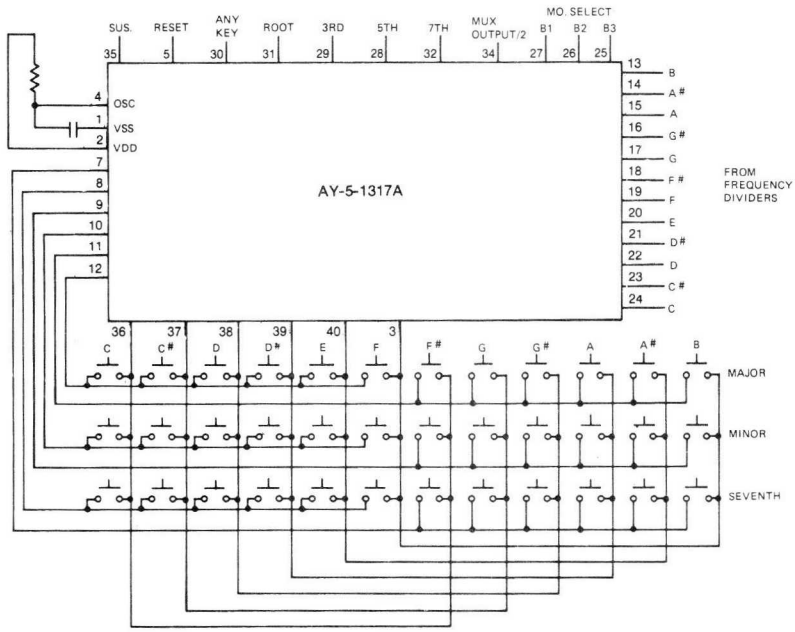
Standard Conditions (unless otherwise noted)

$V_{DD} = -15V \pm 3V$
$V_{SS} = 0V$ (substrate voltage)
Operating Temperature (T_A) = +25°C

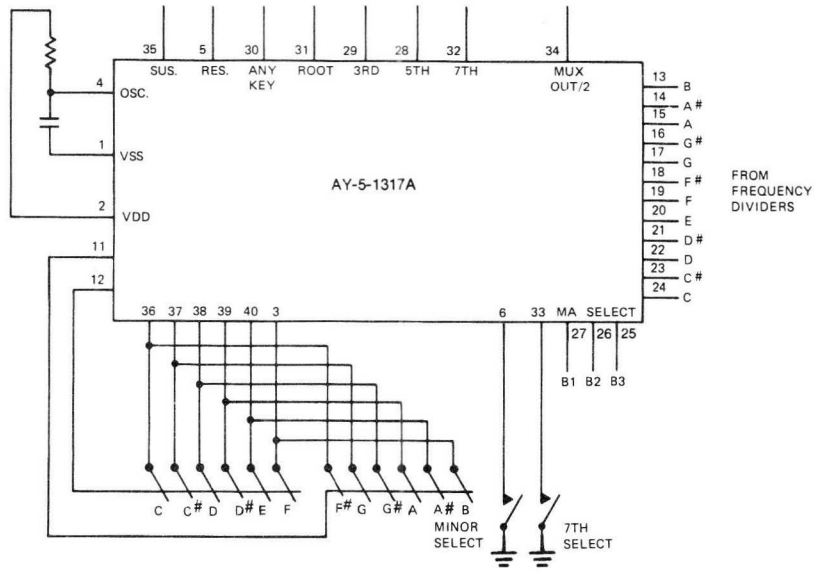
Characteristic	Sym	Min	Typ**	Max	Conditions
Input Logic Levels					
Logic 0	VIL	V_{DD}	—	−8.5V	
Logic 1	VIH	−1.0V	—	+0.3V	
Input Capacitance	CIN	—	—	10 pF	
Note Outputs					
Logic 0	R_{OFF}	160kΩ	—	—	
Logic 1	R_{ON}	—	—	500Ω	
Row Drivers Output Impedance		—	750Ω	—	$V_{DD} = -15V$
Control Input		10kΩ	—	1000kΩ	
Keyboard Row Input Impedance		24kΩ	—	100kΩ	
Keyboard Scan Frequency		—	25kHz	—	500 pF,750K,$V_{DD} = -15V$

**Typical values are at +25°C and nominal voltages.

STANDARD INTERCONNECTION FOR A 3×12 KEY MATRIX



STANDARD INTERCONNECTION FOR A SINGLE ROW KEYBOARD WITH SEPARATE KEY FOR MINOR AND SEVENTH



Piano Keyboard Circuit

FEATURES

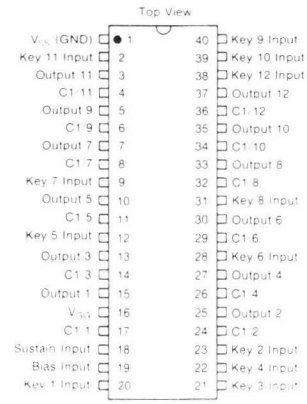
- 12 keys per package
- Loudness proportional to key press velocity
- Sustain input to give loud pedal operation

DESCRIPTION

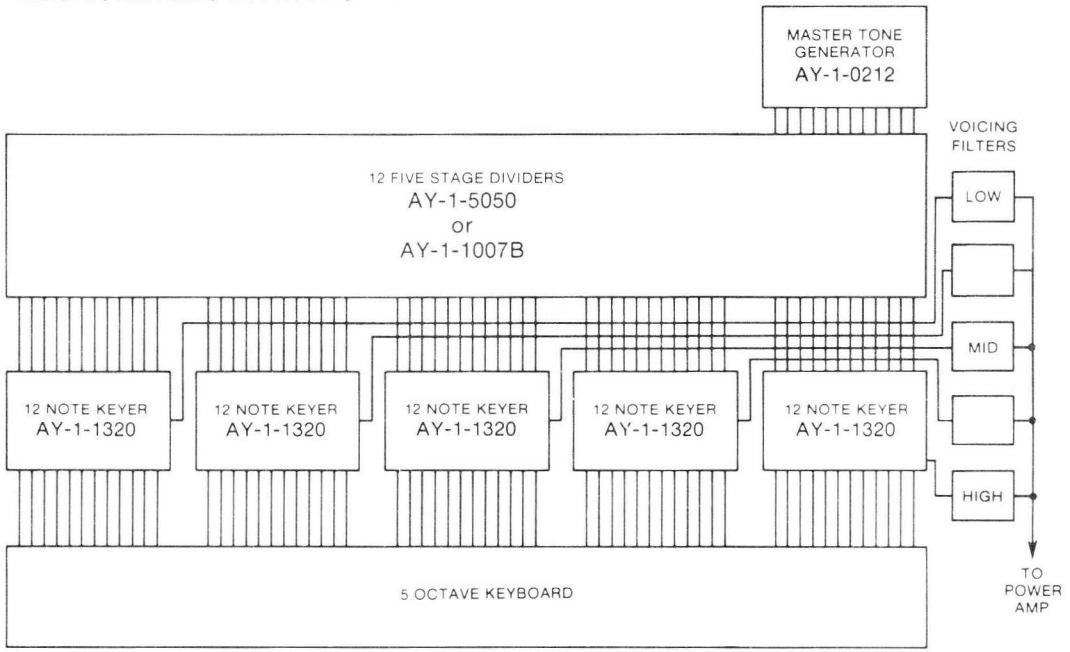
The electronic piano chip when used in conjunction with standard divider circuits will make an instrument closely resembling a piano in operation and sound. The chip is arranged so that the loudness of the notes is proportional to the velocity of the keys as in an acoustical instrument. Additionally the notes are arranged to die away at a realistic rate. A sustain input is provided so that the operation of the loud pedal can be emulated.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



ELECTRONIC PIANO BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
V_{SS}	Positive supply
V_{GG}	Negative supply (-25 to -29V)
$V_{BIAS\ 1}$	Bias supply to keying circuit (-27V nominal)
Sustain	When a logic '1' the outputs are damped with a time constant of 180msec. when the key is released. This input simulates the action of the loud pedal in a piano.
Key Inputs (1-12)	These inputs are switched from logic '0' to logic '1' by a break before make change over switch. During the transit the input is held at an intermediate logic level. The transit time determines the initial output level.
C1 (1-12)	The capacitor C1 connected to this pin establishes the key velocity time constant. 0.5μF gives a time constant of 18msec.
Output (1-12)	This output provides an exponentially decaying DC level proportional to the amplitude of the desired note. The capacitor C2 determines the damper time constant. The resistor R1 together with C2 determines the undamped decay time constant. The DC level is chopped by external frequency dividers to generate the note.

OPERATION

In the rest condition with the key up capacitor C1 is charged to -12 Volts. When the key is depressed C1 is first disconnected and it starts to discharge through the 39K resistor with a time constant of 18msec. And the end of the key travel the final voltage on C1 is transferred to the gate of T3 via T2. This causes C2 to be charged to V_{C1} + 4 Volts. The faster the key depression the larger the initial voltage on C2 and the louder the note.

The DC voltage on C2 is chopped via R1 and the divider circuit and the resulting square wave is fed to the voicing circuits and amplifiers. C2 slowly discharges through R1 to give the required exponential decay of note amplitude. When the key is released the 50K damping resistor is optionally connected across C2 to damp the notes with a 110msec. time constant.

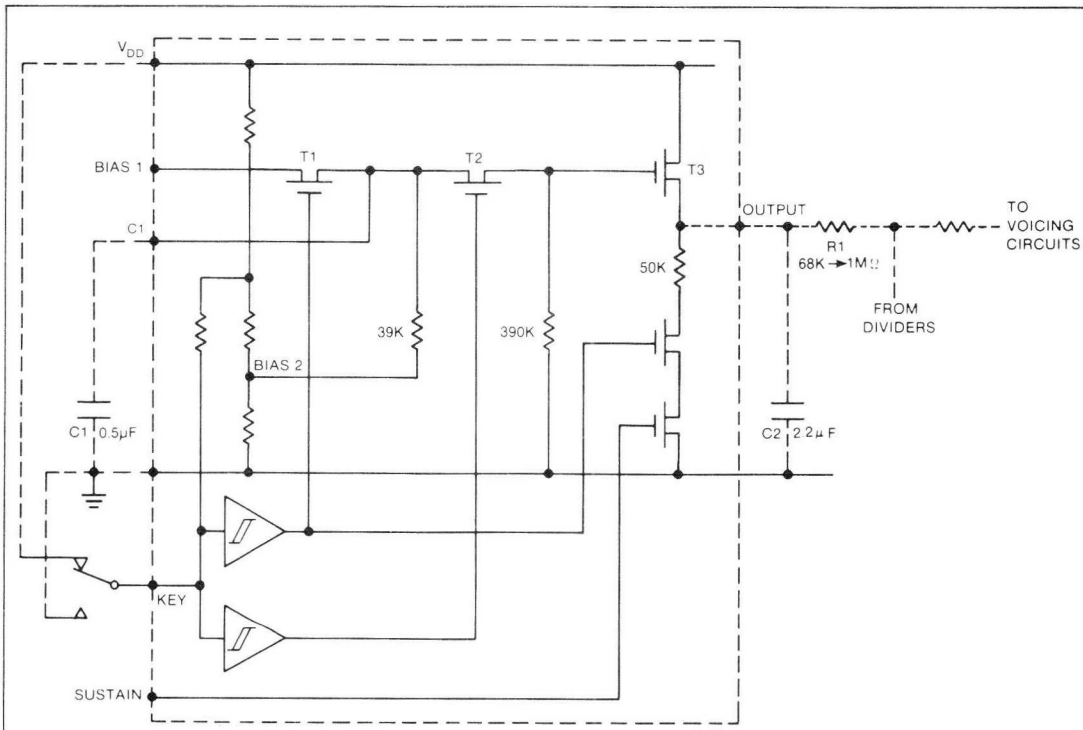


Fig.1 KEY CIRCUIT SCHEMATIC

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -30 Volts
Storage Temperature Range ..... -65°C to +150°C
Ambient Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = -25 to -29 Volts
V_{SS} = 0V
$V_{BIAS\ 1} = V_{GG}$
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Min.	Typ**	Max	Units	Conditions
Key Input Logic '1'	-24	—	-29	Volts	Key up
Key Input Logic '0'	+0.3	—	-1	Volts	Key down
Key velocity time constant	—	18	—	ms	C1 = 0.5μF (Note 1)
Output peak amplitude	—	8	—	Volts p-p	(Note 2)
Output decay time constant	—	286-2486	—	ms	See Table 1
Damper time constant	—	110	—	ms	C2 = 2.2μF
Dynamic range	—	30	—	dB	
Power Supply Current I_{GG}	—	3	—	mA	
Power Supply Current I_{BIAS}	—	3	—	mA	

**Typical values are at +25°C and nominal voltages.

Note 1. The key transit time determines the initial amplitude of the note. The longer the time the softer the note. If the transit time is 18ms the amplitude will be approximately 37% of maximum. Capacitor C1 determines the time constant.

Note 2. This is the amplitude that would be obtained if the key transit time was zero.

Table 1 — TYPICAL COMPONENT VALUES/DECAY TIME
C2 = 2.2 μF Square wave chopper

Octave	R1 kΩ	R2 kΩ	Decay Time msec.
C7-C6# 2093-1108Hz	68	470	286
C6-C5# 1046.4-554.2Hz	120	470	484
C5-C4# 523.2-277.1Hz	220	470	825
C4-C3# 261.6-138.6Hz	330	470	1155
C3-C2# 130.8-69.3Hz	680	470	1980
C2-C1# 65.4-43.6Hz	1000	470	2486

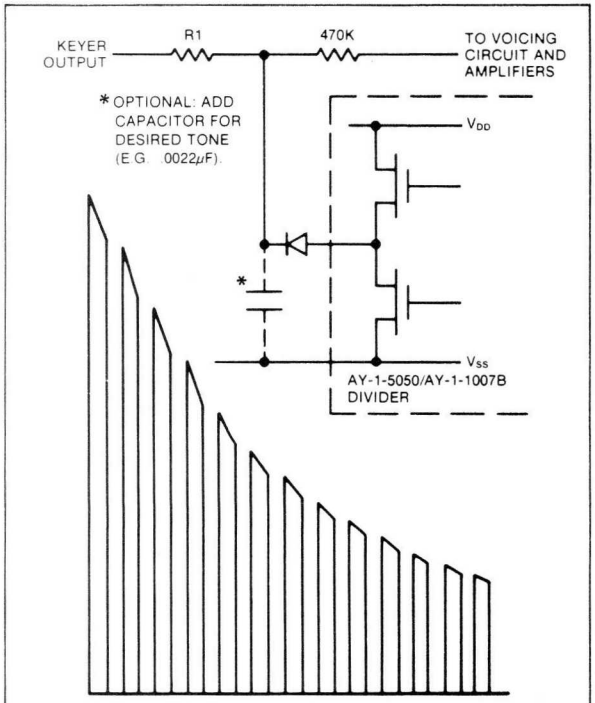


Fig.2 OUTPUT CIRCUIT AND WAVEFORMS

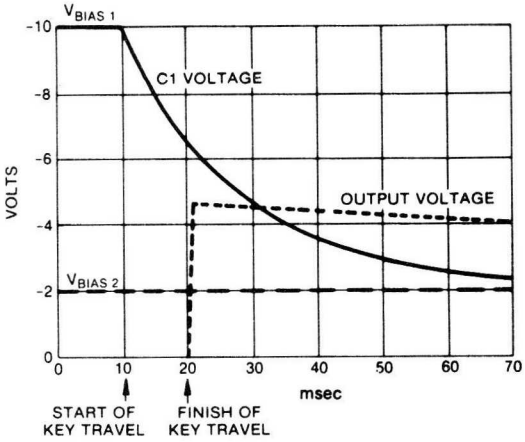


Fig.3 KEY VELOCITY WAVEFORMS

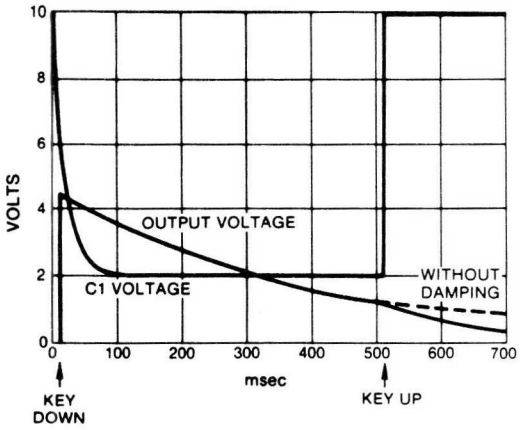


Fig.4 OUTPUT ENVELOPE DECAY WAVEFORM

4-5-6-7 Stage Frequency Dividers

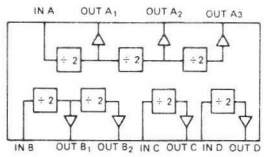
FEATURES

- DC to 1 MHz operating frequency range.
- Diode protection on all inputs.
- Low output impedance in both states.
- Choice of configurations:
  1) AY-1-5050: 7-Stage Frequency Divider, 3+2+1+1
  2) AY-1-5051: 4-Stage Frequency Divider, 2+1+1
  3) AY-1-6721/5: 5-Stage Frequency Divider, 3+2
  4) AY-1-6721/6: 6-Stage Frequency Divider, 3+2+1

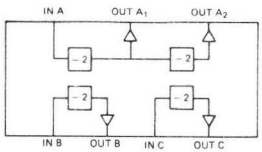
DESCRIPTION

The AY-1-5050, AY-1-5051, AY-1-6721/5 and the AY-1-6721/6 are constructed on monolithic silicon chips using MTOS (Metal-Thick-Oxide-Silicon) P-Channel Enhancement Mode Field Effect Transistors. All circuits can be driven from a sine or square wave input. The different types all have the same specifications and are fully compatible with one another.

BLOCK DIAGRAMS



AY-1-5050



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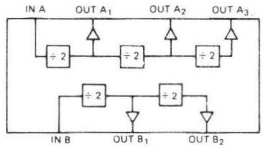
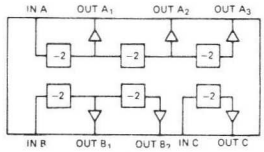


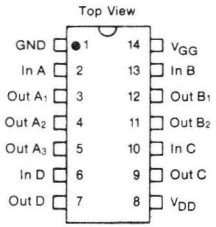
AY-1-6721/5



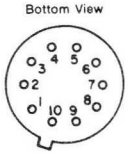
AY-1-6721/6

PIN CONFIGURATIONS

14 LEAD DUAL IN LINE
AY-1-5050

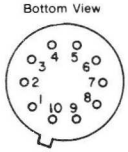


10 LEAD
AY-1-5051



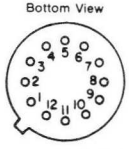
1	Out A_1	6	In C
2	Out A_2	7	Out C
3	In B	8	V_{GG}
4	Out B	9	V_{DD}
5	GND	10	In A

10 LEAD
AY-1-6721/5



1	GND	6	In A
2	Out B_2	7	Out A_1
3	Out B_1	8	Out A_2
4	In B	9	Out A_3
5	V_{GG}	10	V_{DD}

12 LEAD
AY-1-6721/6



1	GND	7	Out C
2	In A	8	V_{DD}
3	Out A_1	9	Out B_2
4	Out A_2	10	Out B_1
5	Out A_3	11	In B
6	In C	12	V_{GG}

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Drain Voltage	−30V to +0.3V
Gate Voltage	−30V to +0.3V
Data Input Voltage	−30V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

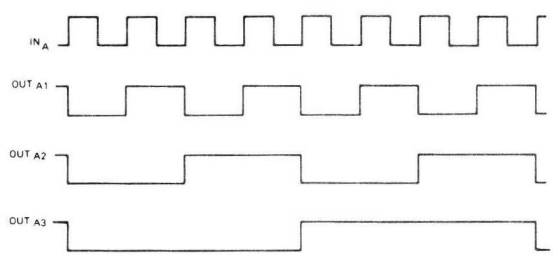
$V_{DD} = -13V \pm 1V$ $C_L = 10$ pF
$V_{GG} = -27V \pm 1V$ Operating Temperature (T_A) = +25°C
$R_L = 1M\Omega$

Characteristics	Min.	Typ**	Max	Units	Conditions
Data Input					
Logic "0" level	—	—	−2	V	
Logic "1" level	−10	—	—	V	
Data Input operating freq.	DC	—	1	MHz	Sine or square wave
Data Input Pulse width					
— "0" level	300	—	—	ns	
— "1" level	300	—	—	ns	
Input Leakage	—	—	5	μA	$V_{in} = -20VDC$
Output Parameters					
Logic "0" level	—	—	−1	V	
Logic "1" level	−11	—	—	V	
Drive Capability					
— "0" level	—	−1	−1.5	V	Sinking current = 0.5 mA
— "1" level	−11	—	—	V	$R_L = 100$ KΩ
— "1" level	−8	—	—	V	$R_L = 10$ KΩ
Data output Rise and Fall time	—	0.6	—	μs	
Current Drain					
I_{GG}	—	3	—	mA	$V_{GG} = -27$ V
I_{DD}	—	***	—		

**Typical values are at +25°C and nominal voltages.

*** V_{DD} is only used for the push-pull outputs therefore I_{DD} is equal to the sum of load currents. This separate V_{DD} enables tremulant to be introduced in the electronic organ application.

TIMING DIAGRAM



CONSUMER

MICRO ELECTRONICS

APPLIANCES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
CLOCK / TIMERS	24 hour programmable, repeatable on/off time switch with 4 digit clock.	AY-5-1230	8-70
		AY-5-1231	8-70
		AY-5-1232	8-70
		AY-5-1233	8-70
OVEN / COOKER TIMERS	Appliance timers with clock. Full control of "start" time, "stop" time, or "duration."	AY-3-1250	8-74
		AY-3-1251	8-74
MICROWAVE OVEN TIMER	Three mode magnetron control, timer and 4 digit clock.	AY-5-1260	8-80
DIGITAL THERMOMETER	Deep-freeze thermometer, -40° C to 0° C.	AY-3-1270	8-82
COINBOX MEMORY	Memory/credit accumulator for coin-operated equipment.	AY-1-8622	8-85
VIDEO TAPE TIMER	Program "start" time for 2/4 hour video tape recorders.	VTR 3300	8-90

Clock / Timers

FEATURES

- 4 Digit Clock.
- Drives 7 segment Fluorescent Displays.
- Programmable switch on and switch off times.
- Repeating or non-repeating operation.
- Dimming control.
- Power on reset, remains reset until time is set.
- Foolproof switch on/off setting, if switch off time not programmed output stays on for 10 minutes only.
- Non-multiplexed set inputs for low radiated noise.
- Indication of set alarm state.
- AY-5-1230/1232/1233: 50Hz Input, 24 hour operation.
- AY-5-1231: 50/60Hz input, 12/24 hour operation.

DESCRIPTION

The AY-5-1230 Series Clock/Timers are circuits designed to provide a four digit clock display and automatic on/off switching of a TV or other appliance at any desired time. A typical application would be the use of an AY-5-1230 Series circuit with GI's AY-5-8320 TV Time/Channel Display circuit to provide a clock display and automatic on and off switching of the TV at any desired time.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

AY-5-1230/1232/1233

Top View

V_{SS} (GND)	1	28	Inhibit Input (Set/Run on AY-5-1232)
Set ON Time/Set OFF Time	2	27	BCD/7 Segment
Repeat Input	3	26	V_{DD}
Set ON Output	4	25	Cancel Input (Reset on AY-5-1233)
Set OFF Output	5	24	ON/OFF Input
Clock Input	6	23	Multiplex Oscillator
Set Hours Input	7	22	Switch Output
Set Minutes Input	8	21	MX 1 Output
V_{LL} (Display Supply)	9	20	MX 2 Output
Seg. G Output	10	19	MX 3 Output
Seg. F Output	11	18	MX 4 Output
Seg. E Output/Strobe Out	12	17	Colon Output
Seg. D Output/2^0 Out	13	16	Seg. A Output/2^3 Out
Seg. C Output/2^1 Out	14	15	Seg. B Output/2^2 Out

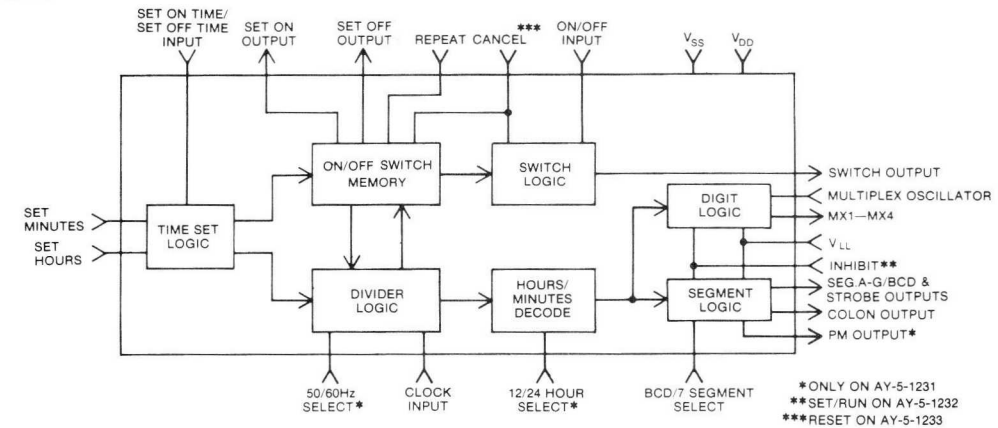
40 LEAD DUAL IN LINE

AY-5-1231

Top View

V_{SS} (GND)	1	40	Inhibit Input
12/24 Hour Select Input	2	39	Set/Run Input
Set ON time/Set OFF time input	3	38	BCD/7 Segment Input
Repeat input	4	37	V_{DD}
On Set Output	5	36	N.C.
Off Set Output	6	35	Cancel Input
N.C.	7	34	Reset Input
N.C.	8	33	ON/OFF Input
N.C.	9	32	Multiplex Oscillator
50/60Hz Select Input	10	31	Switch Output
Clock Input	11	30	N.C.
Set Hours Input	12	29	PM Output
Set Minutes Input	13	28	MX 1 Output
V_{LL} (Display Supply)	14	27	MX 2 Output
Segment G Output	15	26	N.C.
Segment F Output	16	25	N.C.
Segment E Output/Strobe Out	17	24	MX 3 Output
Segment D Output/2^0 Out	18	23	MX 4 Output
Segment C Output/2^1 Out	19	22	Colon Output
Segment B Output/2^2 Out	20	21	Segment A Output/2^3 Out

BLOCK DIAGRAM



PIN FUNCTIONS

AY-5-1230 Pin. No.	AY-5-1231 Pin No.	AY-5-1232 Pin No.	AY-5-1233 Pin No.	Name	Function
1.	1.	1.	1.	V_{SS}	Positive Supply
2.	3.	2.	2.	Set ON time/ Set OFF time Input	When taken to logic '0' the ON time is displayed and the Set hours and Set minutes inputs operate the ON time counter. When taken to logic '1' the OFF time is displayed and the Set hours and Set minutes inputs operate the OFF time counter. When left open circuit the time is displayed. When either Set ON or Set OFF is activated the Switch logic is set and the switch output will operate at the set times.
3.	4.	3.	3.	Repeat Input	When connected to logic '0' the Switch output comes on every 24 hours. When left open circuit the Switch output comes on only once after which the Switch logic is reset. The switch logic can be set again by pressing Set ON and Set OFF.
4.	5.	4.	4.	Set ON Output	This output goes to logic '0' when an ON time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
5.	6.	5.	5.	Set OFF Output	This output goes to logic '0' when an OFF time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
6.	11.	6.	6.	Clock Input	The timing clock is input to this pin. Hysterisis is provided so that the input waveform is not critical.
7.	12.	7.	7.	Set Hours Input	When this input is taken to logic '0' the hours counter is advanced twice per second.
8.	13.	8.	8.	Set Minutes Input	When this input is taken to logic '0' the minutes counter is advanced twice per second. During setting the minutes counter does not overflow into the hours counter.
9.	14.	9.	9.	V_{LL} (Display Supply)	The on chip pull down resistors provided for each high voltage output are connected to this pin. When driving fluorescent display this pin is connected to -32 Volts.
10-16	15-21	10-16	10-16	7 Segment Outputs	High voltage outputs capable of driving fluorescent displays directly. At logic '0' to display. They have on-chip pull down resistors to V_{LL}.
13-16	18-21	13-16	13-16	BCD Outputs	In the BCD mode the time data is output on these pins.
17.	22.	17.	17.	Colon Output	This high voltage output is enabled on MX3 time and flashes once per second.
18-21	23,24 27,28	18-21	18-21	MX4-MX1 Outputs	These outputs are switched to logic '0' successively to select the digits, MX4 is 10s hours, MX1 is units mins. There are 5 time slots the fifth being blank. These outputs are high voltage and have on-chip pull down resistors to V_{LL}.
22.	31.	22.	22.	Switch Output	This output goes to logic '0' when the ON time is reached and returns to logic '1' when the OFF time is reached. If an OFF time has not been programmed the output will return to logic '1' ten minutes after the ON time has been reached. The output will sink 30mA.
23.	32.	23.	23.	Multiplex Oscillator	Not used normally. An external capacitor can be connected to reduce the mux frequency, or an external clock can be applied if required.
24.	33.	24.	24.	ON/OFF Input	When this input is taken to logic '0' the switch output is alternately turned ON and OFF. This input has antibounce logic to prevent maloperation.
25.	35	25.	—	Cancel Input	When this input is taken to logic '0' the Switch logic is reset and the Switch output turned off.
26.	37.	26.	26.	V_{DD}	Negative supply 15V nom. (11-19V)
27.	38.	27.	27.	BCD/7 Segment Select	When this input is wired to logic '0' BCD operation results.
28.	40.	—	—	Inhibit Input	When this input is taken to logic '0' display outputs are switched off. This input can be used for display dimming.
—	2.	—	—	12/24 Hour Select	When connected to V_{SS} selects 12 hour operation.
—	10	—	—	50/60Hz Select	When connected to V_{SS} selects 60Hz operation.
—	29.	—	—	PM Output	This output is on during the PM period. It is a high voltage output enabled at MX4 time slot.
—	39	28.	—	Set/Run Input	When taken to logic '1', the clock is stopped and the seconds counter is reset to zero.
—	34	—	25	Reset Input	When taken to logic '0', this input resets either the clock, the "on" time, or the "off" time, depending on the state of the Set ON and Set OFF inputs.

NOTE:
1. All inputs have a pull down resistor to V_{DD}.
2. At power-on the chip is reset but the clock does not start to count until either the set hours or set minutes button has been pressed.

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin (except display pins) with respect to V_{SS} pin . . . . . +0.3 to −20V
Voltage on display pins with respect to V_{SS} pin . . . . . +0.3 to −35V
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range . . . . . −55°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = OV
V_{DD} = −11 to −19V
V_{LL} = −31 to −33V
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	50/60	—	Hz	50Hz only on AY-5-1230/1232/1233.
Logic '0'	+0.5	—	−2	Volts	Note 1
Logic '1'	-10	—	−19	Volts	
Multiplex Clock Frequency	—	100	—	kHz	Note 2
Control Inputs					
Logic '0'	+0.3	—	−1.5	Volts	
Logic '1'	−6	—	−19	Volts	
Pull Up Resistance	—	200	—	KΩ	to V_{DD}
Segment Output					
Logic '0'	—	—	−2	Volts	Iout = 2mA
Logic '1'	—	—	10	μA	V_{OUT} = −35V
Mx Outputs					
Logic '0'	—	—	−2	Volts	Iout = 5mA
Logic '1'	—	—	10	μA	V_{OUT} = −35V
Pull Up Resistance	—	200	—	KΩ	to V_{LL}
Switch Output					
Logic '0'	—	—	−2	Volts	I_{OUT} = 30mA
Logic '1'	—	—	10	μA	V_{OUT} = −19V
Set ON, OFF Outputs:					
Logic '0'	—	—	−2	Volts	I_{OUT} =2mA
Logic '1'	—	—	10	μA	V_{OUT} = −19V
Power Supply Current	—	6	13	mA	V_{DD} = −11V
	—	8	17	mA	V_{DD} = −19V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. The clock input may be taken positive provided that the current is limited to 100μA
2. This results in a multiplex rate of 5kHz.

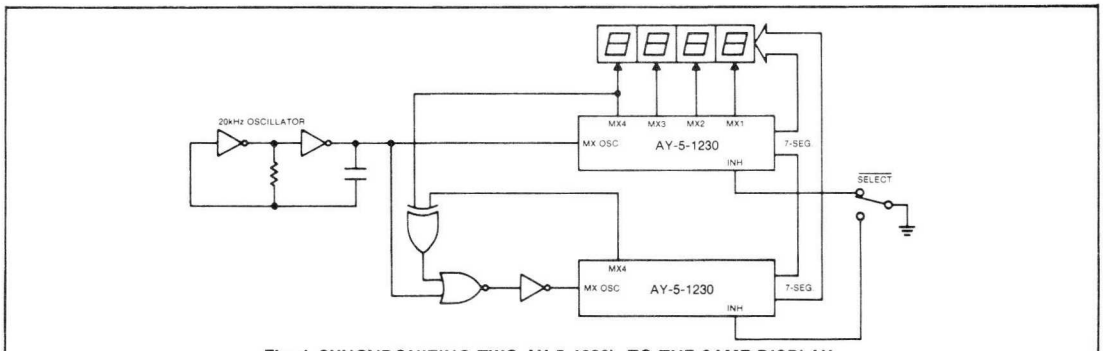


Fig. 1 SYNCHRONIZING TWO AY-5-1230's TO THE SAME DISPLAY

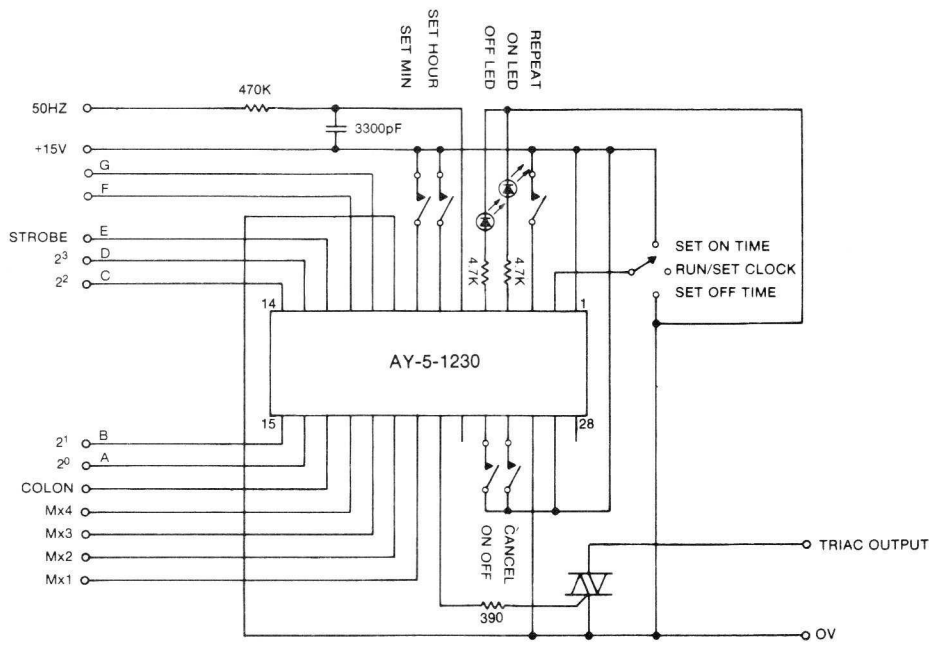


Fig. 2 AY-5-1230 CONNECTION DIAGRAM

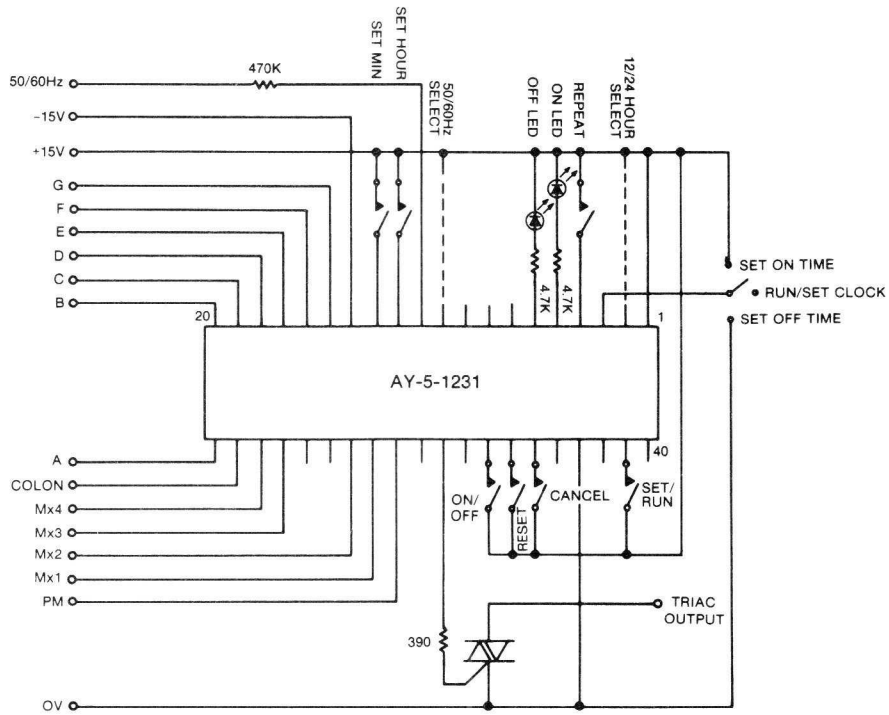


Fig. 3 AY-5-1231 CONNECTION DIAGRAM

CONSUMER

Oven / Cooker Timers

FEATURES

- 4 digit time display
- 7 segment outputs
- Programmable on and off times for 3 outputs
- Cook duration and/or on-time/off-time entry
- 3 digit minute minder
- Audio tone generated at minute minder time-out
- Standby oscillator
- Indication of power failure
- Indication of auto/manual for each timer
- 12/24 hour operation — bonding option
- AM/PM indicator
- Colon output
- 50/60Hz operation — bonding option
- Manual override of programmable outputs
- 3 digit temperature setting for outputs 1 and 2
- Interfaces with fluorescent display direct drive chip.

ADDITIONAL AY-3-1250 FEATURES

- 4 digit display for all functions, i.e. time, programmed on/off times, minute minder, temperature, 7×4 matrix keyboard.
- Incremental setting of hours, minutes and temperature.

ADDITIONAL AY-3-1251 FEATURES

- 14 digit display
  4 digits — time and programmed on/off times
  3 digits — minute minder
  3 digits — oven 1 temperature
  4 digits — hotplate temperature settings.
- 4 outputs with variable ratio for control of hotplate duty cycle.
- Direct keyboard entry of all numbers
- 10×4 matrix keyboard

DESCRIPTION

The AY-3-1250 and AY-3-1251 are designed to be incorporated in domestic cookers/stoves. In addition to the three timing functions for automatic cooking each circuit includes a count-down timer (Minute Minder). Control of an oven temperature for 2 of the outputs is also provided.

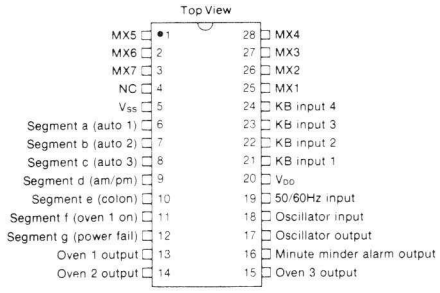
Both clocks and automatic timer controls can use 12 or 24 hour systems, but when in the 12 hour mode a P.M. key is provided to enable the controls to be set more than 12 hours ahead.

INTRODUCTION

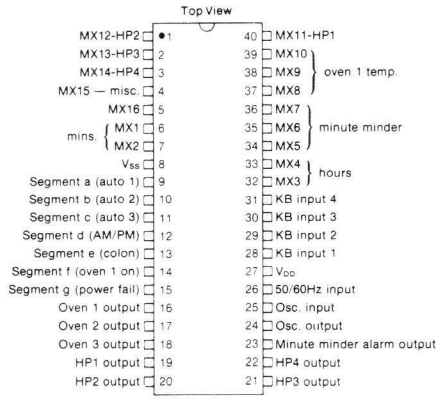
The AY-3-1250 and AY-3-1251 designs consist of a central processing unit with on-chip ROM program and various blocks of mask programmable logic for system interfacing.

PIN CONFIGURATION

28 LEAD DUAL IN LINE
AY-3-1250



40 LEAD DUAL IN LINE
AY-3-1251



AY-3-1250 PIN FUNCTIONS

Pin No.	Name	Function
25-28, 1-3	MX1-MX7	These outputs are successively taken to logic '0' to strobe a matrix keyboard. MX1-MX5 also act as display digit strobes: MX1 — units of minutes MX4 — tens of hours MX5 — status lights.
5	V_{SS}	Negative supply.
6-12	Segment a-g	At logic '0' to display. During MX5 these outputs drive miscellaneous indicator lamps.
13-15	Oven 1-3 Outputs	These outputs are switched to logic '0' when the respective on-time is reached and returned to logic '1' when the off-time is reached. Oven outputs 1 and 2 can also produce a variable duty cycle output for temperature control.
16	MM audio	A 1kHz output modulated at 1Hz appears on this pin when the minute minder has timed out. The output is cancelled on receipt of the appropriate keyboard command.
17	Osc output	A resistor is connected across these pins to define multiplex frequency. During a power failure this is used as a standby frequency source.
18	Osc input	
19	50/60Hz input	Clock timing is derived from this input. Hysteresis is provided to eliminate the effect of power transients etc.
20	V_{DD}	Positive supply
21-24	KB1-KB4	Keyboard inputs.

AY-3-1251 PIN FUNCTIONS

Pin No.	Name	Function
32-40, 1-7	MX1-MX16	At logic '0' to select digit. These outputs also strobe a matrix keyboard.
8	V_{SS}	Negative supply.
9-15	Segment a-g	At logic '0' to display. During MX15 these outputs drive miscellaneous indicator lamps.
16-18	Oven output 1-3	These outputs are switched to logic '0' when the respective on-time is reached and returned to logic '1' when the off-time is reached. Oven outputs 1 and 2 can also produce a temperature dependent duty cycle output.
19-22	HP1-4	These outputs control the duty cycle of hotplate elements. The mark:space ratio is variable from 0% to 100% by entering the number 0-9 at the keyboard.
23	Minute Minder output	A 1kHz output modulated at 1Hz is output on this pin when the minute minder has timed out. The output is cancelled on receipt of the appropriate keyboard command.
24	Osc. output	A resistor is connected across these pins to define multiplex frequency. During a mains failure this is used as a standby frequency source.
25	Osc. input	
26	50/60Hz input	Clock timing is derived from this pin. Hysteresis is provided to eliminate the effect of mains transients etc.
27	V_{DD}	Positive supply.
28-31	KB1-4	Keyboard inputs.

KEYBOARD ALLOCATION
AY-3-1250

	KB1	KB2	KB3	KB4
MX1	Hrs up	Hrs down	Mins up	Mins down
MX2	Set time	Clear	Set min	Set 01 temp
MX3	Set on 1	Set off 1	Duration 1	Auto/man 1
MX4	Set on 2	Set off 2	Duration 2	Auto/man 2
MX5	Set on 3	Set off 3	Duration 3	Auto/man 3
MX6	On/off 1	On/off 2	On/off 3	Set 02 temp
MX7		Repeat	Reset	PM

KEYBOARD ALLOCATION
AY-3-1251

	KB1	KB2	KB3	KB4
MX2	Set time	Clear	Set MM	Set 01 temp
MX3	Set on 1	Set off 1	Duration 1	Auto/man 1
MX4	Set on 2	Set off 2	Duration 2	Auto/man 2
MX5	Set on 3	Set off 3	Duration 3	Auto/man 3
MX6	On/off 1	On/off 2	On/off 3	Set 02 temp
MX7		Repeat	Reset	
MX8	0	1	2	3
MX9	4	5	6	7
MX10	8	9	PM	
MX11	HP1	HP2	HP3	HP4

CONSUMER

OPERATION

On initial power-up, all registers are reset to '0' and the display is blank apart from time display which shows 0:00. In the following description certain operations/times are mask programmable to values other than those available in the standard versions (AY-3-1250/1251). These are noted with an asterisk for reference to the notes at the end of this section.

Time Display: AY-3-1251

Following a "Set-Time" instruction the time can be entered directly from the keyboard, commencing with the hours. Digits are entered from the right and overflow on the left. A keyboard entry is accepted within 5 seconds(*1) of the previous entry. After this period (or if another register has been selected) the device checks that the entry is valid. In the event of an invalid entry the display flashes at 1Hz(*2) and the clock fails to start. The clear key deletes the entry and the time register is reset to zero. In the 12 hour mode depression of the "PM" key enables a time to be set over the full 24 hour range. The internal "seconds" register is reset whenever the time register is updated. Thus the next "minutes" change of the clock occurs exactly 60 seconds after the last number entered.

Time Display: AY-3-1250

Following a "Set-Time" instruction the hours and minutes are incremented and decremented independently by the "hrs. up", "hrs. down", "mins. up", and "mins. down" keys. Momentary depression of a key causes a single increment (decrement). Continued depression after 1 sec.(*3) gives an increment (decrement) rate of 5Hz(*4). The internal "seconds" register is reset whenever the time register is updated. Thus the next "minutes" change of the clock occurs exactly 60 seconds after the last increment/decrement command.

Automatic Output Control

(a) SETTING

Three outputs are under automatic control. The input controls associated with each output are "set start time", "set stop time" and "set Cook duration". Programming can be accomplished by any combination of 2 inputs.

On selection of "Set Start Time" or "Set Stop Time" the display shows all zeros or the previous setting if a program is under way. If 00:00 is the required setting then no further entry is required. Otherwise the data is entered in a similar way to the "Set Time" input. If no key is depressed within 5 seconds(*1) the display reverts to a time display. The auto lamp is lit if a start time and cook duration or a stop time have been set.(*5) Thus enables automatic or semi-automatic operation. An invalid entry on the AY-3-1251 causes the display to flash at 1Hz(*2) and the "auto" lamp is not lit. "Set Cook Duration" functions in a similar way. The display flashes(*2) and the auto mode is not selected if cook duration is greater than the period between real time and selected stop time. If a cook program is required with a start time less than 24 hours from the current time and a stop time more than 24 hours from the current time, the program can be entered by the "Set Start Time" and "Set Stop Time" instructions.

Selection of the Cook Duration register during a cooking cycle gives a display of the time remaining till completion.

(b) USE

(i) Fully automatic

The time program is entered and oven temperature selected. When the start time is reached, the appropriate output is activated and the 'ON' lamp is lit (a separate output is provided to drive the 'ON' lamp for oven 1. This ensures that the lamp is lit continuously during the cooking cycle of this temperature controlled output.)

When the stop time is reached the "auto" and "ON" lamps are extinguished, the output is de-activated and the appropriate register reset to 0. The minute minder audio output appears for 10 seconds.

(ii) Semi-automatic

The stop time is entered and the "on/off" switch depressed to turn the appropriate output on. When the stop time is reached, the output is switched off, the "auto" and "on" lamps are extinguished, the stop time register is reset to 0, and the minute minder audio output appears for 10 seconds.

(iii) Manual

An "Auto/Manual" key is provided for each output. Depresssion of this key while in the auto mode extinguishes the "auto" lamp and oven control is by the "on/off" keys only.

Minute Minder: AY-3-1250

Depression of the "minute minder" key displays the controls of the minute minder register. The LH digit is blanked and times of up to 9 hours 59 minutes can be entered via the "set hrs." and "set mins." keys(*6). If a countdown is underway, the time remaining is displayed. Otherwise the display is all zeros.

Minute Minder: AY-3-1251

The minute minder is constantly displayed and, on depression of the "minute minder" key, times of up to 9 hrs. 59 mins.(*6) can be entered directly from the keyboard. An invalid entry causes the minute minder display to flash(*2) and the countdown does not start.

In both versions, the count down begins immediately after the last (valid) keyboard entry. At the completion of the minute minder period the display shows all zeros, the lamp remains lit and the audio tone sounds. The lamp and audio signal are cancelled by depression of the "minute minder" and "clear" keys in turn(*7). In the event of a clear instruction not being input, the lamp and audio alarm are automatically cancelled one minute later.

The minute minder program can be cancelled at any time by depressing the "minute minder" and "clear" keys.

Repeat Mode

In repeat mode the device functions in exactly the same way as described, except that at the end of the program the registers are not reset and the program is repeated 24 hours later.

An indicator lamp shows the status of the repeat mode which can be toggled by depression of the "Repeat" key.

Temperature Control: Oven 1 output

Oven 1 output, as well as being under program control, can also be controlled by temperature settings. The "set temperature" key is depressed and the required temperature entered as a 3 digit number via the keyboard in the AY-3-1251 or by "set hrs." and "set mins." keys in the AY-3-1250. In the latter case, the selected temperature is displayed by the 3 RH display digits. In the AY-3-1251, the temperature is constantly displayed. The "set mins." key increments the units and tens of degrees while the set hrs. key increments the hundreds of degrees. The "clear" key resets the temperature to zero while in "set temperature" mode.

The output is a pulse waveform of frequency 1kHz with a mark/space ratio variable from 0% to 100% in steps of 1/120(*8). The mark/space ratio output depends on the selected temperature, the maximum output corresponding to a temperature setting of 300° C(*8). The display is blank for temperatures below 60° C(*9). While oven 1 is off the output is held at logic 1(*10).

Temperature Control: Oven 2 output

A facility also exists for control of oven 2 temperature in exactly the same way. However, because of pin limitations, special arrangements have to be made for display of oven 2 temperature in the AY-3-1251. The minute minder can be incorporated in the 4 digit time display (mask option) thus releasing 3 digits for oven 2 temperature, or both oven temperatures can be displayed by the oven temperature digits. Alternatively, the device can be interfaced to a fluorescent display driver chip which is capable of driving up to 21 digits directly.

Hotplate Control

This function is available in the AY-3-1251 only. 4 separate outputs and 4 keyboard inputs are used to control the duty cycle of the hotplate elements. To set hotplate "temperature" the appropriate key is depressed to select the hotplate, followed by a keyboard digit 0-9. These heat settings cover the full 0% to 100% range by varying the mark/space ratio of the pulse at the hotplate output. The pulse has a period which is mask programmable up to 32 seconds to conform to BS5406 for various loads. The duty cycle for each setting is mask programmable as a fraction of 63 to enable fine control for simmering.

Override inputs to the matrix keyboard are available to enable pan sensing on one hotplate. The outputs switch to logic '0' (the on-state) on an AC power input zero crossing.

Standby Mode

The multiplex oscillator is also a standby frequency source during a power failure. The oscillator frequency is adjusted to 200kHz by an external resistor. Overall stability is likely to be better than ±5% and may be as low as ±2%.

In the event of a power failure, the chip detects the absence of the 50/60Hz input. Timing is thus achieved by counting the oscillator frequency, and the "power fail" lamp is lit. On re-application of the power, the timing returns to the 50/60Hz input, but the "power fail" lamp remains lit until cancelled by the "reset" input. Hence the chip functions as normal during a power failure except for the loss of time keeping accuracy.

OPTIONS AVAILABLE

The two versions detailed in this specification are the standard push-button devices of the AY-5-1250 series.

However, the AY-3-1250/1251 is a 4-bit microprocessor with internal ROM and RAM which is fully programmable with interface logic which is partially mask programmable. In general the chip is suitable for applications requiring simple arithmetic, display of up to 43 digits and interfacing with analog systems.

The following options refer to the asterisked notes appearing in the preceding text:

(*1) Programmable from 1 to 15 seconds or static.

(*2) Alternatively E's can be displayed.

(*3) Programmable from 0.1 to 1.5 seconds.

(*4) Programmable from 10Hz to 1Hz.

(*5) Alternative mask option requires "auto" button to be pressed before device goes into auto mode.

(*6) Minute minder can be 2, 3 or 4 digits.

(*7) Alternatively a "clear" instruction cancels alarm.

(*8) Programmable to suit various ranges of temperature.

(*9) Programmable from 0° to 100°.

(*10) Output can be a steady on/off control, a pulsed temperature output or a composite of both.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Voltage on any pin with respect to V_{SS} ..... −0.3V to 20V
Ambient Operating Temperature range ..... 0°C to 85°C
Storage Temperature range ..... −65°C to 150°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$V_{SS} = 0V$
$V_{DD} = +12V \pm 10\%$

Characteristic	Min.	Typ.	Max.	Units	Conditions
50/60Hz Clock input					
Logic '0'	−0.3	—	3	V	
Logic '1'	8	—	13.2	V	
Multiplex Clock Frequency	—	200	—	kHz	See Note 1
Multiplex and Segment output					
Logic '0'	—	—	2	V	$I_{OUT} = 20mA$
Logic '1'	8	—	V_{DD}	V	$I_{source} = 10\mu A$
Keyboard					
Contact Resistance					
'On'	—	—	100	Ω	
'Off'	1	—		MΩ	
Capacitance	—	—	20	pF	
Switch Outputs					
Logic '0'	—	—	2	V	$I_{out} = 30mA$
Logic '1'	8	—	V_{DD}	V	$I_{source} = 10\mu A$

NOTE 1: External resistor determines oscillator frequency.

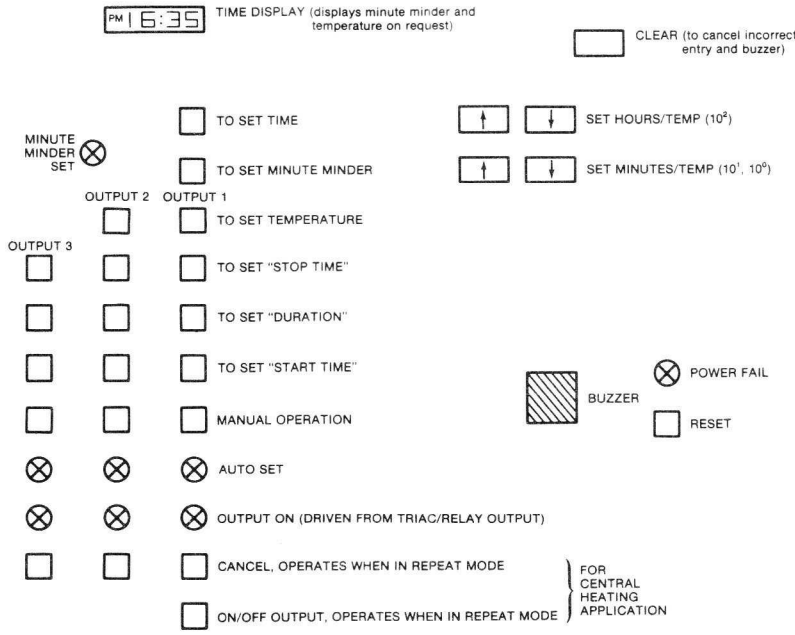


Fig.1 TYPICAL AY-3-1250 CONTROLS FOR INCREMENTAL INPUT COOKER TIMER

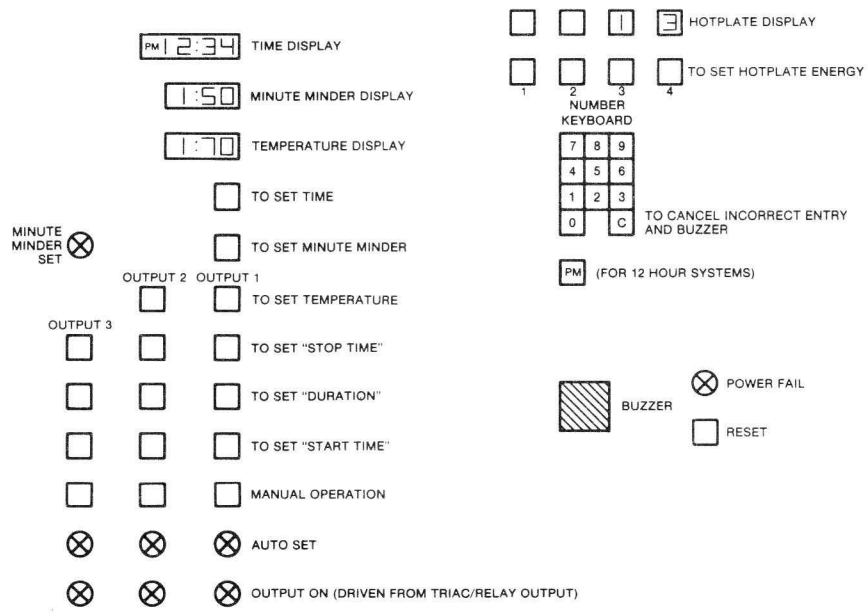


Fig.2 TYPICAL AY-3-1251 CONTROLS FOR FULL KEYBOARD COOKER TIME

CONSUMER

Microwave Oven Timer

FEATURES

- Oven control timer (up to 99 mins. 99 secs.)
- Four-digit time display
- Minute timer (up to 99 mins. 99 secs.)
- Interfaces easily with a capacitive keyboard or standard switches
- Interlock circuitry easily adapted for safety
- Ten number digit entry, five function entries, leading zero suppression
- Status indication
- Output has up to three controlled duty cycles
- Built-in twelve hour clock
- Audio output at end of timed sequence.

DESCRIPTION

The AY-5-1260 is a microprocessor based timer circuit ideally suited for microwave ovens. It has an output which produces three duty cycles for magnetron control and two other outputs which are used as indicators for the five functions which can be entered.

OPERATION

When connected as shown in the System Diagram with a touch plate capacitive control, the timer is used as follows:

Clock Set

After power is turned on, time can be set by touching the clock pad. This illuminates all five LED function indicators. Time can now be entered, i.e., 8:15, touch 8 then 1 then 5. The display will show each new digit entry from the right hand side of the display.

The clock will start when the clock pad is touched once again. The clock will now run from the 60 Hz line power in a normal fashion updating time every minute.

Defrost

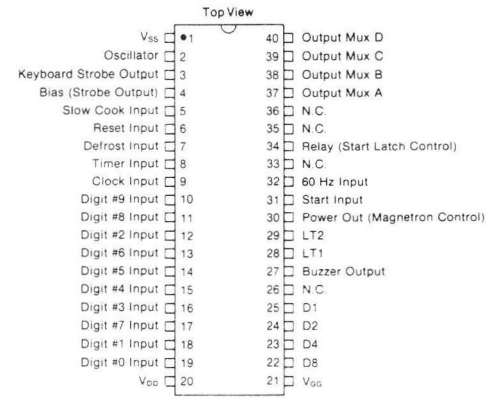
The defrost function can be actuated by touching the defrost pad illuminating the defrost LED and entering the defrost time in minutes and seconds. If 15 minutes is desired, touch 1 then touch 5 and touch 0 twice. The display will read 1500. The defrost will start when the start switch is actuated and end with an audible beep for 3 seconds. The output duty cycle for defrost is 40% on 60% off.

Slow-Cook

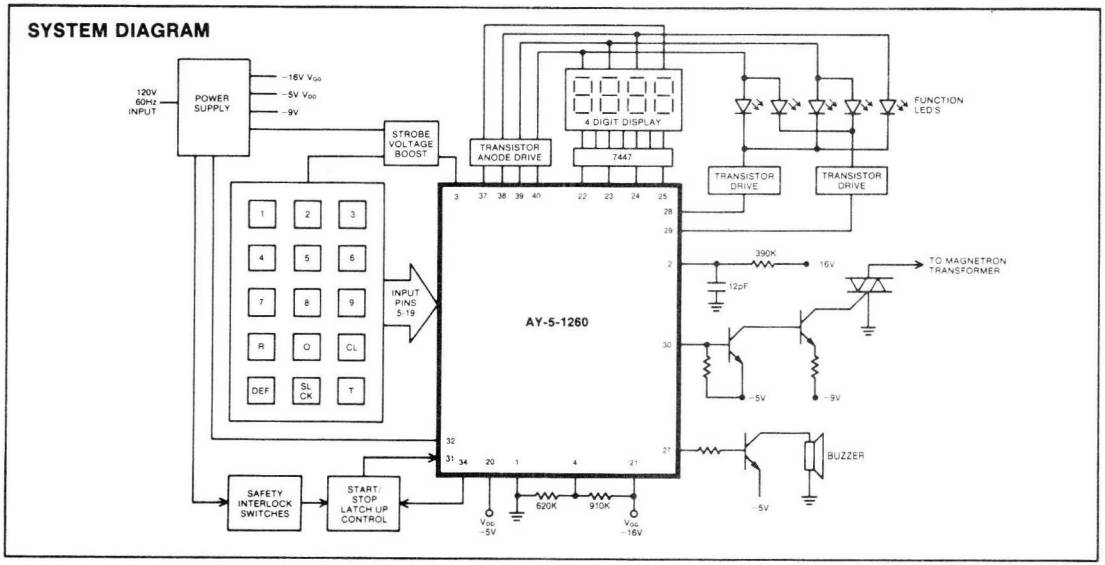
The slow cook mode can be actuated by touching the slow-cook pad (illuminates the slow-cook LED) and entering the slow-cook

PIN CONFIGURATION

40 LEAD DUAL IN LINE



SYSTEM DIAGRAM



time in minutes and seconds. If 13 minutes 30 seconds is desired, touch 1, 3, 3, 0 sequentially on the keyboard. The display will read 1330. The slow cook will begin when the start switch is actuated and end with an audible beep for 3 seconds when finished. The output duty cycle for slow cook is 50% on and 50% off.

Cook

The cook mode can be actuated by entering the cook time in minutes and seconds. If 10 minutes is desired, touch 1, 0, 0, 0 sequentially on the keyboard. The display will read 1000. The cook will start when the start switch is actuated and end with an audible beep for 3 seconds when finished. The output duty cycle during cook is 100% on.

Minute Timer

The minute timer doesn't turn the oven on, but can be used for other timed chores in the kitchen. If 3 minutes is desired, touch 3, 0, 0 in sequence, then touch the timer pad and the timer will count down 3 minutes and beep for 3 seconds when finished.

Multiple Defrost, Cook or Slow Cook Operation

The timer can also be set up to automatically defrost then cook for a desired time. Times can be set as described in the defrost, slow cook/cook modes, but after a defrost entry a slow cook time or cook time should be entered before activating the start switch. The timer will now count down in the defrost mode, switch to a hold time equal to the cook or slow cook time entered, then switch to the actual cook or slow cook mode for the time entered. The oven now has the ability to defrost and cook as desired.

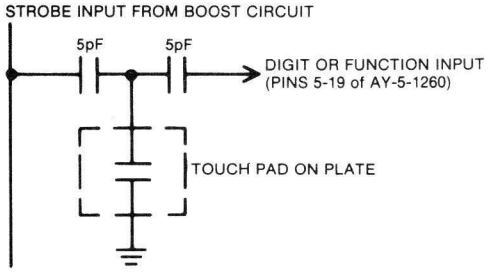


Fig.1 TOUCHPLATE FUNCTION

Reset

The reset can be used if a mistake in entry has been made and correction is necessary. Touching the reset pad always brings back the time of day from the clock. All new entries can be made after reset. If a timed function is running and an abort is desired the stop switch turns the output off and returns the timer back to the time of day as in reset.

Touch Plate Operation

As long as strobes continue to all inputs, the AY-5-1260 detects no new input commands. As soon as an input pad is touched, the strobe to that input is grounded and that digit or function is requested.

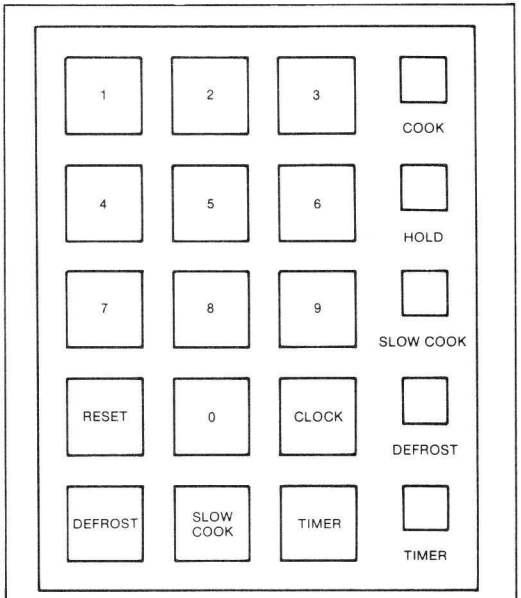


Fig.2 TYPICAL TOUCHPLATE LAYOUT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

	Min	Max
Supply voltage	+0.3	−20 Volts
Logic input voltages	+0.3	−20 Volts
Operating Temperature	0°	+70°C
Soldering Temperature	—	260°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Typ	Max	Units	Conditions
V_{GG}	14.6	—	17	Volts	
V_{DD}	4.5	—	5.5	Volts	
Logic "0" Input	V_{SS} +.3	—	V_{SS} −1	Volts	
Logic "1" Input	10	—	17	Volts	
Logic "1" input pins 31 & 32	10	—	15	Volts	
Touch Plate "0"	—	−1	—	Volts	
Touch Plate "1"	—	−2.88	—	Volts	
Onboard OSC Freq.	150	—	180	kHz	
On Resistance Inputs Pins 5-19	—	—	15	kΩ	
Output Leakage	—	—	20	μA at 17 Volts	
Input Leakage Pins 2, 31-33, 36	—	—	5	μA at 17 Volts	
Input Leakage Pins 5-19	—	—	20	μA at 17 Volts	

CONSUMER

Digital Thermometer

FEATURES

- Temperature range −39.9 to 0°C (−39.9 to 39.9 actual)
- Accuracy ± 1°C, 0°C to −30°C
- Direct drive of liquid crystal displays
- Direct drive of 0.6" common anode L.E.D. displays
- Uses thermistor temperature sensor
- Can be used as a digital voltmeter with digital autozero ± 399 range
- 9 volt supply
- Leading zero blanking
- Power failure/over-range indication
- Adjustable hysteresis: 0, 0.2, 0.4, 0.8, 2, 4, 8 degrees.
- Two control/alarm outputs, high and low.

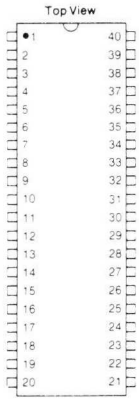
DESCRIPTION

The AY-3-1270 Digital Thermometer/Controller chip when used in conjunction with a Thermistor, an LED or LCD display, and a power supply forms a complete unit intended primarily for use in Deep Freezers, though it may also be used for the display and control of any parameter.

A power fail detector is incorporated on the chip. If power is removed for more than a specified time the initial reading at restoration of power will be retained and the display will flash. The display will also flash if during normal operation an overrange condition occurs.

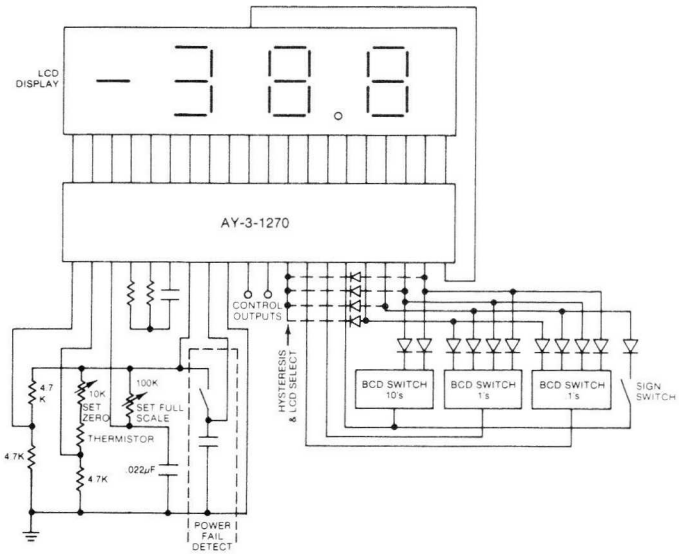
With minor changes to the peripheral circuitry the chip can be used for other temperature ranges or used as a 2¾ digit digital voltmeter.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



Not yet defined.

SYSTEM DIAGRAM L.C.D. Thermometer/Controller with .1°C Set Point Steps & Power Fail Detection



PIN FUNCTIONS

Pin	Function
Segment A1, B1, C1, D1, E1, F1, G1 Outputs	Units digit 7 segment outputs capable of driving common anode LED or LCD displays
Segment A2, B2, C2, D2, E2, F2, G2 Outputs	Tens digit 7 segment outputs capable of driving common anode LED or LCD displays
Segment C3, E3, F3 Outputs	Hundreds digit outputs capable of driving the c, e, f segments respectively on common anode LED or LCD displays.
Segment A3-B3-D3-G3 Output	Single output for driving the a, b, d, &, g, segments of a common anode LED or LCD display simultaneously.
± Output	Polarity output capable of driving an LED or LCD display.
Decimal Point Output	Output capable of driving a DP on an LCD display.
Set Point Input 2°	Common input for the units, tens and hundreds 2° bit.
Set Point Input 2^1	Common input for the units, tens and hundreds 2^1 bit.
Set Point Input 2^2/sign	Common input for the units and tens 2^2 bit and the sign bit.
Set Point Input 2^3	Common input for the units and tens 2^3 bit.
Set Point Input Units Strobe	Common input for the units set point switch.
Set Point Input Tens Strobe	Common input for the tens set point switch.
Set Point Input Hundreds/Sign Strobe	Common input for the hundreds and sign switch
Backplate Drive Output	Square wave signal connected to the Backplate of the LCD.
Clock Oscillator 1, 2, 3	An R-C network connected to these pins sets the clock frequency.
Ramp Input	Connected to ramp R and C.
Comparator Input 1	Connected to nominal 4.5V reference.
Comparator Input 2	Connected to thermistor network.
10 Sec Timer/Reset Input	Connected to C and reset switch to detect power fail and subsequently resetting.
Set Point Hysteresis/LCD select	Common input for the hysteresis and LCD select switches.
Control Output Low	Comes on when temperature reading is less than Set point minus hysteresis. Goes off when temperature reading equals Set point (See Fig. 1).
Control Output High	Goes off when temperature reading is greater than Set point plus hysteresis. Comes on when temperature reading equals Set point (See Fig. 1).
V_{SS}	Negative supply
V_{CC}	Positive supply

OPERATION

The AY-3-1270 uses a single ramp conversion technique to measure the imbalance of a thermistor bridge temperature sensor. A digital autozero system which operates on every other measurement cycle is employed to compensate for offsets in the comparators.

The chip may be used as a digital voltmeter by removing the thermistor network and connecting the signal to be measured between the two comparator inputs.

The set point circuitry compares the actual reading to the value presented to the set point inputs.

Two outputs are provided, one which operates at set point plus hysteresis and the other which operates at set point minus hysteresis. In addition .05° display hysteresis has been introduced to prevent control output and L.S.D. jitter.

An optional power failure detection circuit is provided. At power up the chip will read normally for about 10 sec.—actual time determined by external components—then it will store the last reading and flash the display. In this condition the chip will continue to make measurements and operate the control outputs normally. Operating the reset button will restore the normal display. If there is a short duration power failure the circuit will ignore it, if it lasts longer than 10 sec. the alarm condition will occur.

There is a high reading option wherein reconnection of the Digit 3 drives the reading range can be changed to 20.0 to 49.9.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3 to +12 Volts
Storage temperature range ..... −65°C to 150°C
Ambient operating temperature range ..... −25°C to 70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise specified)
$V_{SS} = 0V$
$V_{CC} = +9V \pm 20\%$
$T_A = -25°C$ to $+70°C$

Characteristic	Min	Typ	Max	Units	Conditions
Display drive output ON Resistance	—	—	150	Ω	$V_{OUT} = +2V$, $I_{OUT} = 12.5mA$
Display Drive Output OFF Resistance	—	—	10	kΩ	$V_{OUT} = (V_{CC} - 1)$, $I_{OUT} = 0.1mA$
Max. Logic '0'	—	—	2	V	
Min. Logic '1'	6	—	—	V	
Input pull-up resistance	20	—	100	kΩ	
Max. switch 'On' resistance	—	—	106	Ω	
Min. switch 'Off' resistance	1	—	—	MΩ	
Strobe output 'ON' resistance	—	—	2	kΩ	$V_{OUT} = +1V$, $I_{OUT} = .5mA$
Strobe output 'OFF' leakage	—	—	10	μA	
Supply Current	—	40	—	mA	

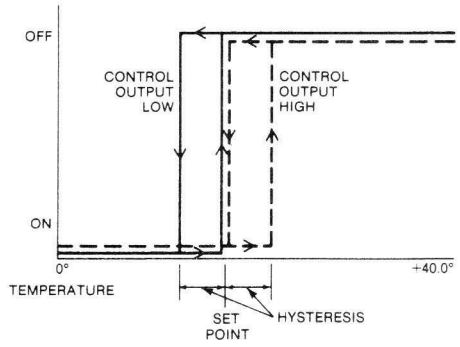


Fig. 1 HYSTERESIS AND CONTROL OUTPUTS

Coinbox Memory

FEATURES

- 63 Credit Capacity
- 2 Special Selection Options
- 7 Different Coin Inputs
- Easy Price or Program Change
- "Make Selection" Control
- Input Noise Rejection on Chip
- On Chip Clock Oscillator

APPLICATIONS

- Arcade Equipment
- Vending Machines
- Gaming Devices
- Programmable Counters and Timers

DESCRIPTION

The General Instrument AY-1-8622 is a single monolithic P-channel MOS/LSI Chip designed for use as a credit accumulator in coin-operated equipment. The chip requires only a power supply and a coin acceptor to complete the cash register section. Coin inputs allow 7 different coin or paper denominations to be used. Both credit and bonus price are easily changed in the field. Two special selection options may be programmed.

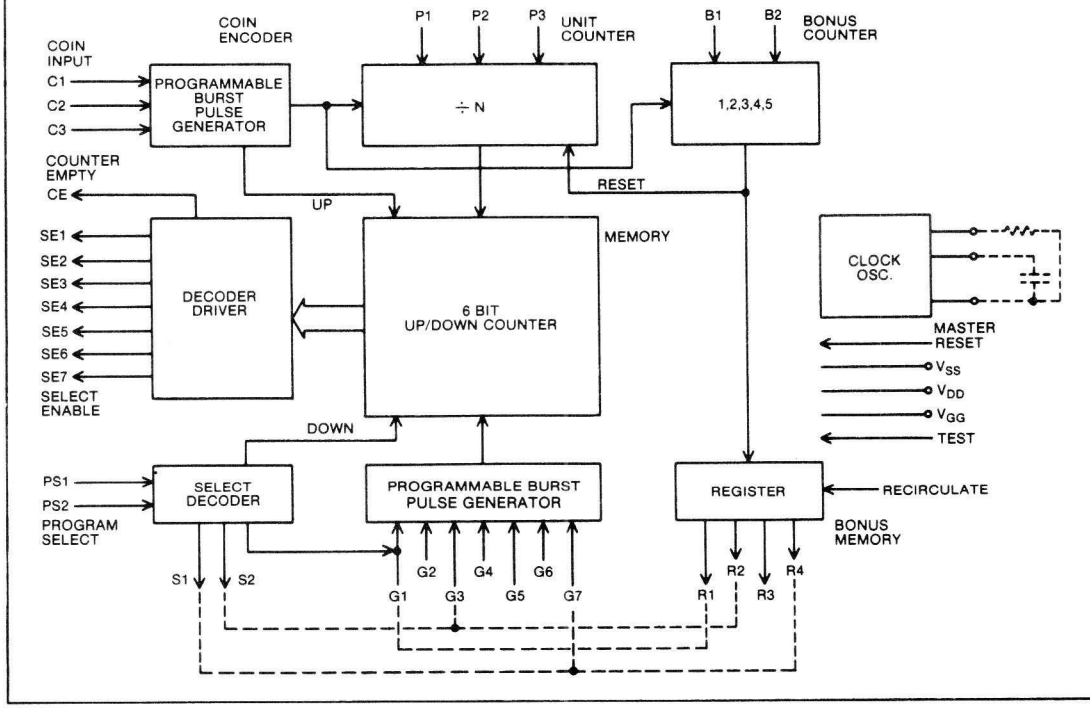
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

V_{SS} Power Supply	1	40	Unit Price Control P3
P2 Unit Price Control	2	39	Selection Enable 2
P1 Unit Price Control	3	38	Selection Enable 3
B1 Bonus Credit Control	4	37	Selection Enable 4
B2 Bonus Credit Control	5	36	Selection Enable 5
C3 Coin Input	6	35	Selection Enable 6
Master Reset	7	34	Selection Enable 7
V_{GG} Supply	8	33	Selection Enable 1
C2 Coin Input	9	32	Counter Empty
C1 Coin Input	10	31	Program Select Output S2
Test Point	11	30	Program Select Output S1
Recirculate	12	29	Clock Capacitor
R4 Bonus Register Output	13	28	Clock Capacitor
R3 Bonus Register Output	14	27	Clock Resistor
R2 Bonus Register Output	15	26	G1 Credit Input
R1 Bonus Register Output	16	25	Program Select input PS1
V_{DD} Supply	17	24	Program Select Input PS2
G7 Credit Input	18	23	G2 Credit Input
G6 Credit Input	19	22	G3 Credit Input
G5 Credit Input	20	21	G4 Credit Input

BLOCK DIAGRAM



CONSUMER

PROGRAMMING THE AY-1-8622

The AY-1-8622 has been designed for the maximum versatility compatible with one package. The user can program the device to operate with different currencies and with different pricing or credit structures.

Currency Programming

C1, C2, and C3 form the 3 coin inputs, with weighting as indicated under the pin function section of this data sheet. If, for example, a nickle (5¢) is chosen as one unit, a dime (10¢) would have a weight of two units, a quarter (25¢) a weight of five units, etc. In this case, the user would program his coin acceptor to produce a "1" at C1 when a 5¢ piece is deposited, a "1" at C2 when a dime is deposited, and a "1" at C3 when a 25¢ piece is deposited.

Pricing Structure Programming

Pricing structure consists of three controllable options: Unit Price Control, Bonus Credit Control, and Program Select Control. The first two of these control how many play credits the customer receives for his coin deposits. Program Select Control determines how many play credits are used by his various play options.

Unit Price Control is through inputs P1, P2, and P3. If, for example, 5¢ is one unit, and 10¢ is one play, P2 would be tied to logic "1". If 25¢ is one play, the P1, P2, and P3 would all be tied to "0".

In many applications it is desirable to present the customer with an incentive for depositing additional money to receive "bonus" plays. For example, two plays for 25¢, five plays for 50¢. This option is controlled by the Bonus Credit Control.

Bonus Credit Control, is derived through inputs B1 and B2, in conjunction with the Program Control Matrix. Unlike the unit price control section which drives the credit accumulator directly, the Bonus Credit Control drives a shift register whose outputs, R1 through R4, form part of the Program Control Matrix. B1 and B2 control how many units are required to increment the shift register. The first bonus places a "0" onto R1, the second moves it to R2, etc.

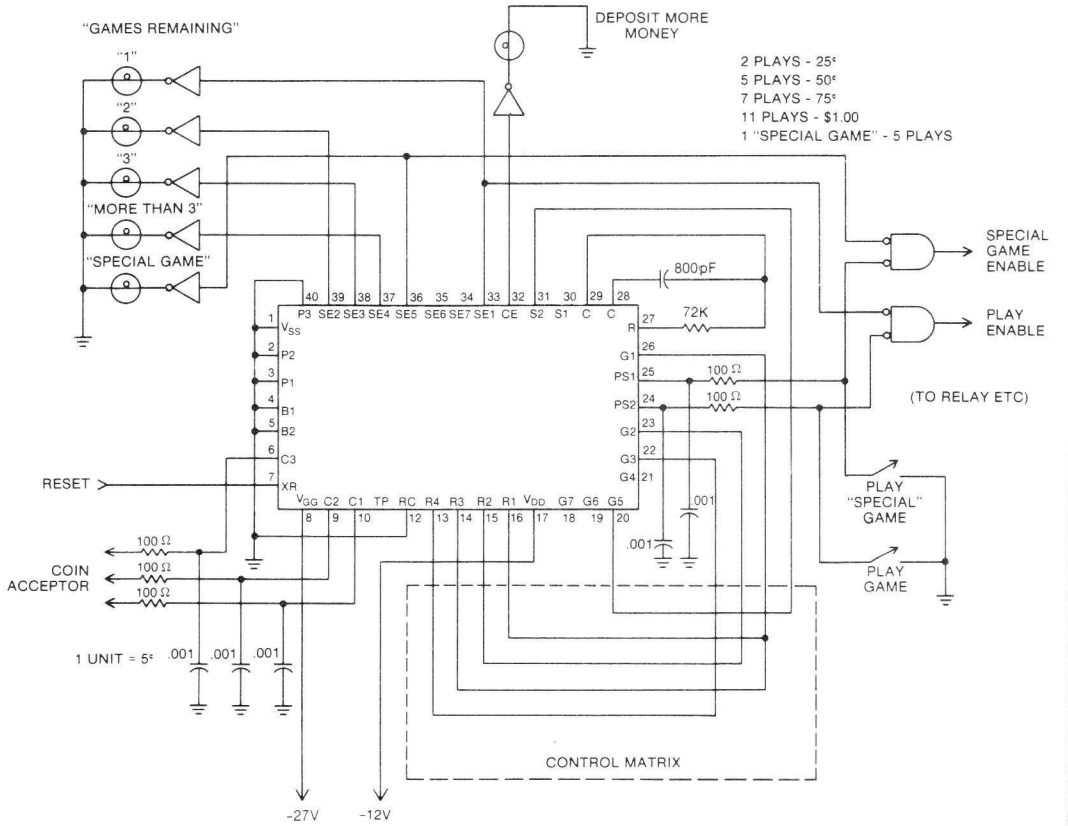
Control Matrix

The Control Matrix consists of three sections: S1 and S2 form the Program Select Outputs, G1 through G7 form the inputs to the Credit Accumulator, and R1 through R4 are the Bonus Register Outputs. The Credit Accumulator, a 6 bit up/down counter, is automatically placed in the "up" count mode when a coin input is made, and a "down" count mode when a selection is made. Although single selections and unit price inputs are fed directly into the counter, special play options and bonus credits are entered through the matrix. A "0" on G1 places 1 credit/debit into the counter, a "0" on G2 places 2 credits/debits into the counter, etc.

Typical Example

In the typical application shown one unit is 5¢. P1, P2, P3, B1 and B2 are tied to "0". As a result, there is one play for 25¢ from the Unit Price Control, and one bonus for 25¢. By tying R1 to G1, the bonus gives a bonus play for 25¢, resulting in a total of two plays for 25¢. R2 is tied to G2, so that the deposit of an additional 25¢ results in three additional plays, or a total of fives plays for 50¢.

TYPICAL APPLICATION



OPERATION

Coin inputs are encoded into a series of pulses by the coin encoder. These pulses are fed into the unit price control divider, controlled by P1, P2 and P3, and into the bonus credit control divider, controlled by B1 and B2. The output from the unit price control divider goes to the 6 bit memory. The output from the bonus credit control clocks a 4 bit shift register. The first bonus credit places a "0" into R1, the second moves the "0" to R2 etc.

The memory, a 6 bit up/down counter, is placed into an "up" count mode when coin inputs are made, and a "down" count mode when selections are made. Input to it comes from the unit price control and from a pulse generator controlled by G1-G7. S1, S2, R1-R4 and G1-G7 form the program control matrix and are interconnected by the user to allow the programming of the number of credits triggered by bonuses and debits triggered by selections.

PIN FUNCTIONS

Pin No.	Name	Symbol	Description
1	V_{SS} Power Supply	V_{SS}	Ground
2,3,40	Unit Price Controls	P2,P1,P3	P1, P2, P3 determine the price in units per credit by the following Matrix:

P3	P2	P1	Units per credit
0	0	1	1
0	1	0	2
1	0	0	3
0	1	1	4
0	0	0	5

4,5	Bonus Credit Controls	B1,B2	B1, B2 determine the number of units needed to increment the bonus shift register one place as follows:

B2	B1	Units per bonus Credit
1	1	1
0	1	2
1	0	4
0	0	5

6,9,10	Coin Inputs	C3,C2,C1	C1, C2, C3 are coin inputs. Inputs are weighted as follows:

C3	C2	C1	Weight
0	0	0	no Input
0	0	1	1 unit
0	1	0	2 units
0	1	1	4 units
1	0	0	5 units
1	1	1	8 units
1	0	1	10 units
1	1	0	20 units

7	Master Reset	MR	All counters and registers are reset by a logic "1"
8	V_{GG} Supply	V_{GG}	-27 Volt supply
11	Test Point	TP	For Testing only. Do not make external connections to this Pin.
12	Recirculate	RC	Logic "1" on Pin 12 locks the bonus shift register after it reaches the 4 bonus credit level. Logic "0" on Pin 12 allows shift register to re-cycle from the fourth level to the first.
13,14 15,16	Bonus Register Outputs	R4,R3, R2,R1	The bonus register outputs indicate the status of the bonus register as follows:

R4	R3	R2	R1	Bonus Credits
1	1	1	0	1
1	1	0	1	2
1	0	1	1	3
0	1	1	1	4

17	V_{DD} Supply	V_{DD}	-12 Volt supply

CONSUMER

PIN FUNCTIONS (continued)

Pin No.	Name	Symbol	Description
18	7 Credit Input	G7	A "0" level input on a credit input enters the respective number of credits into the credit accumulator. These inputs are internally clocked by the coin inputs and program select inputs, and are for program control matrix use only. Credits are added when the coin input is addressed and are subtracted when program select inputs are enabled.
19	6 Credit Input	G6	
20	5 Credit Input	G5	
21	4 Credit Input	G4	
22	3 Credit Input	G3	
23	2 Credit Input	G2	
26	1 Credit Input	G1	
24,25	Program Select Inputs	PS2,PS1	These inputs cancel credits as follows: **PS2** **PS1** **Result** 1 1 No Cancellation 1 0 Single Credit cancellation 0 1 Option 1 selected 0 0 Option 2 selected Selection of option 1 or 2 results in program select outputs being triggered. This allows user selection of the number of credits cancelled by both options.
27	Clock Resistor		A 800 pF capacitor between Pins 28 and 29, and a 72K resistor between Pins 27 and 29 give a nominal system frequency of 6.2KHz.
28	Clock Capacitor		
29	Clock Capacitor		
30,31	Program Select Outputs	S1,S2	Program control matrix outputs. Output states are as follows: **S2** **S1** **Option** 0 1 Option 1 selected 1 0 Option 2 selected Single credit select is internally connected to GI.
32	Counter Empty	CE	This Pin is at logic "1" until at least one credit is in the credit counter.
33	Selection Enable 1	SE1	The Selection Enable outputs indicate the number of credits in the credit counter as follows: **SE7 SE6 SE5 SE4 SE3 SE2 SE1 Credits** 1 1 1 1 1 1 0 1 1 1 1 1 1 0 0 2 1 1 1 1 0 0 0 3 1 1 1 0 0 0 0 4 1 1 0 0 0 0 0 5 1 0 0 0 0 0 0 6 0 0 0 0 0 0 0 7 or more
34	Selection Enable 7	SE7	
35	Selection Enable 6	SE6	
36	Selection Enable 5	SE5	
37	Selection Enable 4	SE4	
38	Selection Enable 3	SE3	
39	Selection Enable 2	SE2	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} ..... -30V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... -20°C to +70°C

*Exceeding these rating could cause permanent damage, Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions

V_{GG} = -27 ±1.0V
V_{DD} = -12 ±1.0V
V_{SS} = 0

Characteristic	Min.	Typ	Max	Units	Condition
All Inputs					
Logic "1"	-8.0	—	-30.0	Volts	
Logic "0"	0.3	—	-2.0	Volts	
Input Impedance	20	—	100	KΩ	
Program Control Outputs					
R1, R2, R3, R4, S1, S2	—	—	—	—	
Logic "1"	V_{DD}-0.5	—	—	Volts	100KΩ to V_{DD}
Logic "0"	—	—	-2.0	Volts	0.5mA
Select Outputs					
CE, SE1 to SE7	—				
Logic "1"	V_{DD}-0.5	—	—	Volts	100µA
Logic "0"	—	—	-4.0	Volts	2.0mA
Coin Input Repetition Rate	—	—	30	Hz	
Coin and Program Select					
Date Hold Time	20	—	—	msec	6.2KHz Clock
Clock Frequency	100	—	50	Hz	
Power Consumption	—	250	400	mW	

NOTES:

Clock Frequency: The clock frequency is determined by the values of an external timing capacitor and a resistor connected to Pin 29. An 800pF capacitor and 72K resistor will produce a clock frequency of 6.2KHz.

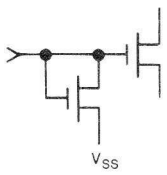
Master Reset: All counters and registers are reset to zero by a logic "1" on Pin 7.

Bonus Recirculate: Logic 1 on Pin 12 locks the bonus register after it reaches the 4th bonus level. Logic "0" allows the 4 bonus levels to be continuously repeated.

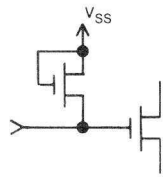
Test Lead: Pin 11 is internally tied to V_{DD}. No external connections should be made to this Pin.

INPUT & OUTPUT MOS STRUCTURES

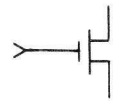
UNIT PRICE CONTROL
BONUS CREDIT CONTROL
RESET, RECIRCULATE INPUTS



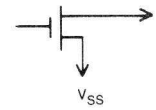
PROGRAM SELECT,
CREDIT INPUTS



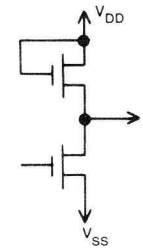
COIN INPUTS



BONUS CREDIT,
PROGRAM SELECT
OUTPUTS



COUNTER EMPTY
SELECTION ENABLE
OUTPUTS



CONSUMER

VTR 3300

Video Tape Recorder Timer

FEATURES

- Four digits plus colon
- LED duplex drive outputs
- No display integrated circuit interface components
- No RFI problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Start time indicator
- 50 Hz or 60 Hz operation
- On-chip oscillator for standby operation with battery during line failure if desired.
- Line power interrupt indication
- Run operation indicator
- Low power dissipation (under 30 mW)

VIDEO TAPE RECORDER FEATURES

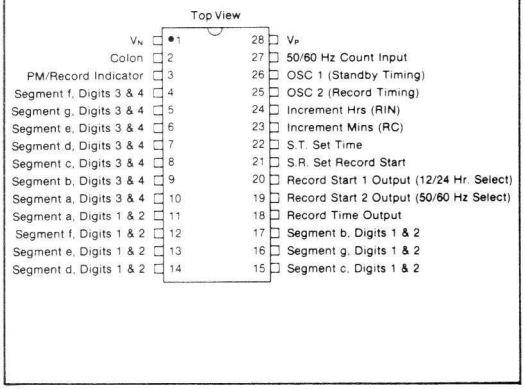
- Simple support electronics
- Analog run setting (user controlled from 5 to 120 minutes with 1 minute resolution)
- Simple setting of actual time and automatic start time
- Hold and synchronize capability for time setting
- Independent hours and minutes setting.

DESCRIPTION

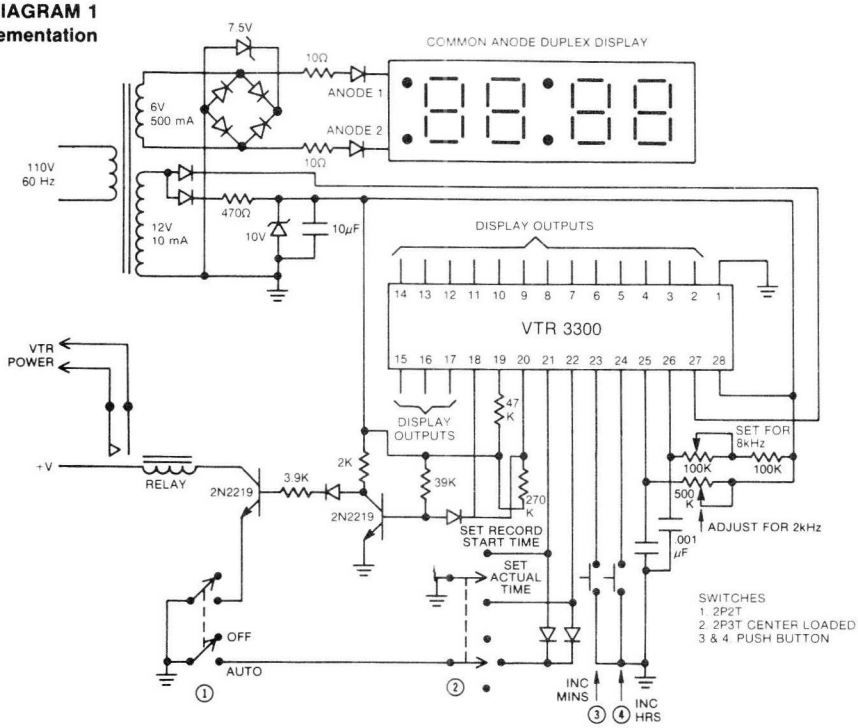
The VTR 3300 is a clock timer circuit for use in video tape recorders. It contains all the necessary logic, control switching, segment drivers and timing circuits to produce an automatic timer with a minimum of external support electronics.

PIN CONFIGURATION

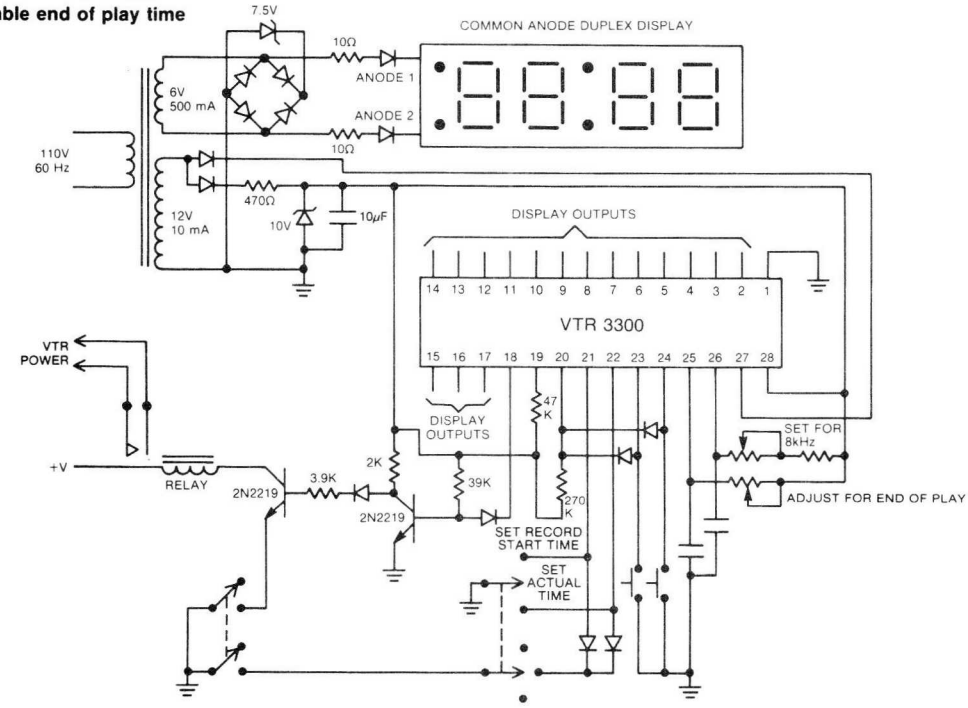
28 LEAD DUAL IN LINE



SYSTEM DIAGRAM 1
Basic Implementation



SYSTEM DIAGRAM 2
Variable end of play time



CONSUMER

PIN FUNCTIONS

V_N - (Pin 1)

Is the most negative power supply to the chip (0 volts).

Segment Drivers (Pins 2-17)

These outputs are 50 Ω switches which drive the segments of common anode LED's directly. Their use and operation is as follows:

To use the VTR3300 with LEDs, the LEDs must be of the COMMON ANODE TYPE, and connected in the following manner.

segment a digit 1 connected to segment a digit 2
segment b digit 1 connected to segment b digit 2
segment c digit 1 connected to segment c digit 2
segment d digit 1 connected to segment d digit 2
segment e digit 1 connected to segment e digit 2
segment f digit 1 connected to segment f digit 2
segment g digit 1 connected to segment g digit 2

segment a digit 3 connected to segment a digit 4
segment b digit 3 connected to segment b digit 4
segment c digit 3 connected to segment c digit 4
segment d digit 3 connected to segment d digit 4
segment e digit 3 connected to segment e digit 4
segment f digit 3 connected to segment f digit 4
segment g digit 3 connected to segment g digit 4

Colon 1 segment connected to colon 2 segment
PM indicator segment connected to sleep/power down indicator segment
Anode digit 1 to anode digit 3
Anode PM indicator to anode digit 4
Anode sleep indicator to anode digit 1
Anode colon upper to anode digit 3
Anode digit 2 to anode digit 4
Anode colon lower to anode digit 2

The anodes can then be selected by the application of alternate half-cycle sine waves derived from a transformer from the line. The phase of the incoming 50/60Hz count to IC will then automatically deliver the correct segment data to the display.

Anode phasing: 50/60 high = digit (1 & 3) selected
low = digit (2 & 4) selected

Record Time Output (Pin 18)

This output turns on while the record time counter is running and is indicated as active by an indicator in the display (Pin 3). This output turns on immediately following a record initiate and is cancelled either by record time being complete, a record time cancel or a Record Start comparison taking place. This pin is also used as an input during circuit test to speed up testing.

Record Start 2 Output/50-60 Hz Mode Select (Pin 19)

This output turns on at record time compare time and stays on unless a Record Start cancel is made.

If the alarm is not cancelled this output will turn off 80 mins for the next 24 hour period.

This pin is also the 50/60 Hz Select input during the time at which Set Time and Set Alarm are at a logic '1' (last data on this input when either Set Time or Set Record Start Time changes state is stored in an internal latch).

Record Start 1 Output/12 Or 24 Hour Select (Pin 20)

This output turns on at Record Start compare time and stays on uninterrupted until either:

a. A Record Start cancel
b. 80 continuous minutes from Record Start time

During the time that Set Time and Set Record Start Time are at a logic '1' together, this pin is the 12/24 hour select input.

The last data on this pin before a data change on Set Time or Set Record Start is stored internally in a latch, and defines 12 or 24 hour operation.

Set Record Start (Pin 21)

This pin, held at zero while Set Time is at a logic '1', enables the Increment Minutes and Increment Hours inputs to the record start counter, such that each change of state (1→0) of the increment inputs will advance the appropriate counter by one unit.

Set Time (Pin 22)

Is identical in operation to the Set Record Start pin, but in this instance allows the counts to be entered into the time counter.

Taking both Set Time and Set Record Start to a logic '0' allows the Record Start outputs to become active when the time reaches the Record Start time. Returning either Set Time or Set Record Start to a logic '1' will cancel the Record Start.

Increment Mins/Record Cancel (Pin 23)

If Set Time or Set Record time is at zero, this input provides one unit of increment for each logic transition from one to zero. (This input is de-bounced against switch noise). If both Set Time and Set Record Time are at a logic '1' or logic '0' and the record timer is running, a logic zero on this input will cancel.

If both Set Time and Set Record Time are at a zero and the Record Start outputs are active (i.e., post record time), then Record Start 2 will be cancelled for a period of up to 5 mins when Pin 23 is taken to logic '0'. If this input is at zero when the alarm comparison takes place, then record start 2 will stay off until 5 minutes have passed.

Increment Hours/Record Initiate (Pin 24)

If either Set Time or Set Record Time is at logic '0', this input provides one unit of increment to the required counter for each logic transition from 1 to 0. (This input is de-bounced against switch noise). If both Set Record Time and Set Time are at logic '1' or logic '0', this input will cause Record Time output to become active for the time resulting from current record timing oscillator frequency.

OSC 2 (Pin 25)

This pin produces a triangular wave oscillation depending on the value of resistance and capacitance. This oscillator is used to produce the Record time period by being gated internally with 160th of Osc 1 frequency (i.e. 50/60Hz).

Additionally connected to this pin is a low level detect circuit used with oscillator 1 for re-setting all internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used to detect that standby operation is required.

OSC 1 (Pin 26)

This pin produces a triangular wave oscillation depending on the external value of resistance and capacitance. The signal is used during normal operation to provide internally to the I.C. -
a. the internal timing for a series of one-shot gates
b. After division, the frequency to de-bounce other external pins via D-type latches. This frequency is further divided down to 50/60Hz and is used as the source frequency during standby operation.
Connected internally to this pin is a low level voltage detector which is used in conjunction with a low level voltage detector on Osc. 2 (pin 25) to reset all the internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used for test purposes.

50/60 Hz In (Pin 27)

This input is the normal source of timing. This input drives both the internal count and the alternate half line selection of the segment outputs.
For equal brightness in the display this input must have a 1:1 mark space ratio (±20%).
There is no necessity for eliminating line noise externally when providing this input signal as an internal arrangement eliminates undesired counts.

V_P (Pin 28)

Is the most positive power supply to the chip (typically 10 volts)

FUNCTIONAL OPERATION

Pins 19, 20, 23 and 24 are dual function pins which operate as inputs or outputs dependent on the state of the Set Time and Set Record Start inputs:

S.T.	S.R.	INC MIN	INC HR	RC	RIN	RS 1	RS 2	50/ 60	12/ 24
1	1	-	-	*	*	-	-	*	*
1	0	*	*	-	-	-	-	-	-
0	1	*	*	-	-	-	-	-	-
0	0	-	-	*	*	*	*	-	-

*Operable - Not Operable

Set time (S.T.)	Pin 22
Set Record (S.R.)	Pin 21
Increment minutes (inc min)	Pin 23
Increment hours (inc hrs)	Pin 24
Record Out cancel (S.C.)	Pin 23
Snooze repeat (S.R.)	Pin 23
Record initiate (SIN)	Pin 24
Record Start 1	Pin 20
Record Start 2	Pin 19
50/60Hz Select	Pin 19
12/24Hr. Select	Pin 20

Using Record Start 1 or 2—Input/Output Functions

When the Set Time (S.T.) and Set Record Start Time (S.R.) inputs are at logic one, the IC outputs Record Start 1 and Record Start 2 become inputs to two bistable gates which store the logic conditions on those pins: 50/60Hz Select on the Record Start 2 pin and 12/24Hr. Select on the Record Start 1 pin.

50/60Hz Select

Set Time or Set Record Start Time must be at zero before data on Record Start 2 changes, or clock can change its 50/60 predivided mode. To avoid this, the following circuit is recommended.

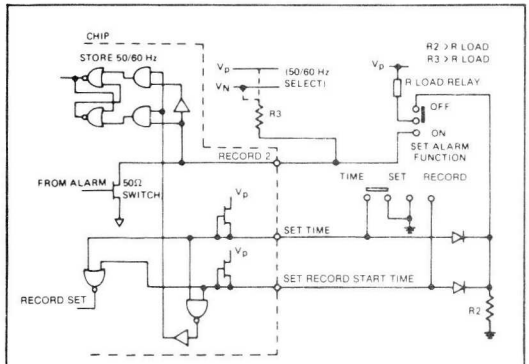


Fig.1 SUGGESTED USE OF RECORD START OUTPUTS TO ENSURE PROPER GENERATION OF INPUT/OUTPUT FUNCTION

With the Set switch in the center position the set inputs are pulled up to a logic '1' by the IC, provided the Record Start switch is in the off position. The load (R load) will pull the junction of the two diodes and R2 to a logic '1'.

The output pin Record Start 2 will either be pulled up or down depending on the connection of R3.

Changing of Set switch will pull down the appropriate input and not affect other external circuit conditions.

Change of position of alarm ON-OFF switch will allow R2 to pull down both Set inputs to zero before Record Start 2 output is connected to load. This ensures that the internal IC latch is disconnected from wake line before data on wake line can influence stored data in latch.

12/24 Hr. Select

For the "Record Start 1 output 12-24 hour select", changing the inputs. Inc Hrs input going to logic zero for at least 20msec will hour mode to 24 hour mode or vice versa.

e.g. 21 : 56 becomes 9 : 56
or 9 : 56 becomes 21 : 56

No leading zero is shown in 24 hour mode:

12 : 32 in 12 hour time becomes 0 : 32 in 24 hour time

(Note: 12 to 24 hour displayed time change can only be achieved when the Record Start is not requested and not in set mode).

For economy of LEDs a single dot is employed which is illuminated during the PM period in 12 hour time.

Time Setting

Four input pins (S.T., SR, Inc Hr., Inc Mins.) are provided to enable the following four functions to be provided:

a. Setting the time
b. Setting the record start
c. Stopping the clock
d. Starting the clock

For synchronizing purposes

S.T. = 0

Allows each depression of Inc Hrs to advance hrs by one count. Clock will stop on the first inc mins and will remain stopped until ST = 1, thus allowing synchronization. The device assumes that the hours may need to be changed without affecting mins, but assumes clock is incorrect if minutes are changed, thus stopping clock and re-setting internal seconds counter to zero.

S.R. = 0

Selects Record Start time and, for each depression of Inc Hours, hours are advanced one and, for each depression of Inc Mins, minutes are advanced one.

NOTE:
No carries from minutes to hours occur during setting of time or alarm

S.T. And S.R.

At zero together - alarm is requested. S.T. and S.R. at logic one together - alarm not requested, but if taken to logic one during post record, record is cancelled.

S.T. and S.R. different will also cancel record if record is active.

S.T.	S.R.	Pre-Record	Post-record
1	1	Not required	Cancel
1	0	Not required	Cancel
0	1	Not required	Cancel
0	0	Requested	Record maintained for 80 mins

S.T., S.R. = 1

If S.T. and S.R. are at a logic 1 together during pre-record time, the following functions can be obtained using Inc Min - Inc Hrs inputs. Inc Hrs input going to logic zero for at least 20msecs will result in record time output going to zero for the period of time set by sleep potentiometer.

At any time Inc Mins input (SC/SR) going to zero for at least 20msec will cancel record timer if record time output is active.

Use of Record Time for Tape Recorder Control

If Record Initiate input (RIN) is directly coupled to Record Start 1 output, then a video tape recorder or any electrical equipment can be turned on at record start time using record start output for a period of time set on Record potentiometer. See figure 2.

Video Recorder Control Outputs

There are three recorder control outputs:

a. Record Start 1
b. Record Start 2
c. Record Time Output

Function

Record Start 1—goes at zero; i.e. is on at Record Start Set time for a period of 80 mins or until an alarm cancel.

Colon Utilization

	COLON CONDITIONS	
FUNCTION	BOTTOM	TOP
Set time	on	off
Set alarm	off	on
Stopped (Sync)	off	off
Run (Record not requested)	1Hz	off
Run (Record requested)	1Kz	1Hz

Sleep dot is on for sleep timer running, flashing for post line interrupt (removed from flashing by movement of S.T. or S.A. to '0')

Stand-By Operation

If a circuit is employed to change the IC power source to battery during line failure, e.g. two diodes, then if the external timing components of oscillator 1 are set to give 8kHz (nominally R = 120K Ω = 2200pF), then the IC will maintain operation to an accuracy of one part in 120, i.e., 30 secs/hr, during the failure. On return to main power the sleep indicator will flash at 1HZ to notify user that indicated time could be in error.

The standby condition is detected by the failure of oscillator 2 to oscillate, therefore oscillator 2 is connected to the line-derived power source, not the battery.

It is assumed OSC 2 input has gone to zero volts.

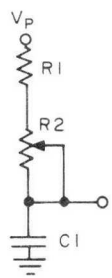
To remove flash condition take S.T. or S.A. momentarily to zero.

Analog Record Time Control

A second oscillator is provided on IC whose frequency can be controlled by an RC network. This oscillator is identical to oscillator one (Standby oscillator) and occupies the same silicon real estate location ensuring that process variations, temperature variations and voltage variations have as nearly as possible identical effects on frequency stability. Oscillator 1, which is set to 8kHz is divided down to 50Hz (20.0 msecs) and is used as a gating time for oscillator 2. The number of gated counts is loaded in the timer (capacity 160 counts) and subsequently counted up at one per minute until 160 is reached.

The range of time is controlled by varying OSC 2 resistance. At 4:1 change in resistance will give variation of 160 to 40 gated pulses, this giving a time of 0 to 120 minutes.

NOTE:



R1, C1 = 120K, 2200PF
R2 = 0 – 450K
Frequency range = 8kHz — 2kHz
Gate time = 20ms
Zero record time counts = $(20\times10^{-3})\times(8\times10^{3}) = 160$
Maximum record time counts = $(20\times10^{-3})\times(2\times10^{3}) = 40$
Range = 120 counts
Hence 1 count = 1 min

Fig.2

To initiate the record timer both S.T. and S.R. must logically be the same, and INC HR/RIN must be momentarily at zero.

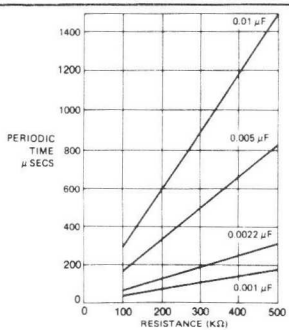


Fig.3 OSCILLATOR CHARACTERISTICS FOR V_P = 10V

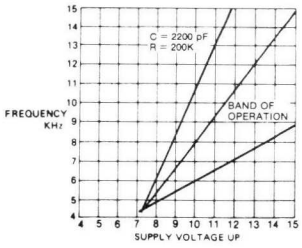


Fig.4 OSCILLATOR CHARACTERISTICS WITH VOLTAGE

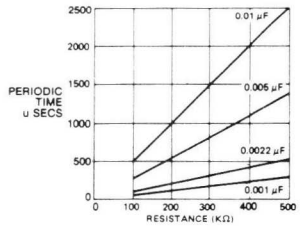


Fig.5 OSCILLATOR CHARACTERISTICS FOR V_P = 7.5V

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage any pin with respect to V_n ..... +20V
Storage temperature ..... -65°C to +150°C
Operating temperature ..... -20°C to +70°C
Lead temperature (soldering 10 sec) ..... +300°C

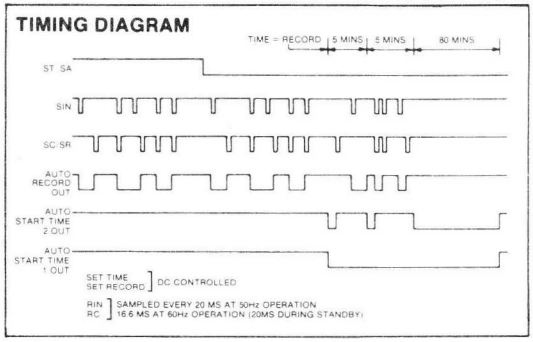
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Typ**	Max	Units	Conditions
Power Supply Voltage	7.5	10	15	Volts	V_n = 0V
Supply Current	—	2	—	mA	
50/60HZ Input					
Frequency (must be identical to anodes)	0	50/60	50,000	Hz	V_p = 10V
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Inputs (Excl Oscillators)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Segments Out (on)	—	30	—	mA	V_{OUT} = 1.5V
(off)	—	10	—	μA	
Start Time 1, 2, Auto Record Out (on)	—	30	—	mA	V_{OUT} = 1.5V
(off)	—	10	—	μA	
Start Time 1, 2 (As Inputs)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Oscillators 1 and 2					
Hi level	—	5.5	—	Volts	Free run
Lo level	—	3.5	—	Volts	
Reset Level	—	—	0.7	Volts	

Unless specified otherwise, characteristics are defined with V_p = 10V at T_A = +25°C.
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Under no circumstances during IC operation must any pin either input or output be taken to a voltage more negative than V_n or IC malfunction will occur.
2. No input or output must be taken to a positive voltage greater than 20 volts or permanent damage can result.
3. No output must be allowed to dissipate a continuous power in excess of 100mW.
4. Total chip continuous power dissipation must not exceed 500mW.
5. The total current being returned to V_n through all device pins must not exceed 1 amp.

TIMING DIAGRAM



Input and Output Characteristics

INPUTS
S.R.
S.T.
INC HR (RIN)
INC MIN (RC)
} Active pull up's to V_p Operate level logic '0' } 250KΩ

50/60HZ count input, active pull down
For correct operation duty cycle of 50/60Hz must be 1:1 ± 20%

OUTPUTS
Normally open circuit
Operate "on" (low impedance typically 50Ω)

INPUTS
Auto Start 1 - as input "1" = 12 hr '0' = 24 hr
Auto Start 2 - as input '0' = 50Hz '1' = 60Hz

CLOCK INPUT NOISE ELIMINATION TIMING
50/60Hz - strobed every 4ms internally for less than 1 μs

CONSUMER

SECURITY

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NO.
SMOKE DETECTORS	Complete ionization smoke detector circuitry.	MEM 4962	8-98
	Circuitry for ionization, photoelectric, or both.	MEM 4963	8-100

MEM 4962

UNDERWRITERS LABORATORIES INC.
RECOGNIZED COMPONENT

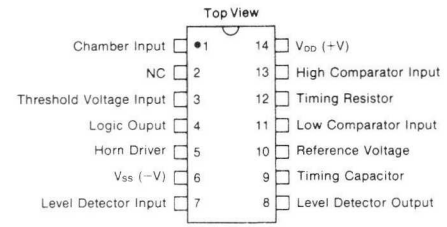
Ionization Smoke Detector

FEATURES

- On-Chip Input MOSFET (Typ. $10^{13}\ \Omega$ to 140°F)
- Stand-By Current Drain 8μA
- Low Battery Warning Beep
- 14-Pin DIP Package
- On-Chip Output Driver
- Designed to Meet UL 217

PIN CONFIGURATION

14 LEAD DUAL IN LINE



OPERATION

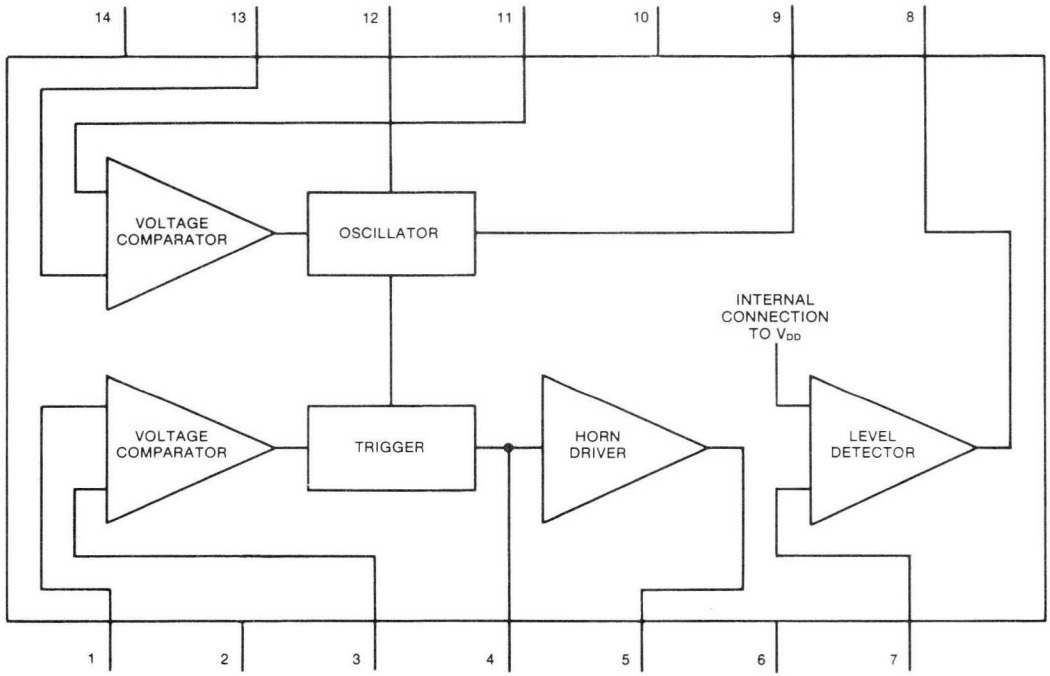
Op. Mode	Input	Osc	Output	
			Logic	N-Ch FET
Stand-by	$V_1 < V_3$, $V_{11} < V_{13}$	Disabled	Low	Off
Alarm	$V_1 > V_3$, $V_{11} < V_{13}$	Disabled	High	On
Low Battery	$V_1 < V_3$, $V_{11} > V_{13}$	Enabled	Pulse*	Pulsed On
Low Battery and Alarm	$V_1 > V_3$, $V_{11} > V_{13}$	Enabled	High	On

*With built-in nominal duty cycle of 1:1500 and nominal frequency determined by 8RC.

LEVEL DETECTOR

$V_{DD} - V_7$	Output @ Pin 8
>0.2V	Low
<0.1V	High

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} 15V
Avg. Horn Current 120mA
Operating Temperature ..... 0 to 60°C
Storage Temperature ..... −30 to 100°C

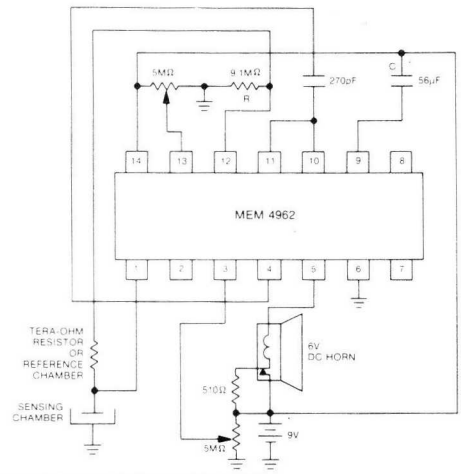
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

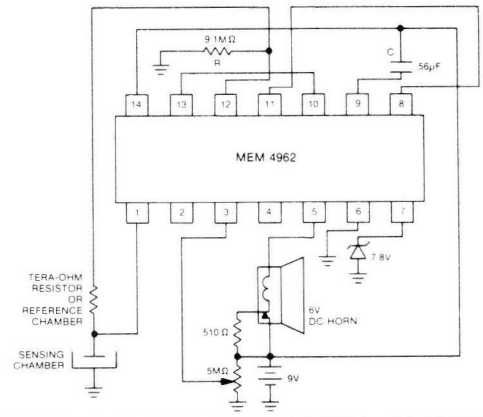
Standard Conditions (unless otherwise noted)

T_A = 25°C
R = 9.1M Ω
C = .56μF

Functional Block	Characteristic	Pin No.	Min	Typ	Max	Units	Conditions
Voltage Comparators	Input Leakage Current	1	–	–	1	pA	Pin 1 @ 9V, Others @ GND
	Pin 1 Breakdown Voltage	1	40	–	–	Volts	Other Pins @ GND
	Common Mode Input Range	1,3 11, 13	1.5	–	V_{DD} −2	Volts	V_{DD} −V_{SS} = 7.5 to 9V
	Trigger Voltage	1, 3 11, 13	–	0.1	0.15	Volts	V_{DD} −V_{SS} = 7.5 to 9V
Oscillator	Period	–	20	45	60	sec	Low Battery condition V_{DD} −V_{SS} = 7.5V
	Pulse Width	–	10	20	–	ms	Low Battery condition V_{DD} −V_{SS} = 7.5V
Output Devices	Logic Sourcing Current	4	5	–	–	mA	1k Ω load Pin 4 and V_{SS}, Alarm condition, V_{DD} −V_{SS} = 7.5V
	Open-Drain N-Ch. FET Sinking Current	5	240	–	–	mA	25 Ω load Pin 5 and V_{DD}, Alarm Condition, V_{DD} −V_{SS} = 7.5V
Complete Chip	Stand-by Current	–	–	4	8	μA	Stand-by Condition, V_{DD}−V_{SS} = 9V
	Low Battery Mode Current	–	–	5	10	μA	Low Battery Condition, Excluding pulse content, V_{DD} −V_{SS} = 7.5V
Ref. Volt.	Ref. Voltage	10	0.8	1.2	3.5	Volts	V_{DD} −V_{SS} = 7.5V
Level Detector	Bias Current	7	–	2.5	3.3	μA	V_{DD} −V_{SS} = 9V

TYPICAL APPLICATIONS Two typical applications are shown. They differ in the way the low battery detect point is determined. The first circuit uses a 5 Meg pot connected to pin 13 while the second circuit uses an external zener diode connected to pin 7.





CONSUMER

MEM 4963

Ionization / Photoelectric Smoke Detector

FEATURES

- Designed to operate with an ionization chamber, photoelectric detector, or both.
- 9 volt operation
- On-chip low leakage FET input and horn driver output
- Smoke Detector interconnection capability: if one detector sees smoke, all detectors sound a warning. An important feature is that the unit detecting smoke will generate an audibly different sound than the rest of the units in the system.
- Designed to meet all applicable U.L. requirements.
- Pulse loading of battery for low battery detection, using either the photo-diode if present, or an external load resistor.
- Engineered for low-cost high volume production.

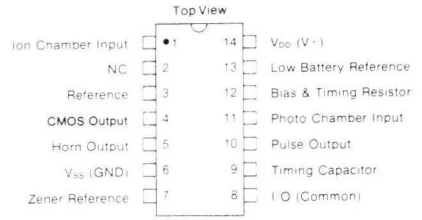
DESCRIPTION

The MEM 4963 has been designed with maximum applications flexibility in mind. Separate input circuitry for an ionization chamber and for photoelectric detector are provided, allowing for the use of the MEM 4963 in systems employing either detection technique or in a system utilizing both in a single unit.

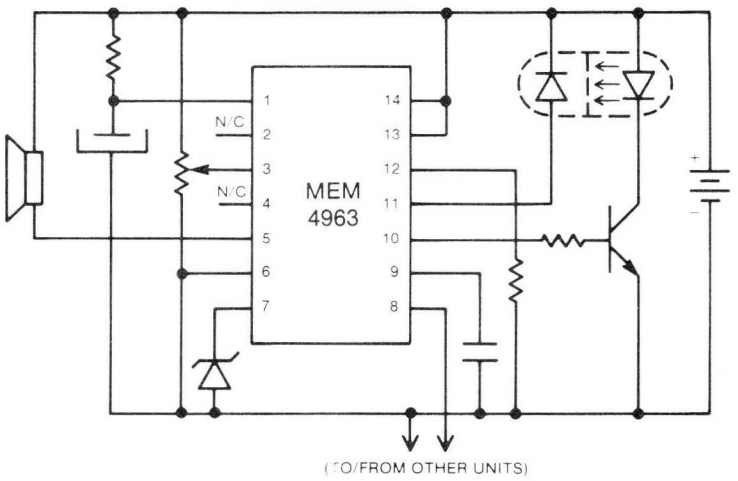
The "communications" capability provides a simple means of achieving a true "system" function for multiple-detector installations for either consumer or commercial applications.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



TYPICAL SYSTEM DIAGRAM (Both Ionization and Photoelectric Detection)



OPERATION

Stand-By

- Battery loaded every 10 sec for 150 μsec
- Photo LED pulsed every 10 sec for 150 μsec.

Local Smoke (ION or Photo)

- Horn sound is steady state
- Battery loaded every .5 sec for 150 μsec
- LED pulsed every .5 sec for 150 μsec.

Low Battery

- Alarm sounds every 40 sec for 20 msec

External Smoke

- Local horn sounds every 100 msec for 20 msec
- LED pulsed every .5 sec for 150 μsec

Priorities

1. Local smoke
2. External smoke
3. Low Batt

} Unit automatically switches from a lower priority to a higher priority output upon receipt of the proper signal.

4. Standby (lowest priority)

NOTE: The Photo LED, if present, is used as load for low battery test. Otherwise, an external load resistor is required.

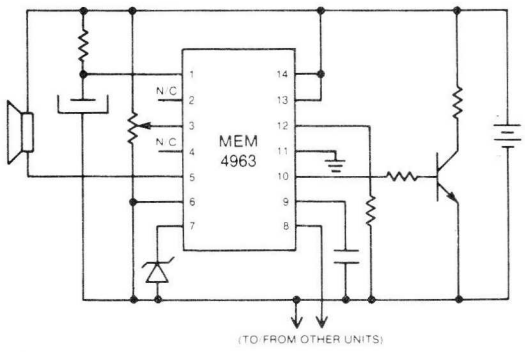


Fig.1 TYPICAL CONNECTION FOR IONIZATION DETECTION ONLY

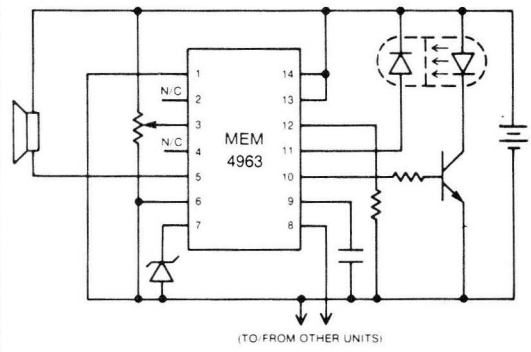


Fig.2 TYPICAL CONNECTION FOR PHOTO DETECTION ONLY

ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

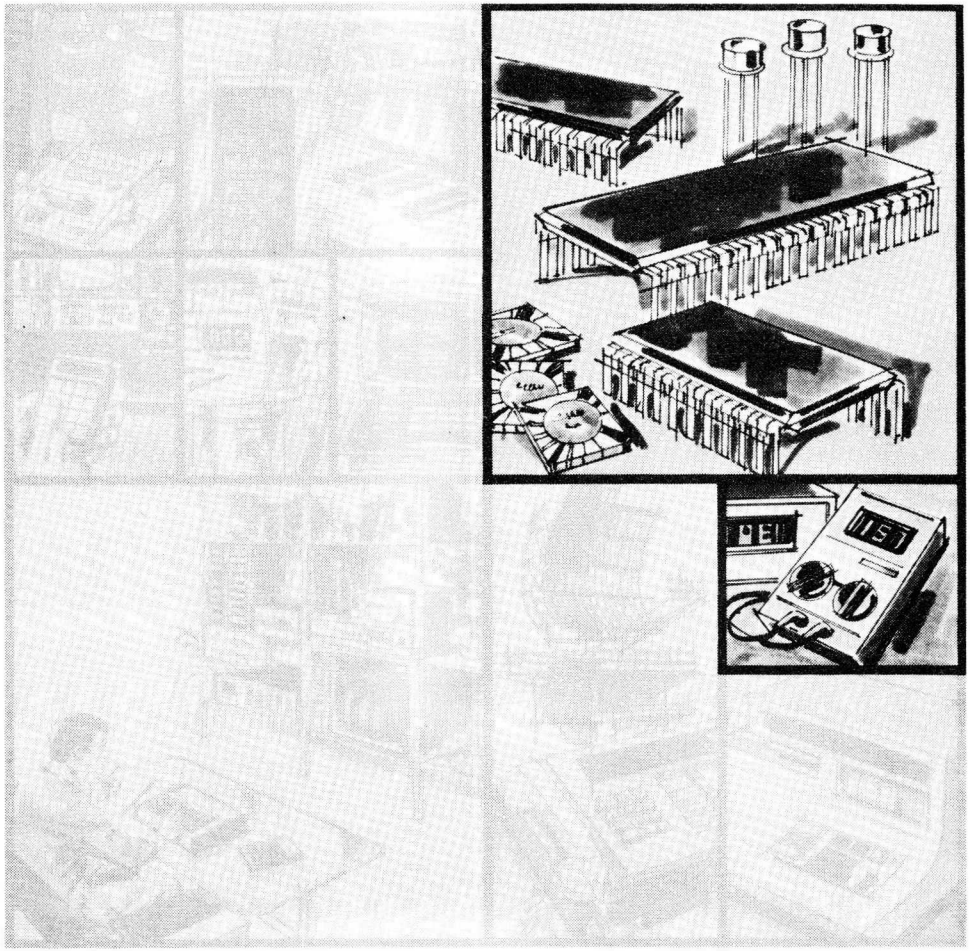
T = 25°C
R = 7.5M
C = .56μF
V_{DD} = 9V Except as Noted

Functional Block	Characteristic	Conditions	Min	Typ	Max	Units
Voltage Comparator	Input Leakage	Ionization Chamber Pin	—	—	1	pA
	Breakdown Voltage	Ionization Chamber Pin	40	—	—	Volts
	Input Range	Common Mode	1.5	—	V_{DD}−2	Volts
	Trigger Voltage		—	0.1	0.15	Volts
Oscillator	Period	Standby	8	—	12	sec
		Ext. Smoke	—	125	—	msec
	Pulse Duration		20	—	45	msec
Total Chip	Operating Current	(Excluding Pulse Content) 9V	—	10	15	μA
Outputs	Horn Driver (N-Ch)	25Ω load @ 7.5V	240	—	—	mA
	CMOS Output (P-Ch)	1 kΩ load @ 7.5V	5	—	—	mA
	I/O Output (P-Ch)	V_{OUT}=5V, V_{DD}=7.5V	5	—	—	mA
Zener	Bias Current		.6	4	7	μA
Pulsed Load Output	Source Current	V_{OUT}=4V, V_{DD}=7.5V	20	—	—	mA
	Pulse Width		120	—	200	μsec
	Period		8	—	12	sec

CONSUMER

INDUSTRIAL/MOSFET 9

Counters/DVMs	9- 3
Mosfet Transistors	9- 29
Mosfet Analog Switches©	9-123



MICRO ELECTRONICS

COUNTERS/DVMs

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
3½ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-5-3507	9-8
		AY-5-3510	9-8
3¾ DIGIT DVM	DVM logic utilizing single ramp integration.	AY-5-3500	9-4
4¾ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-3-3550	9-13
4 DIGIT COUNTER	Counts, stores and decodes 4 decades to BCD outputs.	AY-5-4057	9-24
4 DIGIT COUNTER/ DISPLAY DRIVER	Counts, stores and decodes four decades to 7-segment outputs.	AY-5-4007	9-18
		AY-5-4007A	9-18
		AY-5-4007D	9-18

3¾ Digit DVM

FEATURES

- Single Ramp Integration.
- Three measurement ranges 999, 1999, 2999.
- Dual Polarity.
- Reading Rate up to 70 measurements per second.
- Overrange indication, 2 most significant digits flash.
- Separate overrange output available on 1999 and 2999 ranges.
- Underrange output.
- Operating voltage 13V to 17V.
- Power consumption 30mW typical.
- 7 segment or BCD output.
- Controllable display brightness.
- Load enable freezes display.
- Hold input halts measurement.

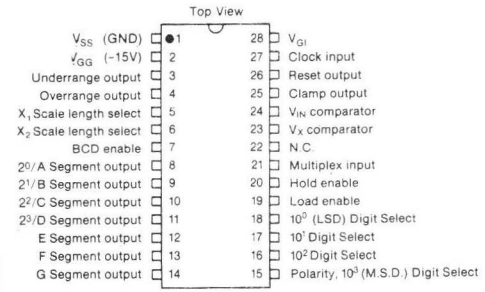
DESCRIPTION

The AY-5-3500 is a single ramp, dual polarity digital voltmeter chip having a selectable scale length of 999, 1999, 2999.

It is manufactured using the MTNS low voltage p-channel nitride technology. Low power dissipation achieved by the use of 4-phase logic with an "on chip" clock generator.

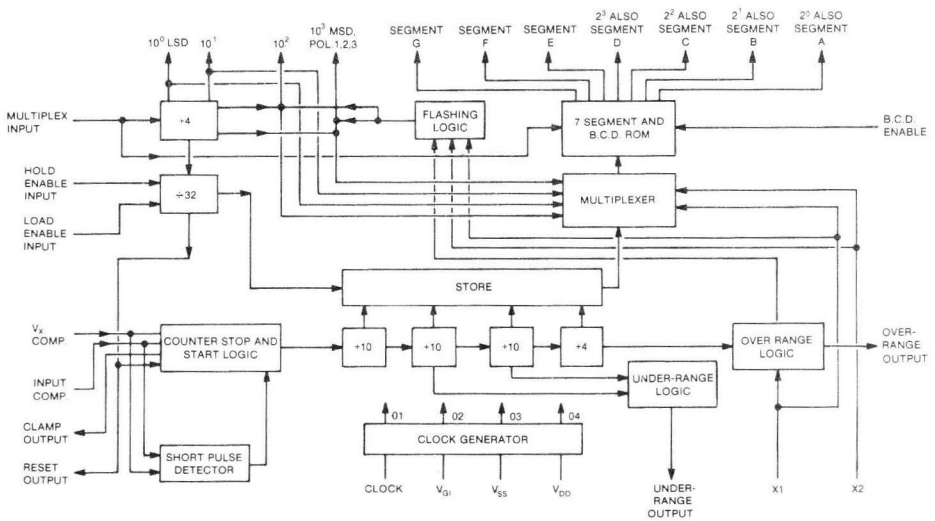
PIN CONFIGURATION

28 LEAD DUAL IN LINE



See next page for details of Pin Functions.

BLOCK DIAGRAM



PIN FUNCTIONS

OVERRANGE OUTPUT
This output goes to logic '1' as soon as an overrange count has been detected. It returns as logic '0' at the end of the measurement cycle.

It operates at 2000 on the 1999 range
It operates at 3000 on the 2999 range

MEASUREMENT CYCLE
The measurement cycle lasts 128 Multiplex clock periods. Data is transferred to the display store from clocks 113 to 120. The counters are reset from 121 to 128.

UNDERRANGE OUTPUT
The underrange output is a pulse from clock 105 to 112 if the reading is less than 259.

SCALE LENGTH SELECT

X1	X2	Scale
0	1	999
1	0	1999
0	0	2999

OVERRANGING

Range	Count	Display	Overrange Output
999	0XXX	XXX	0
	1XXX	1XXX } First	0
	2XXX	XXX } Two Digits	0
	3XXX	3XXX } Flash	0
1999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	1XXX } First Two	1
	3XXX	3XXX } Digits Flash	1
2999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	2XXX	0
	3XXX	3XXX } First Two Digits Flash	1

CLAMP OUTPUT
The clamp output goes to a logic '1' after 3 Counter clock periods following the input from the V_{IN} comparator. This output is used to switch off the V_{IN} comparator thus reducing the average input current by a factor of approx. 70. Fig.2 shows input waveforms without use of clamp output and Fig.3 shows waveforms with use of clamp output and timing for Clamp output.

BCD ENABLE
Logic '0' = BCD
Logic '1' = 7 segment

BCD OUTPUTS
The BCD outputs appear on the 7 segment output lines (Logic (1) is the Active Level); E, F, G are blanked to logic '0'
$A = 2^0$
$B = 2^1$
$C = 2^2$
$D = 2^3$

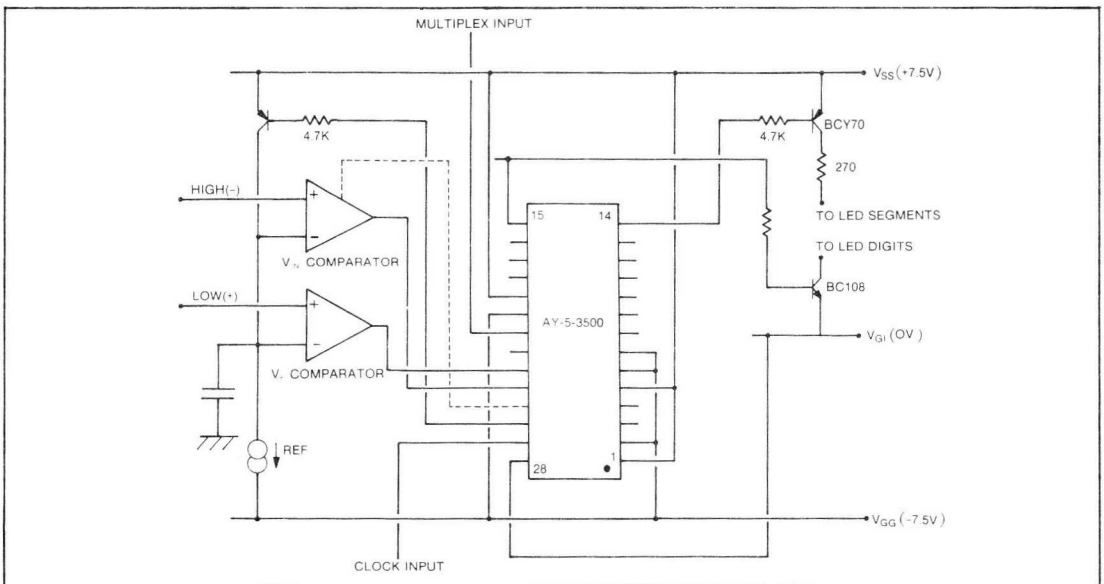
LOAD ENABLE
Logic '0' = Normal Operation
Logic '1' = Freeze Display

HOLD ENABLE
Logic '0' = Halts measurement cycle in reset state
Logic '1' = Normal Operation

RESET OUTPUT
Logic '1' resets ramp generator

NEGATIVE SIGN OUTPUT
Displayed on segment G output on 999 and 1999 ranges. Inhibited on 2999 range.

OPERATION
A linear stable ramp is generated and compared to zero volts and the input voltage in two comparators. The time between the changing of the comparator outputs is proportional to the magnitude of the input voltage, and the sequence of switching gives the polarity.



AY-5-3500 D.V.M. -FSD 999 COMMON CATHODE LED DISPLAY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . −20V to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratngs could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{GG} = −15 ±2V
V_{GI} = V_{GG}/2 (Note 8)
Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	200	—	kHz	
Pulse width	1.5	—	—	μs	At logic '0' and '1' levels
Rise and Fall time	—	—	1	μs	
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−9	—	−17	V	
Multiplex Input					
Frequency	0.5	1.5	10	kHz	(See Note 1)
Pulse width	15	—	—	μs	At logic '0' and '1' levels (Note 2)
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−4	—	−17	V	
Control Inputs					
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−4	—	−17	V	
Leakage (all inputs)	—	—	1	μA	V_{IN} = −10V at 25°C
Segment,Overrange, Underrange Outputs					
Logic '0'	—	—	30	kΩ	V_{OUT} = −0.3V (Note 3)
Logic '1'	—	—	2	kΩ	V_{OUT} = V_{GI} +1V (Note 4)
Digit Select Outputs					
Logic '0'	—	—	1	kΩ	V_{OUT} = −1V (Note 5)
Logic '1'	—	—	15	kΩ	V_{OUT} = V_{GI} +0.3V (Note 6)
Clamp and Reset Outputs					
Logic '0'	—	—	20	kΩ	V_{OUT} = −0.2V (Note 3)
Logic '1'	—	—	5	kΩ	V_{OUT} = V_{GI} + 1V (Note 7)
Supply Current	—	2	—	mA	V_{GG} = −15V excluding output current

**Typical values are at +25°C and nominal voltages.

NOTES
1. This gives a reading rate of typically 12 per second.
   On the 2999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 64.
   On the 1999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 42.
   On the 999 range the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 21.
2. In 7 segment mode, outputs are energised when Multiplex input is at Logic '1'.
   The display brilliance is therefore controlled by the input Mark-Space ratio.
3. Output device connected to V_{SS}.
4. Output device connected to V_{GI} segment energised.
5. Output device connected to V_{SS} digit selected.
6. Output device connected to V_{GI}.
7. Output device connected to V_{GI} Reset condition.
8. V_{GI} is only applied to the output drivers, thus its absolute value is not critical.

TIMING DIAGRAMS

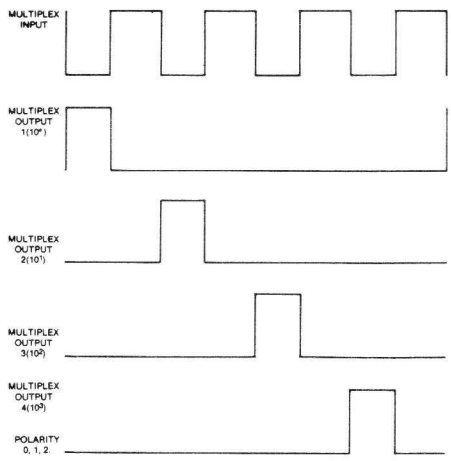


Fig.1 MULTIPLEX INPUT AND OUTPUT

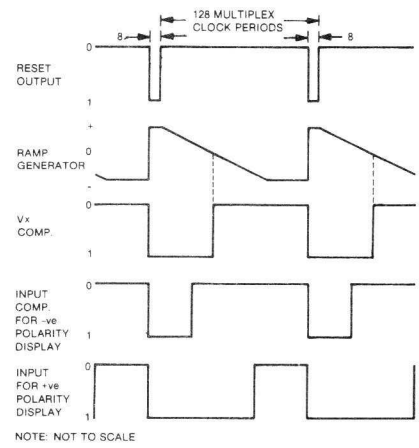


Fig.2 INPUT AND RESET OUTPUT

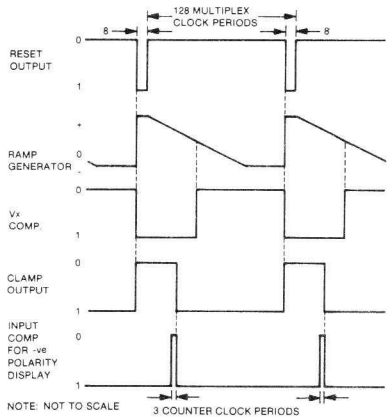


Fig.3 INPUT AND RESET OUTPUT TIMING DIAGRAM SHOWING CLAMP OUTPUT

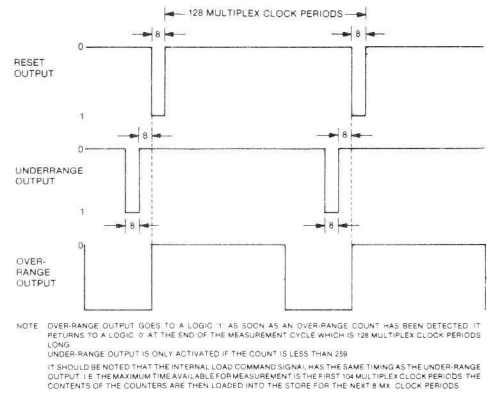


Fig.4 UNDER-RANGE AND OVER-RANGE OUTPUT

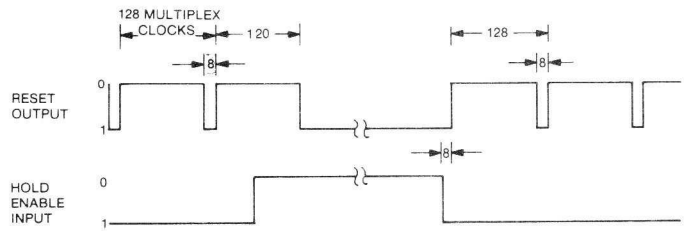


Fig.5 RESET OUTPUT WITH RESPECT TO HOLD ENABLE INPUT

3½ Digit DVM

FEATURES

- 3½ Decade Display (±1999 max. reading)
- Automatic Polarity Detection
- Overrange Indication

AY-5-3507
- Direct LED 7-Segment Drive
- Up to 5 readings per second

AY-3-3510
- BCD Outputs
- Up to 50 readings per second
- Chopper Output provided for oscillator synchronization or underrange indication

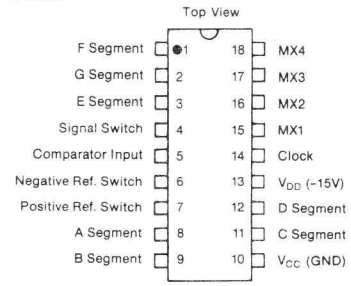
DESCRIPTION

The AY-5-3507 and the AY-5-3510 are MOS LSI circuits containing all the logic necessary for a 3½ Decade Digital Voltmeter utilizing Dual Ramp integration. Automatic polarity detection is incorporated as is automatic overrange indication. For the AY-5-3507, the outputs are multiplexed onto a 7-segment bus allowing easy interface to LED and similar displays. For the AY-5-3510 the outputs are multiplexed onto a BCD bus allowing easy interface to a wide variety of displays.

PIN CONFIGURATION

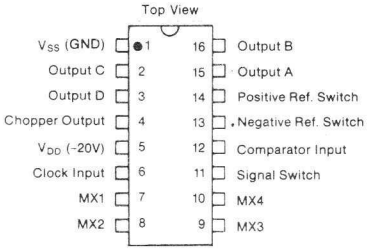
18 LEAD DUAL IN LINE
AY-5-3507

Top View

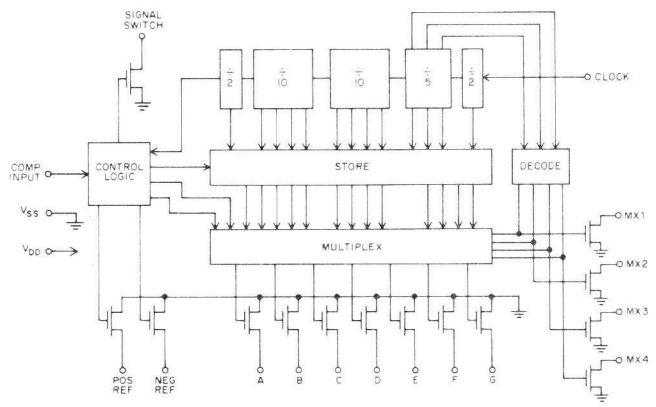


16 LEAD DUAL IN LINE
AY-5-3510

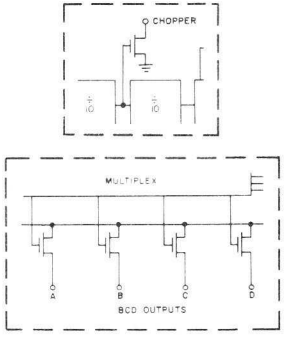
Top View



BLOCK DIAGRAM



AY-5-3507



SAME AS AY-5-3507 EXCEPT AS MARKED ABOVE.

AY-5-3510

PIN FUNCTIONS

Name	Functions
COMPARATOR INPUT	A logic '0' level corresponds to a negative input signal. A logic '1' level corresponds to a positive input signal.
CLOCK INPUT	This signal should be supplied from an external oscillator giving a square wave signal.
REFERENCE SWITCH OUTPUTS	These outputs drive analog switches which connect the Reference Voltages to the Integrator. A logic '0' at the Comparator Input will be followed by a logic '1' at the Positive Reference Switch Output. A logic '1' at the Comparator Input will be followed by a logic '1' at the Negative Reference Switch Output.
SIGNAL SWITCH OUTPUT	This output will be at logic '1' during the time that the signal is connected to the integrator.
DISPLAY MULTIPLEX OUTPUTS	Each output will be at logic '1' for 2 clock periods to display (see Fig. 4). The outputs selected will be as follows:— MX1 O/1, ±, Over-range MX3 Decade 2 (10^1) MX2 Decade 3 (10^2) MX4 Decade 1 (10^0)
AY-5-3507 **SEGMENT OUTPUTS**	The outputs of the 3 decade counters are presented sequentially on the outputs A, B, C, D, E, F, G. In the first multiplex position 1 is indicated by segments B and C,—is indicated by segment G, overrange by the flashing of segments A and D. 0, + and underrange are not indicated.
AY-5-3510 **CHOPPER OUTPUT**	This output is a square wave at 1/100 the clock input frequency. It can be used either to phase lock the clock oscillator to the mains or to provide a 5% FSD under-range signal.
AY-5-3510 **DISPLAY OUTPUTS**	The outputs of the 3 decade counters are presented on the outputs A, B C, D in BCD complement code. A=2^0, B=2^1, C=2^2, D=2^3. At MX1 time, the most significant digit is output on A with its complement on D, sign is output on B and over-range on C.

OPERATION

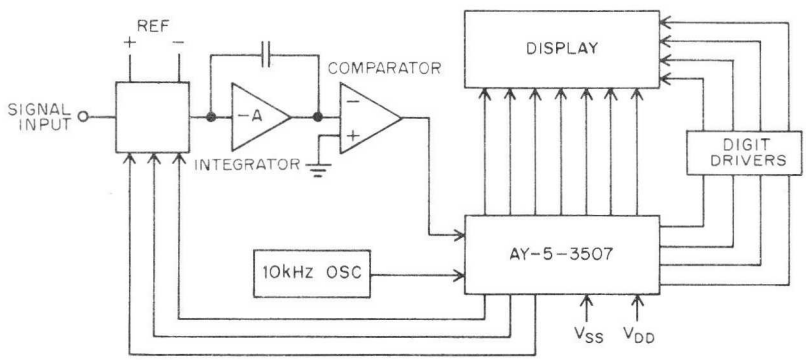
The operation of the circuit is as follows.

Initially the signal, and reference outputs are in the logic '0' state. The counter counts continuously and at the 1999 to 0000 transition a ÷2 is toggled driving the signal switch output to logic '1' turning on the signal switch. The integrator generates a ramp, the amplitude and polarity of which depend on the amplitude and polarity of the input signal. After a further 2000 clock pulses the ÷2 is toggled again. This stores the state of the comparator output in a D type flip flop (this signal represents the sign of the input signal). The appropriate reference switch is then energized to cause the integrator output to ramp back to zero. When the comparator output subsequently changes state the reference is switched off and the number in the counter is transferred to the store together with polarity information.

Should the input signal be so large that zero is not reached during one counter cycle, an overange flip flop will be set and will remain set until the next 1999 to 0000 transition of the counter. During overrange the main display will be set to 0000 and the overrange indicator will flash.

To minimize pin requirements, a time shared output is used. The display store output (including ±, 0/1 and overrange) is gated sequentially, a decade at a time, onto a common 7 line (AY-5-3507) or 4 line (AY-5-3510) output bus.

3½ DECADE DIGITAL VOLTMETER



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Maximum voltage between any pin and V_{SS} pin . . . . +0.3 to −20 V
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C
Maximum power dissipation . . . . 500mW (total), 50mW (per output)

*Exceeding these ratings could cause permanent damage. Functional operaton of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

	AY-5-3507	AY-5-3510
V_{CC}	GND	-
V_{SS}	-	GND
V_{DD}	−12 to −18V	−18 to −24V
Operating Temperature (T_A) =	0°C to +70°C	0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
AY-5-3507					
DC CHARACTERISTICS					
Clock & Comparator Inputs					
Logic '0' Level	−6	—	−18	Volts	
Logic '1' Level	+0.3	—	−1	Volts	
Input Leakage	—	—	10	μA	V_{IN} = −18V, T_A = +25°C
Display Multiplex Outputs (Note 1)					
Logic '1' sink current	1.2	2	3.2	mA	V_{OUT} = −2V, T_A = +25°C, V_{GG} = −12V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −18V, T_A = +25°C
Switch Outputs (Note 1)					
Logic '1' sink current	0.5	0.8	1.25	mA	V_{OUT} = −2V, T_A = +25°C, V_{GG} = −12V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −18V, T_A = +25°C
Segment Outputs (Note 1)					
Logic '1' sink current	4.25	7	11	mA	V_{OUT} = −2V, T_A = +25°C, V_{GG} = −12V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −18V, T_A = +25°C
Supply Current	—	1.5	2.2	mA	V_{DD} = −12V, T_A = +25°C
	—	3.6	5.25	mA	V_{DD} = −18V, T_A = +25°C
AC CHARACTERISTICS					
Clock & Comparator Inputs					
Input Capacitance	—	—	10	pF	V_{IN} = 0V, f = 1MHz
Clock Frequency	DC	—	20	kHz	V_{DD} = −18V
	DC	—	10	kHz	V_{DD} = −12V
Clock Pulse Width	10	—	—	μs	Note 2
Display Multiplex Outputs					
Propagation delay	—	—	4	μs	from Clock positive edge
Segment Outputs					
Propagation delay	—	—	10	μs	from Multiplex output positive edge
AY-5-3510					
Clock & Comparator Inputs					
Logic '0' Level	−8	—	−24	Volts	
Logic '1' Level	+0.3	—	−1	Volts	
Input Capacitance	—	—	5	pf	V_{IN} = 0V
Input Leakage	—	—	10	μA	V_{IN} = −24V
Clock Frequency	DC	—	200	kHz	
Display Multiplex Outputs (Note 1)					
Logic '1' sink current	2	—	—	mA	V_{OUT} = −6V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −24V
Display & Switch Outputs (Note 1)					
Logic '1' sink current	0.7	—	—	mA	V_{OUT} = −4V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −24V
Supply Current	—	—	10.5	mA	V_{DD} = −24V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. All outputs are single-ended ("open-drain"). External pull-down resistors are required.
2. A square waveform is preferred.

TIMING DIAGRAMS

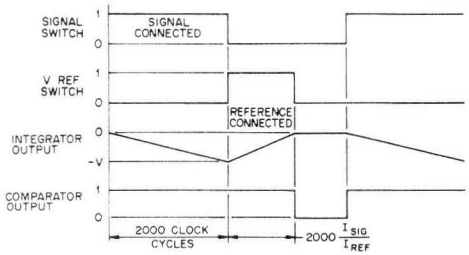


Fig.1

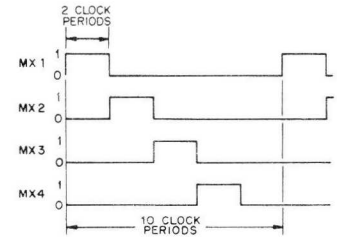


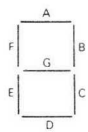
Fig.2 MULTIPLEX WAVEFORMS

TRUTH TABLES

AY-5-3507

7 SEGMENT OUTPUT TRUTH TABLE (MX2-MX4)

	Segment Output						
Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1



MX1 OUTPUT TRUTH TABLE

	Segment Output							
Display	A	B	C	D	E	F	G	
0	0	0	0	0	0	0	0	
1	0	1	1	0	0	0	0	
+	0	0	0	0	0	0	0	
–	0	0	0	0	0	0	1	
UR	0	0	0	0	0	0	0	
OR	1	0	0	1	0	0	0	Flashed

AY-5-3510

BCD OUTPUT TRUTH TABLE (MX2-MX4)

A	B	C	D	Digit Output
1	1	1	1	0
0	1	1	1	1
1	0	1	1	2
0	0	1	1	3
1	1	0	1	4
0	1	0	1	5
1	0	0	1	6
0	0	0	1	7
1	1	1	0	8
0	1	1	0	9

MX1 OUTPUT TRUTH TABLE

A	B	C	D	0/1	Polarity	Over-range
1	X	X	0	0		
0	X	X	1	1		
X	1	X	X		+	
X	0	X	X		–	
X	X	1	X			
X	X	0	X			OR

ANALOG CIRCUIT DIAGRAMS

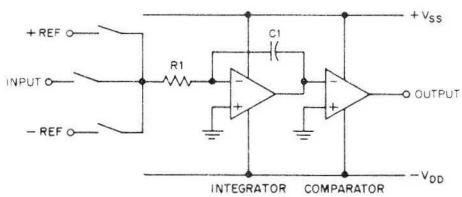


Fig.1 BASIC ANALOG CIRCUIT-AY-5-3507

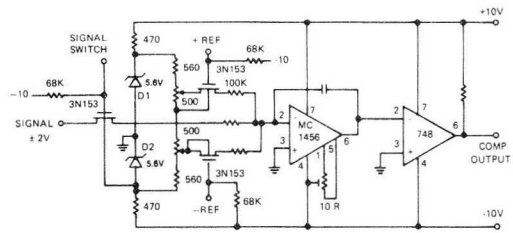


Fig.2 TYPICAL ANALOG CIRCUITRY-AY-5-3510

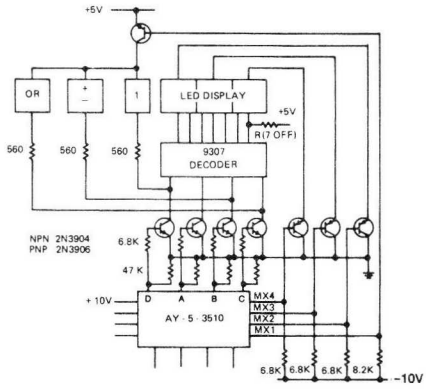


Fig.3 DISPLAY INTERFACE For AY-5-3510

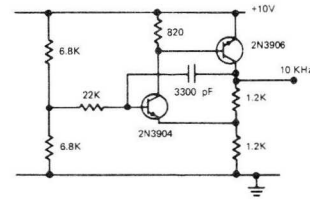
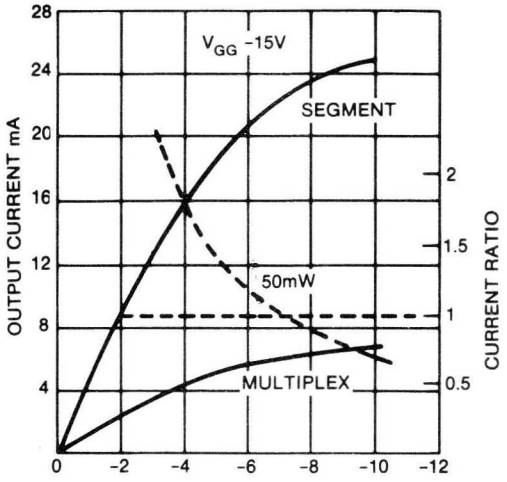


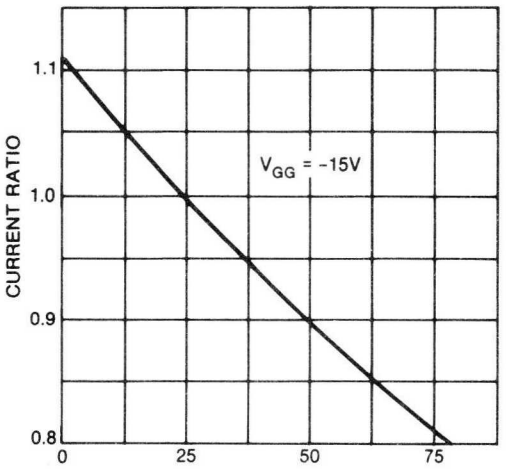
Fig.4 CLOCK OSCILLATOR-AY-5-3510

INDUSTRIAL/ MOSFET

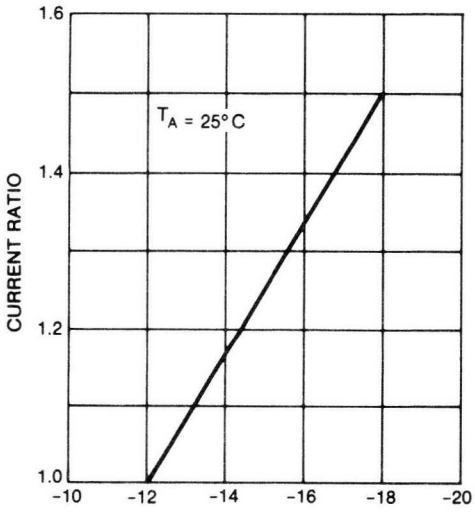
TYPICAL CHARACTERISTIC CURVES



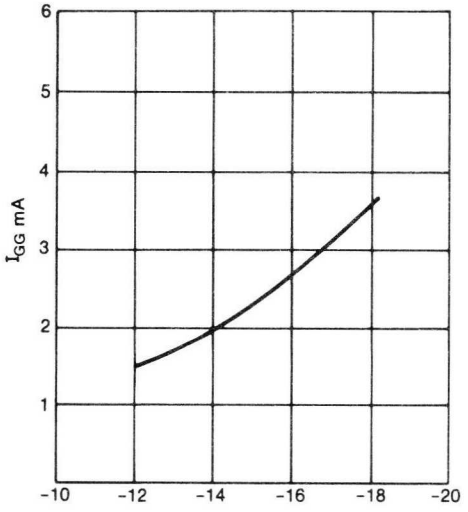
OUTPUT CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT CURRENT vs. TEMPERATURE



NORMALIZED OUTPUT CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

4¾ Digit Multi-Meter / Counter

FEATURES

- 4¾ digit display (±29,999 max. reading)
- 6 range autoranging
- Autozero, auto polarity
- Direct LED 7 segment drive
- Leading zero blanking/overrange blinking
- Multiplexed BCD output
- Single power supply
- On chip clock
- 20,000, 29,999 or freerun counter mode.

DESCRIPTION

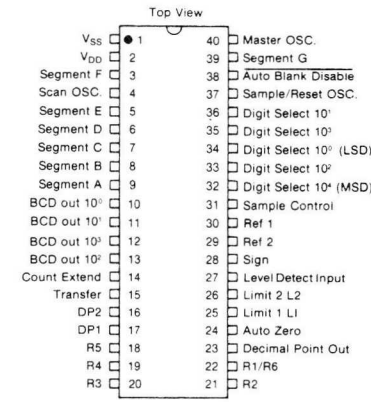
The AY-3-3550 contains all the logic for a 4¾ digit DMM (±29,999 maximum reading) incorporating dual ramp integration. Outstanding features of this "state-of-the-art" DMM chip include 6 range autoranging, autozero, auto polarity, direct 7-segment LED drive, and multiplexed BCD outputs. An on-chip oscillator controls the sampling rate, digit select multiplexing and BCD counting.

Fabricated in GI's advanced N-channel Ion Implant process to enable operation from a single power supply (+4.5V to +11V), the AY-3-3550 typically draws only 12mA when operating at +5V.

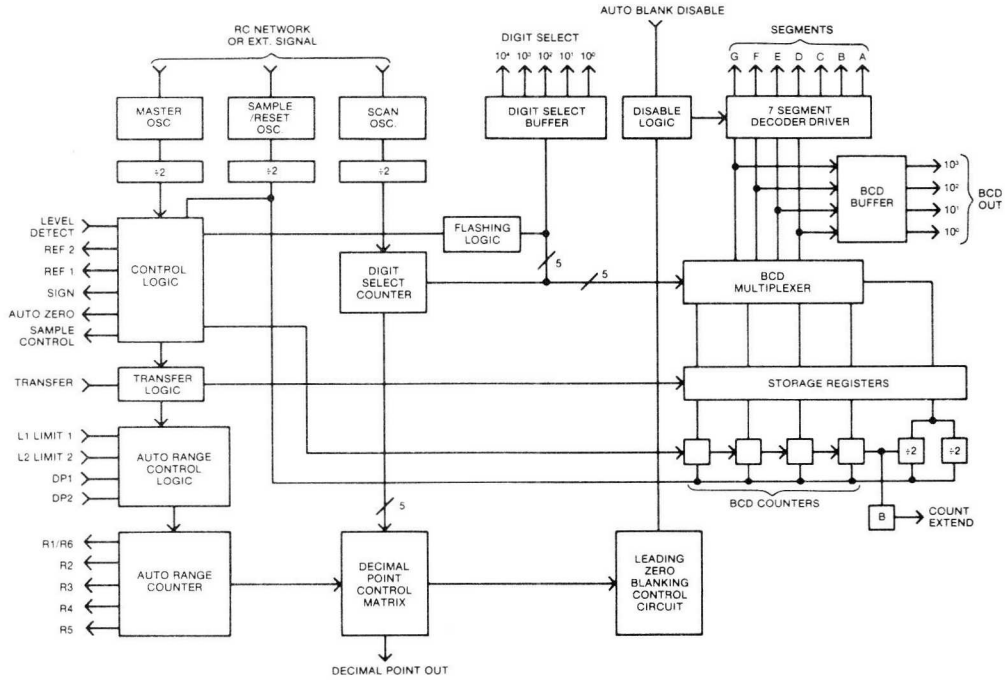
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



Functional Description

Operation

(Refer to Figs. 1 and 2 and the Block Diagram). An input on the Sample/Reset OSC Input triggers the internal reset signal which in turn resets the internal BCD synchronous counters, synchronizes the master clock with the control signals and simultaneously activates the 10^4 Multiplex output. At the first master clock following the trailing edge of the internal reset, the "Sample Control" signal is activated. This signal opens the switch in the analog section to integrate the unknown input voltage. After 10,000 internal clocks, the "Sample Control" signal is deactivated and either Ref SW1 or Ref SW2 activates depending upon the comparator logic level. This in turn switches the integrator to the opposite polarity source. Compared to the unknown input voltage, the integrator capacitor is discharged until the output voltage reaches the comparator threshold value. This variable time is proportional to the unknown voltage. The Comparator input voltage change at this time stops the internal counter and internally produces a transfer pulse to store the measured count. The storage registers are fed to the BCD multiplexer which is controlled by a digit select counter. According to the multiplexing sequence, the seven segment information and BCD data are made available at the Seven Segment and BCD Output pins. Note that the Autozero signal is deactivated during the counting cycle. Also, the correct polarity signal Sign Output is available when either of the reference switches are activated.

Transfer Logic and Timing

BCD data in the decade counter is transferred to the storage registers by means of an active Comparator Input. BCD data can also be transferred to the latches under the control of the Transfer Input signal.

The Transfer signal at its active (high) state causes a continuous transfer and display mode; or it can be pulsed to transfer on command. The Transfer signal in its active state also triggers the auto-range up-down counter whose function is determined by its control logic. The internal transfer pulse is superseded by an external signal applied at the Transfer Input. The Transfer signal in its active state also blanks the Decimal Point Output.

Scan OSC. Logic and Timing

The digit select counter and decoder is edge-triggered from either a signal applied at the Scan OSC. Input or from the output of the internal scan oscillator. The frequency of the internal oscillator is controlled by an RC network tied at this input. The digit select counter is set to the MSD position by a reset signal. Each of the five digit select line outputs is sequentially activated (low) when the corresponding digit is selected. The internal synchronization logic is incorporated to ensure that both the seven segment and BCD data from the selected latch are valid prior to enabling the corresponding Digit Select Output.

Sample/Reset OSC.

An input pulse on this pin activates an internal one-shot which resets the BCD decade counter and forces the digit select counter to the MSD position. This reset pulse also synchronizes the master oscillator frequency to control the logic outputs and BCD counters. An RC network tied to this input causes the internal oscillator to function at the frequency selected.

Leading Zero Blanking and Decimal Point Control

At the start of each MSD to LSD scan cycle, a blanking of leading zeros occurs until the decimal point active state is clocked. Any number following a decimal point is displayed. Leading zero blanking does not affect the BCD outputs and the 10^1 and 10^0 digits in the display. This feature allows the chip to work as a 3¾ DMM. Leading zero blanking is inhibited whenever the Auto Blank Disable is tied to an active (low) level.

Autoranging

The autorange up-down counter is edge triggered by a transfer pulse (internal or external) in conjunction with the associated control logic. The autorange counter is decoded into one of the five output signals through buffers R1 thru R5. Range R1 acts a R6 when the DP2 control signal is zero.

Down Ranging

If the display count is less than 1800, the autorange counter is downranging, except in the resistance range (Function 2). When in this mode, the counter is upranging. Between count 1800 and 20,000, no autorange movement occurs. At 20,000 or above the counter upranges except in the resistance range when the counter downranges. Depending upon the state of the Limit 1 and Limit 2 control signals, the scale length could be 20,000, 29,999 or free run.

Flashing Logic

The MSD digit flashes when the count is above 20,000 and the chip is in scale length 29,999 (L2=1,L1=0). If leading zero blanking is not disabled in this mode, all digits except MSD are blanked out and the MSD flashes indicating an overrange situation in the highest possible range. This feature prevents current drain through the segments in an overflow condition.

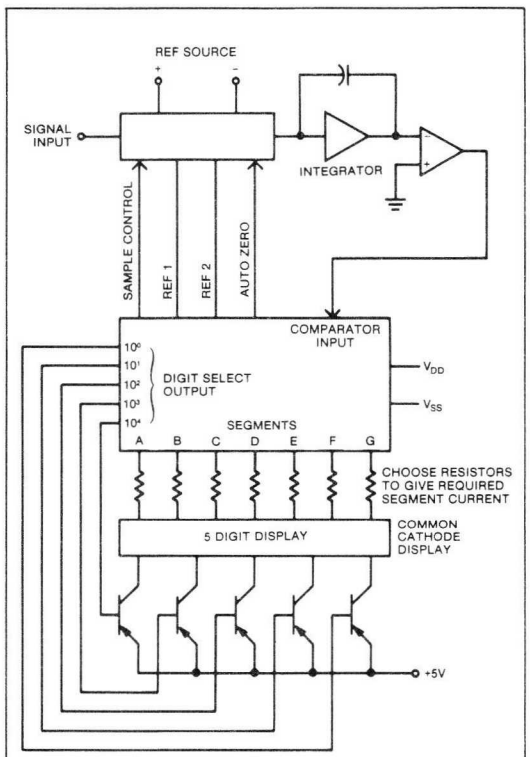
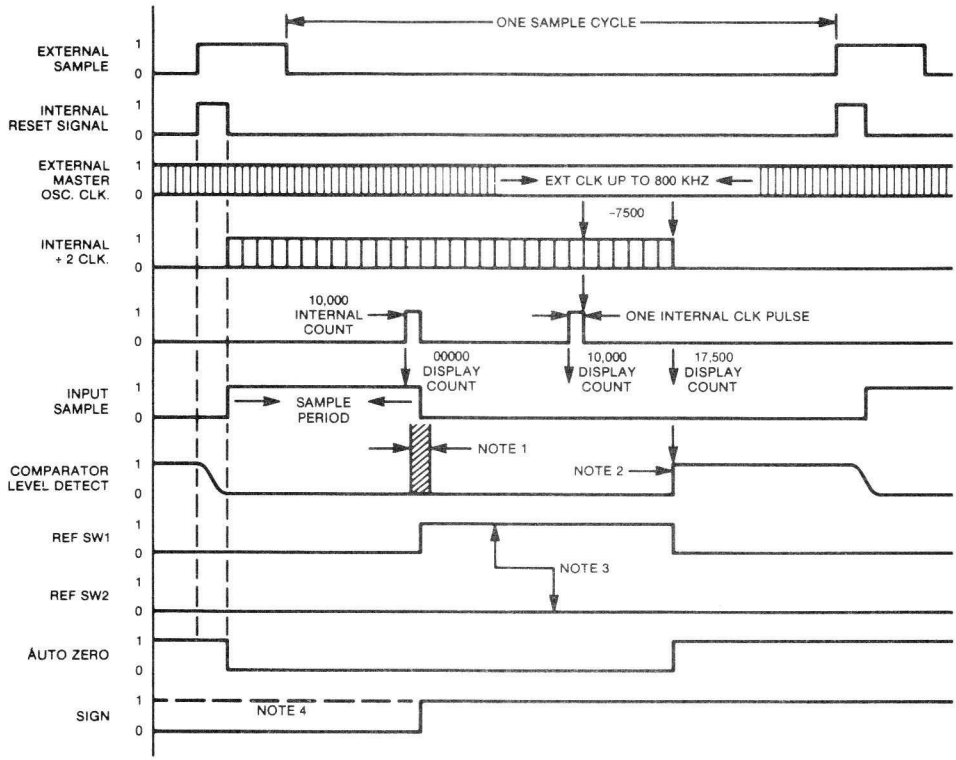


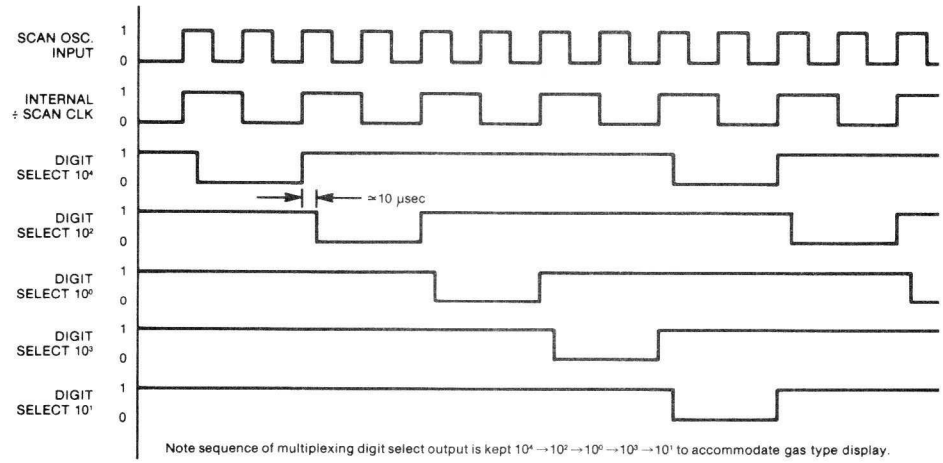
Fig.1 DIAGRAM SHOWING DISPLAY CONNECTION AND CONTROL INPUT TO ANALOG SECTION.

TIMING DIAGRAMS



NOTE:
1) During the shaded area, the comparator level DETECT INPUT should be well defined and no noise should be allowed at the input.
2) The comparator change is determined by the EXTERNAL CIRCUIT at this point. The count in the counter is proportional to the input measuring voltage.
3) The waveform of REF1 and REF2 would be reversed if the comparator level is in the opposite state.
4) Polarity would be reversed if the comparator input is reversed.

Fig.2 TIMING DIAGRAM OF CONTROL SIGNAL FOR ONE SAMPLE CYCLE



Note sequence of multiplexing digit select output is kept $10^4 \rightarrow 10^2 \rightarrow 10^0 \rightarrow 10^3 \rightarrow 10^1$ to accommodate gas type display.

Fig.3 SCAN CLOCK INPUT AND MULTIPLEXING DIGIT SELECT OUTPUT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3V
Storage Temperature ..... -55° C to 150° C
Operating Temperature ..... 0° C to +70° C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

Operating Temperature (T_A) = +25° C
V_{SS} = 0.0V
V_{DD} = +4.5V to +11V

Parameters	Min	Typ	Max	Units	Conditions
Clocks input voltage low	0.0	—	0.7	V	
Clocks input voltage high					
Pin No. 4,40	V_{DD}-1.0	—	V_{DD}	V	
Pin No. 37	V_{DD}+1.0	—	V_{DD}	V	
Master Clk Freq.	DC	(Internal)	400	kHz	From 0° C to 70° C } NOTE 1
Scan Clk Freq.	DC	(Internal)	10	kHz	From 0° C to 70° C } NOTE 1
Sample Clk Freq.	DC	(Internal)	100	Hz	From 0° C to 70° C } NOTE 1
Comparator input voltage HI	3.0	2.6	V_{DD}	V	At V_{DD} = 5V
Comparator input voltage LO	V_{SS}	2.0	2.5	V	At V_{DD} = 5V
Group A					
Input Logic Level HI	V_{DD} -1.0	—	V_{DD}	V	Input Resistance = 100KΩ
Input Logic Level LO	V_{SS}	—	V_{SS} +0.7	V	
Group 2 & 3					
Output Logic Level HI	V_{DD} -1.2	—	V_{DD}	V	At 40μA (V_{DD} = 5V)
Output Logic Level LO	V_{SS}	—	V_{SS} +0.5	V	At 2.0mA
Group 4					
Output Logic Level HI	V_{DD} -1.0	—	V_{DD}	V	At 40μA (V_{DD} = 5V)
Output Logic Level LO	V_{SS}	—	V_{SS} +0.4	V	At 100μA
Group 1					
Output Logic Level HI	V_{DD} -1.2	—	V_{DD}	V	V_{DD} = 5V
Output Logic Level LO	V_{SS}	—	V_{SS} +1.2	V	V_{DD} = 5V @ 1mA
For REF1, REF2, Sample Control, Autozero & Clk Extend					
Output Rise Time	—	—	5.0	μs	V_{DD} = 5V
Output Fall Time	—	—	5.0	μs	
Supply Current	—	—	12	mA	@ V_{DD} = 4V, V_{SS} = 0V, Input Freq = 300 KHz

Pin Numbers

Group A = 15, 16, 17, 25, 26, 38
Group 1 = 3, 5, 6, 7, 8, 9, 23, 28, 29
Group 2 & 3 = 10, 11, 12, 13, 14, 32, 33, 34, 35, 36
Group 4 = 18, 29, 20, 21, 22, 24, 27, 30, 31

NOTE 1:
Master Clock Oscillator:
R = 25K to V_{DD}, C = 100 pF to V_{SS}
Scan Clock Oscillator:
R = 100K to V_{DD}, C = .001μF to V_{SS}
Sample Clock Oscillator:
R = 1 Meg to V_{DD}, C = .01μ F to V_{SS}

Fig.4 TRUTH TABLE FOR DECIMAL POINT AND AUTORANGE FUNCTIONS

Auto Range	Function 1 (ACV. DCV.)		Function 2 (Resistance)		Function 3 (Current)		Function 4	
	DP1	DP2	DP1	DP2	DP1	DP2	DP1	DP2
	0	1	1	0	0	0	1	1
R1	A		*		*		D	
R2	B		C		*		B	
R3	C		E		B		C	
R4	D		D		C		D	
R5	E		C		D		E	
R6	*		B		E		*	

NOTES:
1) *denotes illegal states.
2) RANGE 1 (R1) output = R1 when DP2 = 1; RANGE 1 OUTPUT acts as RANGE 6 OUTPUT when DP2 = 0.
3) When decimal point A is "ON", no blanking occurs.
4) DECIMAL POINT POSITION is shown in Fig.5 below.

MSD LSD

DIGIT SELECT				
10^4	10^3	10^2	10^1	10^0
2_i	9_i	9_i	9_i	9_i
B	C	D	E	A

POSITION OF DECIMAL POINT ON DISPLAY

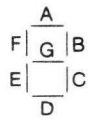
Fig.5

Scale Length	Condition		Leading Zero Blanking	Blinking MSD on Overrange
	L2	L1		
20,000	0	1	YES	NO
20,000	0	0	YES	NO
29,999	1	0	YES	YES, OVER 20,000 COUNTS
FREE RUN COULD BE USED AS FREQ. CTR.	1	1	NO	NO

Fig.6 SCALE LENGTH SELECT AND OVERFLOW CONDITION TABLE

DECIMAL **7-SEGMENT** **BCD**

	A	B	C	D	E	F	G		2^0	2^1	2^2	2^3
0	0	0	0	0	0	0	1		0	0	0	0
1	1	0	0	1	1	1	1		1	0	0	0
2	0	0	1	0	0	1	0		0	1	0	0
3	0	0	0	0	1	1	0		1	1	0	0
4	1	0	0	1	1	0	0		0	0	1	0
5	0	1	0	0	1	0	0		1	0	1	0
6	0	1	0	0	0	0	0		0	1	1	0
7	0	0	0	1	1	1	1		1	1	1	0
8	0	0	0	0	0	0	0		0	0	0	1
9	0	0	0	0	1	0	0		1	0	0	1



NOTE:
Logic "0" = Low Segment "ON"
Logic "1" = High Segment "OFF"

Fig.7 Seven segment and BCD output truth table.

AY-5-4007
AY-5-4007A
AY-5-4007D

Four Digit Counter / Display Drivers

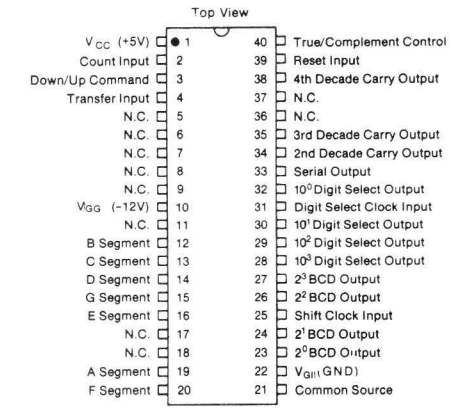
FEATURES

- Minimum interface required to drive most common types of LED, fluorescent, seven segment displays.
- Large output current capability on seven segment outputs, typically 25mA with 1V drop.
- Fully synchronous up/down counting operation.
- Look ahead carry for error free outputs when reversing count direction.
- Internal oscillator needing no external components for operating the digit select counter.
- Four digit select outputs with inversion control for display driving flexibility.
- Multiplexed BCD outputs and serial output from storage register is available.
- TTL/DTL compatible on inputs and outputs.
- Blanking action of Reset Input.
- Counting rate up to 600 kHz.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-5-4007A

Top View



DESCRIPTION

The Four Digit Counter Display Driver is an LSI subsystem designed for application in counting display systems such as frequency counters, digital voltmeters, digital timers, event counters using 7 segment numeric displays. It contains a 4 decade up/down synchronous BCD counter, a storage register, multiplexing circuits, internal oscillator for digit selection and 7 segment decoder to count and display up to 9999.

Built-in control circuits provide flexibility of use with a minimum of external components.

The device is constructed on a single monolithic chip using MTNS P-channel enhancement mode transistors.

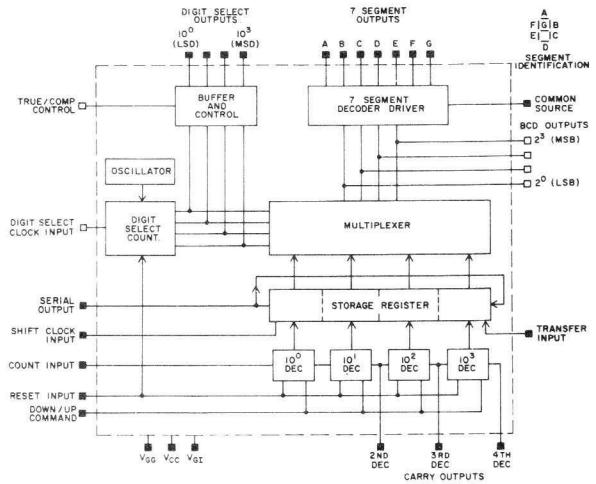
AY-5-4007A, Available in 40 Lead Dual In Line package, allows for all available functions.

The AY-5-4007 and AY-5-4007D incorporate the most commonly used features in 24 Lead Dual In Line packages.

BLOCK DIAGRAM

AY-5-4007A shown:

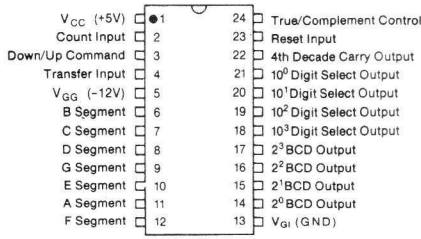
■ indicates functions available with the AY-5-4007D.



PIN CONFIGURATIONS

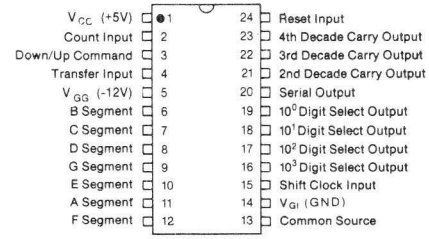
24 LEAD DUAL IN LINE
AY-5-4007

Top View



24 LEAD DUAL IN LINE
AY-5-4007D

Top View



NOTE: For AY-5-4007D, True/Complement control is internally connected to logic "0" level.

PIN FUNCTIONS

Name	Function
COUNT INPUT	Count Input operates the decade counters synchronously on the positive going edges (logic '0' to '1' transitions).
RESET INPUT	When this input goes to a logic '1' it resets the decade counters to 0000, forces the digit select counter to the MSD position and the Digit Select Outputs to 'not active' logic levels to blank the display. It must be present for a minimum of 10 μsec.
DOWN/UP COMMAND	The count direction depends upon the logic level on the DOWN/UP Command input. Logic '0' = Count UP. Logic '1' = Count DOWN.
2ND DECADE CARRY OUTPUT **3RD DECADE CARRY OUTPUT** **4TH DECADE CARRY OUTPUT**	Normally the Carry Outputs are at a logic '0' level; when activated a positive pulse is generated on the output line, which is identical with the Count Input causing the carry.
TRANSFER INPUT	Placing the Transfer Input at a logic '1' allows transfer of data from the decade counters to the storage register.
SHIFT CLOCK INPUT	This input is used to apply clock pulses to the storage register for serial shift operation. Normally Shift Clock is maintained at a Logic '1' and negative pulses are necessary to perform shift operation. Actual shifting of storage register data is done on the second edge (positive going) of each clock pulse. A Pull-up resistor is internally provided for the Shift Clock Input so that this line, if not used, may be left floating. Since the storage register is quasi-static in serial shift operation the width of negative pulses (at logic '0') has to be limited to 20μsec. During serial shift operation the Transfer Input must be at a logic '0'.
SERIAL OUTPUT	This is the serial output of the storage register. When serial shift operation is not performed the Serial Output is the least significant bit of the least significant digit of the storage register.
10^0 DIGIT SELECT OUTPUT (LSD) **10^1 DIGIT SELECT OUTPUT** **10^2 DIGIT SELECT OUTPUT** **10^3 DIGIT SELECT OUTPUT (MSD)**	These outputs provide sequentially an active logic level (logic '1' if the True/Complement Control is at a logic '1'; logic '0' if the True/Comlement Control is at a logic '0'), to specify which of the corresponding digits is selected and displayed, the remaining 3 Outputs being 'not active'. All the Digit Select Outputs are forced to a 'not active' logic level as long as the Reset Input is active
2^0 BCD OUTPUT(LSB) **2^1 BCD OUTPUT** **2^2 BCD OUTPUT** **2^3 BCD OUTPUT(MSB)**	These outputs provide the Binary Coded Decimal representation of the digit being selected and displayed by the multiplexer. The truth table shows BCD Codification of these outputs.
"A" TO "G" SEGMENT	These outputs are programmed according to the truth table. Each output terminal is actually connected to the drain of the corresponding output transistor.
COMMON SOURCE	This is the common of the seven segment output transistors. When not externally available the corresponding terminal is internally tied to VGI (0V) line. It may be connected to any voltage between VSS and VDD according to requirements.
TRUE/COMPLEMENT CONTROL	This input controls the polarity of the Digit Select Outputs active logic level. When the TRUE/COMPLEMENT Control is at a logic '1', active level for the Digit Select Outputs is a logic '1', when at a logic '0' active level is a logic '0'.
DIGIT SELECT CLOCK INPUT	An external signal applied to this terminal overrides the internal oscillator. When the internal oscillator is used, this terminal must be left floating.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC} . . . . . −20 to +0.3V
Storage temperature range . . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of thse devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

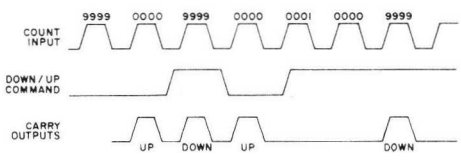
V_{CC} = +5.0 ±0.5V V_{GG} = −12V ±1V OR −7.0V ±0.5V
V_{GI} = 0V Operating Temperature (T_A) 0°C to +70°C

	V_{GG} = −12V ±1V			V_{GG} = −7V ±0.5V				
Characteristic	**Min**	**Typ****	**Max**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Inputs								
Logic '0'	V_{GG}	-	+0.8	V_{GG}	-	+0.8	Volts	See Fig. 4.
Logic '1'	V_{CC} −1.5	-	V_{CC} +0.3	V_{CC} −1.5	-	V_{CC} +0.3	Volts	
Capacitance	-	-	10.0	-	-	10.0	pF	V_{IN} = V_{CC} f=1MHz
Leakage	-	-	5.0	-	-	5.0	µA	V_{IN} −V_{CC} = −10V at 25°C
Repetition Rate	D.C.	-	600	D.C.	-	350	kHz	Square Wave
Pulse Width	0.7	-	-	1.0	-	-	µsec	Pulse either high or low
Tr & Tf	-	-	100			100	µsec	
True/Complement/ Control Input								
Input Current	10	40	100	10	-	50	µA	V_{IN} = V_{CC}
	10	25	50	10	-	25	µA	V_{IN} = V_{GI} See Fig. 5
Digit Select Clock								
Input Current	10	60	150	5	25	75	µA	V_{IN} = V_{CC} (Sink)
	50	250	1600	50	150	1000	µA	V_{IN} = V_{GI} (Source) See Fig. 3.
Internal Freq.	1.0	2.0	4.0	1.0	2.0	4.0	kHz	
External Freq.—Data only	D.C.	-	100	D.C.	-	50	kHz	
Display	D.C.	-	15	D.C.	-	7	kHz	Display Duty Cycle 25%
Shift Clock								
Frequency	D.C.	-	1	D.C.	-	0.8	MHz	
Pulse Width	0.4	-	1000	0.5	-	1000	µsec	See functional description
Input Current	20	100	400	10	30	200	µA	V_{IN} = V_{GI} (See Fig. 6)
Outputs—7 Segment (See Note 2)								
Leakage Current	-	-	10	-	-	10	µA	V_{OUT}—V_{CC} = −10V at 25°C
Device on Current	15	25	45	12	20	35	mA	V_{CS}—V_{OUT} = +1.0V at 25°C, V_{CS} = V_{CC}
Device on Current	12	18	27	7	11	17	mA	V_{CS}—V_{OUT} = −1.0V at 25°C, V_{CS} = V_{GI}
Power Dissipation (per segment at 25°C)	-	-	200	-	-	200	mW	See Note 1 & Fig. 1
Other Outputs								
Logic '0'	-	0.2	0.4	-	0.3	0.4	Volts	I_{OL} = 1.6mA with 10pF load
Logic '1'	V_{CC} −1.0	V_{CC} −0.65	-	V_{CC} −1.0	V_{CC} −0.65	-	Volts	I_{OL} = 50µA
Propagation Delay	-	-	1.0	-	-	1.5	µsec	Carry Output } See Fig. 2
			1.5	-	-	2.0	µsec	Serial Output }
Tr, Tf Rise, Fall Times	-	0.15	0.3	-	0.3	0.6	µsec	
Power I_{GG}	-	25	40	-	13	20	mA	(V_{CC} to V_{GG})

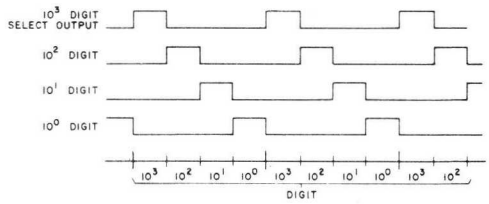
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Derate Power Linearly to 100mW at 70°C.
2. See also Typical 7-Segment Output Curves, Figs.9, 11, & 13 (−12V ±1V)
   See also Typical 7-Segment Output Curves, Figs.10, 12, & 14 (−7V ±0.5V)

TIMING DIAGRAMS



CARRY OPERATION



DIGIT SELECT OPERATION
(True/Complement Control is at logic '1' level)

OPERATION

Decade Counters

The four decade counters are synchronously operated on the positive going edges of the Count Input; a single DOWN/UP Command controls the direction of counting. The edge-triggered structure of the master-slave flip-flops allows the count direction to be changed between count pulses at either Count Input level. A Reset Input resets decade counters to 0000.

Carry outputs are provided at the 2nd, 3rd and 4th decade; these outputs are activated when an overflow (in counting up) or an underflow (in counting down) condition exists in the corresponding decade counter. The carry output pulse is the same as the Count Input pulse causing the carry.

The look ahead design of the carry stages gives error free outputs when reversing the count direction.

Storage Register

Data in the decade counters is transferred to the storage register under control of the Transfer Input signal. The Transfer Input may be connected to a logic '1' for a continuous transfer and display operation.

The Storage register may also be operated as a parallel-in serial-out shift register. In this case clock pulses are to be provided to Shift Clock Input, the serial content of storage register is available on the Serial Output line, and recirculated back to the first stage input. A train of 16 clock pulses is needed to extract the full content of the register, least significant bit of least significant digit first. When operating the storage register serially, Transfer input is to be kept at a logic '0'.

Digit Select Counter and Multiplexer

The digit select counter is driven by a built in oscillator which requires no external components. The internal oscillator can be overridden by applying an external signal to the Digit Select Clock Input.

The digit select counter controls the multiplexer to route information from storage register to the 7 segment decoder drivers and to the BCD Outputs.

The counter scans from MSD (10^3 digit) to LSD (10^0 digit). Each of the four Digit Select Outputs is sequentially activated when the corresponding digit is selected and displayed.

The Digit Select counter is forced to MSD position and Digit Select Outputs are forced to 'not-active' logic levels as long as Reset Input is active. This feature blanks the display when the device is being reset. The True/Complement Control inverts the Digit Select Outputs active logic level for flexibility of output interface circuitry.

Internal delay logic ensures that both 7 segment outputs and BCD outputs are valid before activation of the corresponding Digit Select Output to avoid "ghost images".

7 Segment Decoder Driver

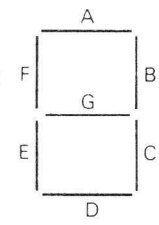
The 7 segment decoder drivers consist of very low impedance output transistors (typically 40 ohms) to minimize external interface components when driving 7 segment displays such as LEDs, fluorescents, incandescents, etc.

The 7 Segment Outputs are the drains of the corresponding output transistors, these outputs are programmed according to the truth table below. A Common Source terminal is also available to increase flexibility of use.

DIGIT	7 SEGMENT OUTPUT TRANSISTOR							BCD OUTPUT			
	A	B	C	D	E	F	G	MSB 2^3	2^2	2^1	LSB 2^0
0	*	*	*	*	*	*	–	0	0	0	0
1	–	*	*	–	–	–	–	0	0	0	1
2	*	*	–	*	*	–	*	0	0	1	0
3	*	*	*	*	–	–	*	0	0	1	1
4	–	*	*	–	–	*	*	0	1	0	0
5	*	–	*	*	–	*	*	0	1	0	1
6	*	–	*	*	*	*	*	0	1	1	0
7	*	*	*	–	–	–	–	0	1	1	1
8	*	*	*	*	*	*	*	1	0	0	0
9	*	*	*	*	–	*	*	1	0	0	1

LEGEND:
* output transistor ON
– output transistor OFF
0 logic '0'
1 logic '1'

SEGMENT IDENTIFICATION



7 SEGMENT AND BCD OUTPUTS TRUTH TABLE

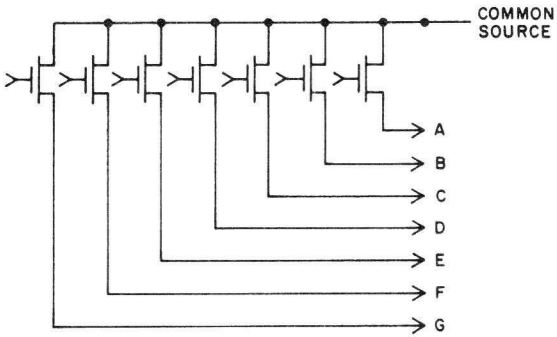


Fig.1 7-SEGMENT OUTPUTS

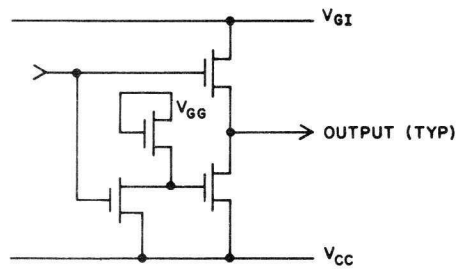


Fig.2 ALL OTHER OUTPUTS

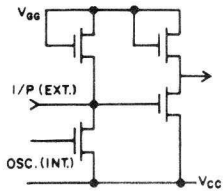


Fig.3 DIGIT SELECT CLOCK INPUT

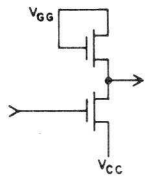


Fig.4 TYPICAL INPUT

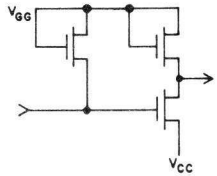


Fig.5 TRUE/COMPLEMENT INPUT

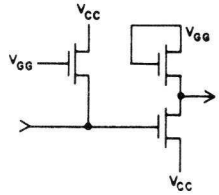


Fig.6 SHIFT CLOCK INPUT

CIRCUIT DIAGRAMS

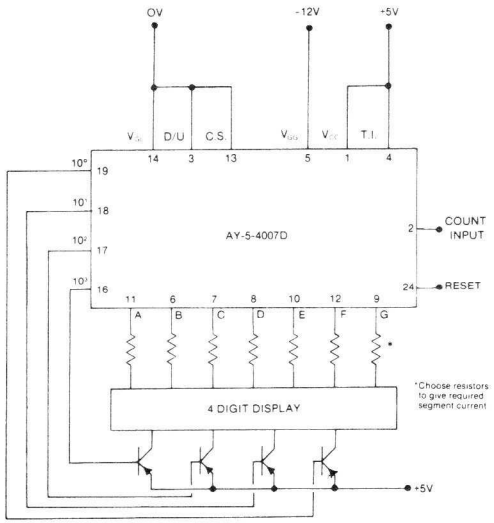


Fig.7 COMMON CATHODE LED DISPLAY

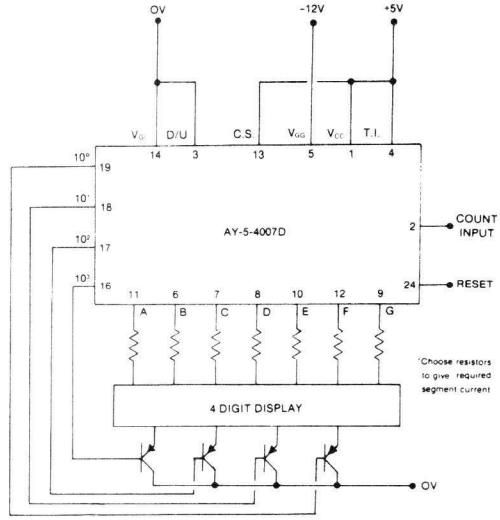


Fig.8 COMMON ANODE LED DISPLAY

TYPICAL CHARACTERISTIC CURVES

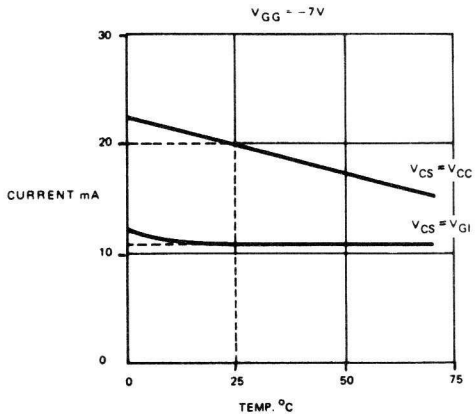


Fig.9

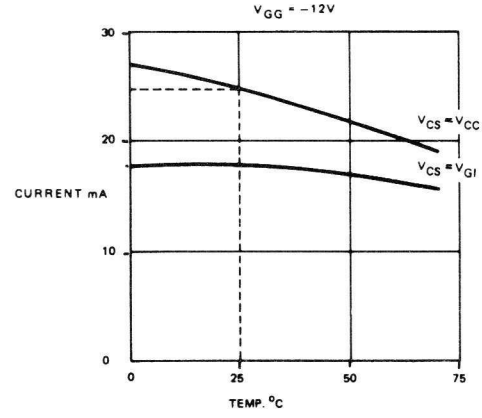


Fig.10

TYPICAL CURVES OF SEGMENT CURRENT VS. TEMPERATURE AT 1V ACROSS OUTPUT DEVICE

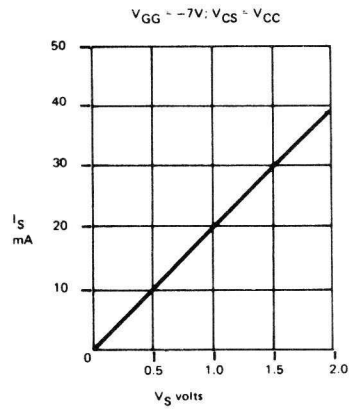


Fig.11

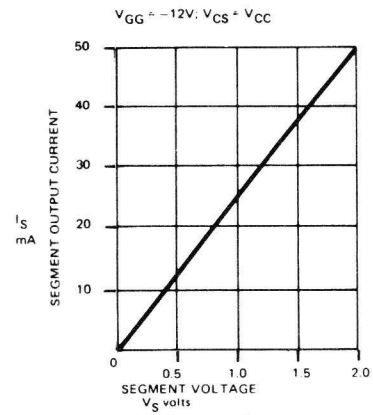


Fig.12

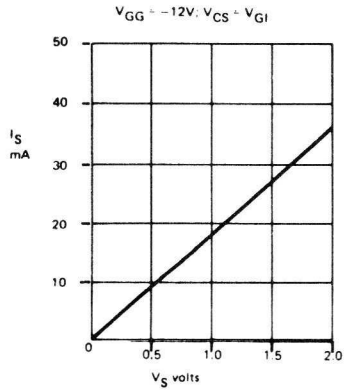


Fig.13

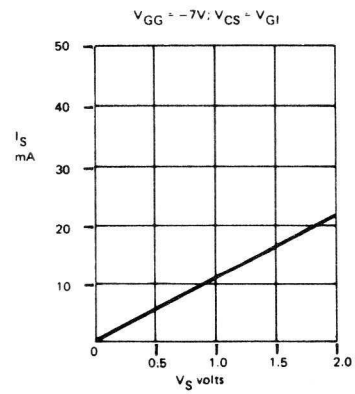


Fig.14

TYPICAL SEGMENT OUTPUT CURRENT V_S OUTPUT VOLTAGE AT +25°C

Four Digit Counter

FEATURES

- Fully static operation.
- Maximum clock input 500kHz.
- Reset input.
- Multiplexed outputs.
- Final Carry output and two intermediate carry outputs.
- TTL/DTL compatible inputs and outputs.

DESCRIPTION

The AY-5-4057 is a fully static four digit counter capable of accepting a count frequency of up to 500kHz. The four counters are connected in series, each having a 4-bit store associated with it. The counters change on the negative going clock transition, and the counter outputs are transferred to the 4-bit stores when the load control is taken to Logic '0'.

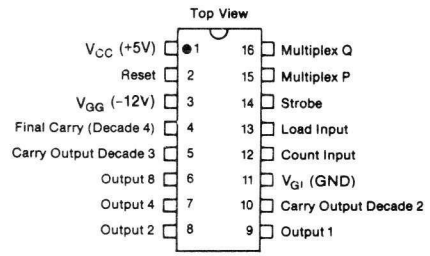
The count held in the four stores is strobed out in sequence by a signal derived from the 'Strobe Input'. The multiplexed BCD outputs are output in sequence and are capable of driving a decoder/driver. The 'Strobe Input' operates on a positive transition (0 to 1), and the multiplex outputs, P and Q are in a 2-bit binary sequence.

In addition to the count outputs, the device has a 'Final Carry Output' (CO 4) and two intermediate carry outputs, CO2 and CO3, from the second and third decades respectively.

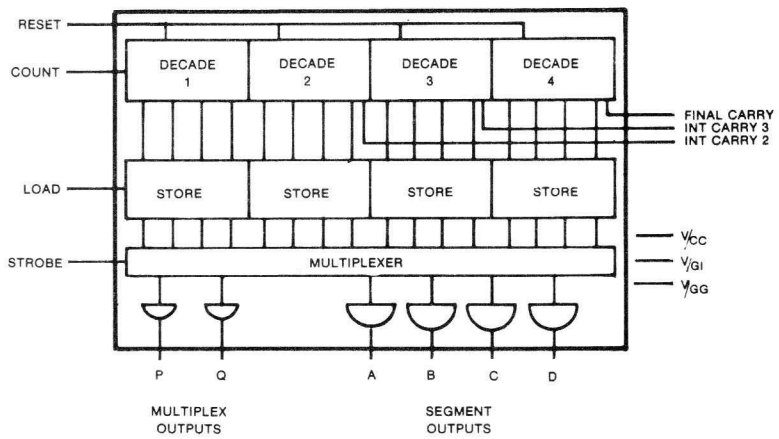
A reset line is provided to reset all four decades to the zero state.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM

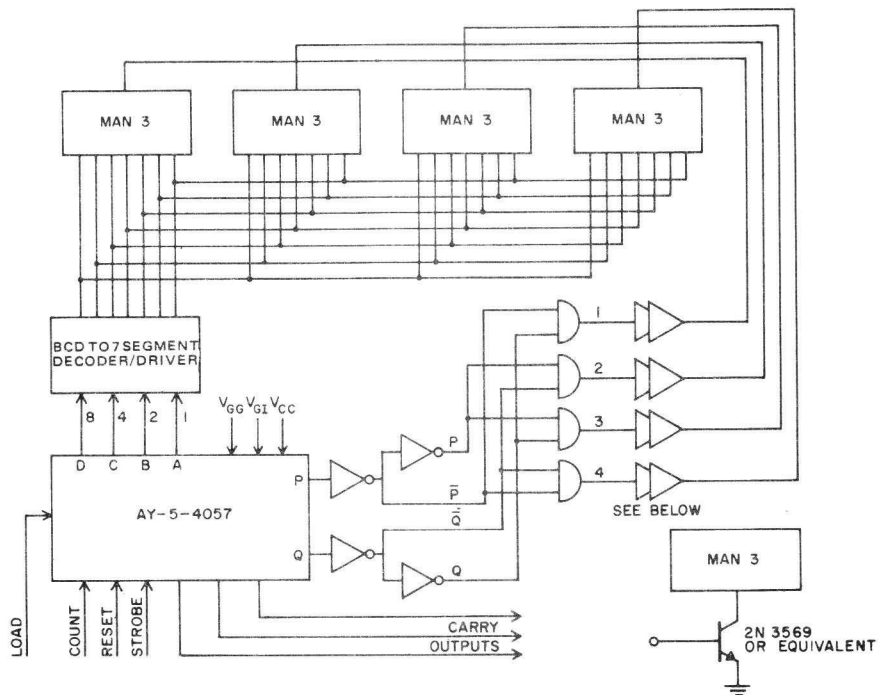


PIN FUNCTIONS

Name	Functions
COUNT INPUT	A negative going (1 to 0) signal on this input causes the counter to be incremented by one.
LOAD INPUT	A logic '0' level on this input causes the contents of the four counters to be transferred to the store. To store any one count, the load input must go to logic '0' a minimum of 800 nsec after the count pulse that sets up the count to be stored. (ts1 on timing diagram) and stay at logic '0' for a minimum of 1 μsec.
RESET	A logic '1' level applied to this input will reset all four counters to the all '0's state. (Store is not reset). A delay of 250 nsec must be allowed (ts2 of timing/diagram) after the reset goes to logic '0' before a count is started.
STROBE	A positive going ('0' to '1') signal on this input clocks the multiplex counter, thereby causing the count to be output in the correct sequence.
P & Q OUTPUTS	The two Multiplex outputs P and Q, identify which decade is being output. P Q 1 0 Strobes decade 1 0 1 Strobes decade 2 1 1 Strobes decade 3 0 0 Strobes decade 4
***INTERMEDIATE CARRY (CO2)**	This output is generated by the second decade of the counter.
***INTERMEDIATE CARRY (CO3)**	This output is generated by the third decade of the counter.
***FINAL CARRY**	This output is generated by the fourth decade of the counter.

*All carry outputs go to logic '1' on count 8 and return to logic '0' on count 10.

COUNTER-DISPLAY INTERFACE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Max. voltage between V_{CC} and any pin. . . . . −20V to 0.3V
Operating Temperature Range. . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

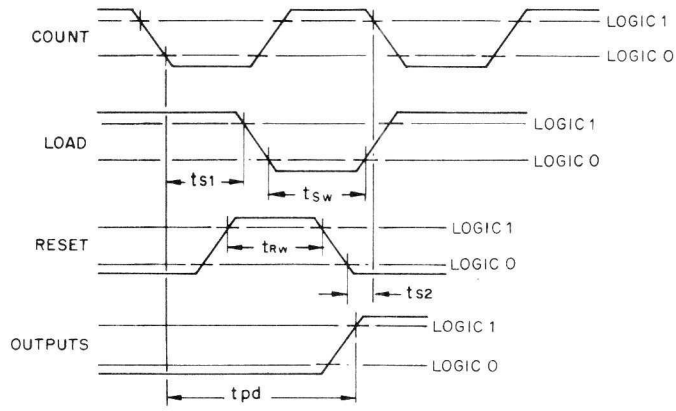
Standard Conditions (unless otherwise noted)

$V_{GG} = -12V \pm 1V$
$V_{CC} = +5.0 \pm 0.5V$
$V_{GI} = OV$

Operating Temperature (T_A) = 0°C to +70°C
Output Loading + 1 TTL Load
CL TOTAL = 10 pF

Characteristic	Min	Max	Units	Conditions
Count Input				
Repetition Rate	DC	500	kHz	
Rise/Fall Times	—	10	μs	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	5	pF	$V_{IN}=V_{CC}$
Load Input				
Pulse Width t_{SW}	1.0	—	μs	
Set-up Time ts1	800	—	ns	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	10	pF	$V_{IN}=V_{CC}$
Strobe Input				
Repetition Rate	DC	10	kHz	
Pulse Width	10	—	μs	
Rise/Fall Times	—	10	μs	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	5.0	pF	$V_{IN}=V_{CC}$
Reset Input				
Pulse width t_{RW}	1	—	μs	
Set-up-Time ts2	250	—	ns	
Logic '0'	—	+0.4	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	10	pF	
Outputs				
Logic '0'	—	+0.4	V	$I_{OL}=1.6mA$
Logic '1'	V_{CC}−1.0	—	V	$I_{OH}=100\mu A$
Propagation delay tpd	—	2.0	μs	
Input Leakage	—	5.0	μA	$V_{in}=V_{CC}$−10V. at 25°C
Power	—	350	mW	

TIMING DIAGRAM



MICRO ELECTRONICS

MOSFET TRANSISTORS

TYPE	PART NUMBER	PAGE NUMBER	PART NUMBER	PAGE NUMBER
P-CHANNEL ENHANCEMENT MODE	MEM511	9-34	MEM560C	9-62
	MEM511A	9-36	MEM561	9-64
	MEM511C	9-38	MEM561C	9-64
	MEM517	9-40	MEM806	9-112
	MEM517A	9-42	MEM806A	9-112
	MEM517C	9-44	MEM807	9-114
	MEM520	9-46	MEM807A	9-114
	MEM520C	9-48	MEM814	9-116
	MEM556	9-56	MEM816	9-118
	MEM556C	9-56	MEM817	9-119
	MEM560	9-62	MEM823	9-120
DUAL P-CHANNEL ENHANCEMENT MODE	MEM550	9-50	MEM954A	9-121
	MEM550C	9-50	MEM954B	9-121
	MEM551	9-50	MEM955	9-121
	MEM551C	9-50	MEM955A	9-121
	MEM954	9-121	MEM955B	9-121
N-CHANNEL ENHANCEMENT MODE	MEM562	9-66	MEM711	9-106
	MEM562C	9-66	MEM712	9-108
	MEM563	9-68	MEM712A	9-108
	MEM563C	9-68	MEM713	9-110
N-CHANNEL DEPLETION MODE	MEM554	9-52	MEM632	9-84
	MEM554C	9-54	MEM636	9-88
	MEM557	9-58	MEM637	9-88
	MEM557C	9-60	MEM638	9-88
	MEM564C	9-70	MEM639	9-92
	MEM571C	9-72	MEM655	9-94
	MEM610	9-74	MEM660	9-96
	MEM614	9-76	MEM667	9-98
	MEM616	9-78	MEM670	9-99
	MEM617	9-78	MEM680	9-100
	MEM618	9-78	MEM681	9-100
	MEM619	9-82	MEM682	9-100
	MEM630	9-84	MEM683	9-104
	MEM631	9-84		

In addition to the MOSFET products detailed on the following pages, GI offers a selection of JEDEC registered 2N and 3N type MOSFETs — contact factory for details.

2N3608	3N128	3N157A	3N176	3N202
2N3609	3N138	3N158	3N177	3N203
2N4038	3N139	3N158A	3N178	3N203A
2N4065	3N141	3N159	3N179	3N204
2N4066	3N142	3N160	3N180	3N205
2N4067	3N143	3N161	3N181	3N206
2N4351	3N145	3N162	3N182	3N207
2N4352	3N146	3N163	3N183	3N208
2N4353	3N147	3N164	3N184	3N211
	3N148	3N165	3N185	3N212
	3N149	3N166	3N186	3N213
	3N150	3N167	3N187	3N214
	3N151	3N168	3N188	3N215
	3N152	3N169	3N189	3N216
	3N153	3N170	3N190	3N217
	3N154	3N171	3N191	3N218
	3N155	3N172	3N192	3N242
	3N155A	3N173	3N193	
	3N156	3N174	3N200	
	3N157	3N175	3N201	

MOSFET TRANSISTORS
Index/Selection Guide

TYPE	PART NUMBER	$BV_{DSS/GSS}$ VOLTS-MIN.	I_{GSSF} nA-TYP.	$V_{GS\ (th)}$ V-MIN/MAX.	$RDS_{(on)}$ OHMS-TYP.	CASE	PAGE NO.
P-CHANNEL ENHANCEMENT MODE	**MEM 511**	−30/−30	−0.05	−3/−6	150	TO-72	**9-34**
	MEM 511A	−30/−30	−0.5	−3/−6	300	TO-72	**9-36**
	MEM 511C	−25/−25	−0.05	−3/−6	150	TO-72	**9-38**
	MEM 517	−30/−25	−0.15	−2.5/−5	35	TO-33	**9-40**
	MEM 517A	−30/−25	−0.15	−2.5/−5	35	TO-5	**9-42**
	MEM 517C	−25/−25	−0.15	−2.5/−5	35	TO-33	**9-44**
	MEM 520	−30/−40	−0.03pA	−3/−6	150	TO-72	**9-46**
	MEM 520C	−25/−25	−0.1pA	−3/−6	150	TO-72	**9-48**
	MEM 556	−50/−50	−0.1	−3/−6	700	TO-72	**9-56**
	MEM 556C	−45/−45	−0.3	−3/−6	700	TO-72	**9-56**
	MEM 560	−35/−35	−0.1	−1.5/−3	100	TO-72	**9-62**
	MEM 560C	−30/−30	−0.2	−1/−3.5	175	TO-72	**9-62**
	MEM 561	−30/−50	−0.05pA	−1.5/−3	100	TO-72	**9-64**
	MEM 561C	−25/−40	−0.5pA	−1.5/−3	150	TO-72	**9-64**
	MEM 806	−40/−40	−0.1pA	−2/−5.5	150	TO-72	**9-112**
	MEM 806A	−40/−40	−0.05pA	−2/−5.5	150	TO-72	**9-112**
	MEM 807	−40/−40	−0.1	−2/−5.5	150	TO-72	**9-114**
	MEM 807A	−40/−40	−0.2	−2/−5.5	150	TO-72	**9-114**
	MEM 814	−35/−35	−0.1	−1.5/−3	80	TO-72	**9-116**
	MEM 816	−30/−30	−0.2	−2/−5	150	Plastic	**9-118**
	MEM 817	−45/±200	−0.05pA	−2.5/−5.5	150	TO-72	**9-119**
	MEM 823	−35/±200	−0.05pA	−2.5/−5.5	150	TO-18	**9-120**
TYPE		**BV_{DSS} VOLTS-MIN.**	**I_{GSSF} nA-TYP.**	**$V_{GS\ (th)}$ V-MIN/MAX.**	**$RDS_{(on)}$ OHMS-TYP.**	**CASE**	**PAGE NO.**
DUAL P-CHANNEL ENHANCEMENT MODE	**MEM 550**	−30	−0.1	−3/−6	250	TO-77	**9-50**
	MEM 550C	−25	−0.2	−3/−6	250	TO-77	**9-50**
	MEM 551	−30	−0.03pA	−3/−6	250	TO-77	**9-50**
	MEM 551C	−25	−1.0pA	−3/−6	250	TO-77	**9-50**
	MEM 954	−30	−0.03	−2/−5	100	TO-77	**9-121**
	MEM 954A	−30	−0.03	−2/−5	100	TO-77	**9-121**
	MEM 954B	−30	−0.03	−2/−5	100	TO-77	**9-121**
	MEM 955	−35	−0.02pA	−2/−5	100	TO-77	**9-121**
	MEM 955A	−35	−0.02pA	−2/−5	100	TO-77	**9-121**
	MEM 955B	−35	−0.02pA	−2/−5	100	TO-77	**9-121**
TYPE	**PART NUMBER**	**$BV_{DSS/GSS}$ VOLTS-MIN.**	**I_{GSSF} nA-TYP.**	**$V_{GS\ (th)}$ V-MIN/MAX.**	**RDS (on) OHMS-TYP.**	**CASE**	**PAGE NO.**
N-CHANNEL ENHANCEMENT MODE	**MEM 562**	20/±30	1.0pA	0.5/4	150	TO-72	**9-66**
	MEM 562C	20/±30	10pA	0.5/4	150	TO-72	**9-66**
	MEM 563	20/±30	1.0pA	0.5/4	40	TO-72	**9-68**
	MEM 563C	20/±30	10pA	0.5/4	50	TO-72	**9-68**
	MEM 711	25/±30	0.1	0.5/1.5	50	TO-72	**9-106**
	MEM 712	25/±30	.01	0.5/2	50	Plastic	**9-108**
	MEM 712A	30/±30	.01	0.5/2	30	Plastic	**9-108**
	MEM 713	20/±30	10pA	0.5/2	50	Plastic	**9-110**
TYPE	**PART NUMBER**	**$BV_{DSS/GSS}$ VOLTS-MIN.**	**I_{GSS} mA-TYP.**	**I_{GSS} nA-TYP.**	**$V_{GSS\ (off)}$ VOLTS-MAX.**	**CASE**	**PAGE NO.**
N-CHANNEL DEPLETION MODE	**MEM 554**	20/+5, −10	5	0.01	−1.5	TO-72	**9-52**
	MEM 554C	20/+5, −10	5	0.05	−1.5	TO-72	**9-54**
	MEM 557	20/±10	5	0.01	−4	TO-72	**9-58**
	MEM 557C	20/±10	5	0.05	−4	TO-72	**9-60**
	MEM 564C	20/±6	5	1.0	−1.5	TO-72	**9-70**
	MEM 571C	20/±6	4	±10	–	TO-72	**9-72**
	MEM 610	20/±6	10	–	−6	TO-72	**9-74**
	MEM 614	20/±6	5	1.0	−1	TO-72	**9-76**
	MEM 616	25/±6	10	20	−4	TO-72	**9-78**
	MEM 617	20/±6	6	20	−4	TO-72	**9-78**
	MEM 618	20/±6	10	20	−4	TO-72	**9-78**
	MEM 619	20/±6	15	20	−4	TO-72	**9-82**
	MEM 630	25/±6	6	20	−4/−2	Plastic	**9-84**
	MEM 631	25/±6	10	20	−4/−3	Plastic	**9-84**
	MEM 637	25/±6	6	20	−4/−2	Plastic	**9-84**
	MEM 636	20/±6	15	20	−4	Plastic	**9-88**
	MEM 637	20/±6	15	20	−4	Plastic	**9-88**
	MEM 638	20/±6	15	20	−4	Plastic	**9-88**
	MEM 639	20/±6	10	–	−6	Plastic	**9-92**
	MEM 655	20/±6	4	±10	−4	TO-72	**9-94**
	MEM 660	20/+30, −20	3	–	−4	TO-72	**9-96**
	MEM 667	20/±100	3	0.05pA	−4	TO-18	**9-98**
	MEM 670	20/±100	3	0.05pA	−4	TO-72	**9-99**
	MEM 680	25/±6	4/30	50	−4	TO-72	**9-100**
	MEM 681	25/±6	2/20	50	−4	TO-72	**9-100**
	MEM 682	25/±6	3/20	50	−4	TO-72	**9-100**
	MEM 683	20/±6	15	20	−4	TO-72	**9-104**

MOSFET TRANSISTORS
Cross-Reference Guide

Competitive Part No.	G.I. Equivalent
3SK45	MEM 680-003
40467A	MEM 557-041
40468A	MEM 571-015
40559A	MEM 557-042
40600	MEM 616-056
40601	MEM 617-020
40602	MEM 618-013
40603	MEM 616-057
40604	MEM 617-021
40673	MEM 616-027
40819	MEM 616-045
40820	MEM 616-043
40821	MEM 617-069
40822	MEM 616-028
40823	MEM 617-010
40841	MEM 616-037
AM2009D	MEM 855D
AM2009F	MEM 855F
AM2009CD	MEM 855P
DD09K	MEM 807
DD10K	MEM 807
DD11K	MEM 807
DD12J	MEM 517A
DD13K	MEM 517
FT601	MEM 616
FT701	MEM 954
FT703	MEM 807
FT704	MEM 556C

Competitive Part No.	G.I. Equivalent
IT1700	MEM 660
IT1701	MEM 807
IT1702	MEM 807
IT1750	MEM 563
IT2700	MEM 954
IT2701	MEM 955
M100	MEM 562
M101	MEM 562
M106	MEM 954
M107	MEM 807
M108	MEM 806
M113	MEM 807
M114	MEM 807
M116	MEM 712A
M117	MEM 660
M163	MEM 806A
M164	MEM 806
M511	MEM 807
M511A	MEM 807
MFE120	MEM 616-041
MFE121	MEM 616-042
MFE122	MEM 617-014
MFE130	MEM 616-058
MFE131	MEM 616-059

Competitive Part No.	G.I. Equivalent
MFE132	MEM 617-023
MFE823	MEM 823
MFE824	MEM 667
MFE3001	MEM 557-043
MFE3002	MEM 710
MFE3005	MEM 557-044
MFE3006	MEM 554-012
MFE3007	MEM 554-013
MFE3008	MEM 617-022
MFE3020	MEM 807
MFE3021	MEM 807
MPF130	MEM 630
MPF131	MEM 631
MPF132	MEM 632
MX02D	MEM 855F
MX52D	MEM 855F
SD5010	MEM 550
SD5011	MEM 551
SFE630	MEM 823-013
UC1700	MEM 806
UC1764	MEM 806
US2766	MEM 955

MOSFET TRANSISTORS
Glossary of Terms and Abbreviations

P-Channel	A device constructed on an N type silicon substrate, whose drain and source components are of P type silicon.
N-Channel	A device constructed on a P type silicon substrate, whose drain and source components are of N type silicon.
Enhancement Mode	A device type that is normally off with zero gate voltage. A threshold voltage ($V_{GS(th)}$) is then required to turn the device on.
Depletion Mode	A device that is normally on with zero gate voltage. A cut-off voltage ($V_{GS(off)}$) is then required to turn the device off.

NOTE: P-Channel devices are almost exclusively enhancement mode whereas N-Channel FETS are made in both Enhancement and Depletion modes, with the Depletion mode being the predominant type.

BV_{DSS}	Drain to source breakdown voltage, all other terminals short-circuited to source.
BV_{GSS}	Gate to source breakdown voltage, all other terminals short-circuited to source.
BV_{SDS}	Source to drain breakdown voltage, all other terminals short-circuited to drain.
Cgs	Gate to source capacitance.
Cgd	Gate to drain capacitance.
Cds	Drain to source capacitance.
Ciss	Small-signal, common-source, short-circuit, input capacitance. Ciss = Cgd + Cgs
Coss	Small-signal, common-source, short-circuit, output capacitance. Coss = Cds + Cdg
Crss	Small-signal, common-source, short-circuit, reverse transfer capacitance. Also called reverse feedback capacitance. Crss = Cdg
Gps	Power gain expressed in decibels (dB) at a specified frequency.
$I_{D(on)}$	Drain current under specified conditions with channel biased on.
I_{DSS}	Zero-gate-voltage drain current. In enhancement mode devices, I_{DSS} is essentially the drain to substrate leakage.
I_{GSS}	Gate leakage current with all other terminals short-circuited to source. In devices with zener protection it is essentially the reverse leakage of the diode.
I_{SDS}	Source leakage current with all other terminals short-circuited to drain. In enhancement mode devices, I_{SDS} is essentially the source to substrate leakage.
I_{GF}	Gate forward current. The forward biased gate leakage current on unprotected N-Channel devices.
N.F.	Noise Figure is the ratio between input signal to noise and output signal to noise, expressed in decibels, it is a function of both frequency and generator impedance.
rds(on)	A.C. drain to source resistance when biased full ON.
$r_{DS(on)}$	Static (D.C.) drain to source on resistance when biased to full ON condition.
td(on)	Turn-on delay time.
td(off)	Turn-off delay time.
tr	Rise time. Measured from the 10% point to the 90% point on the leading edge of the waveform.
tf	Fall time. Measured from the 90% point to the 10% point on the lagging edge of the waveform.
$V_{DS(on)}$	Drain to source voltage drop under specified conditions with device biased ON.
$V_{GS(th)}$	Gate to source threshold voltage. Defined as the gate-source voltage required to turn the device on for minimum useful gain (Enhancement Mode)
$V_{GS(off)}$	Gate to source cutoff voltage. Gate to source voltage required to cut-off channel current. (Depletion Mode)

NOTE: $V_{GS(th)}$ and $V_{GS(off)}$ are analagous in that they both represent the voltage potential required to change the state of the device.

Yfs	Magnitude of common-source forward transfer admittance, usually expressed in micromhos (μmhos) at low frequencies (1 kHz). Yfs is approximately the same as gfs. At high frequencies Yfs includes the effect of gate-drain capacity.
Yos	Magnitude of common-source output admittance with the input a.c. short-circuited. Expressed in micro-mhos (μmhos)
I_{D1}/I_{D2}	ON gate-voltage drain current ratio. The differential between the two drain currents when biased with common source and gate potentials.
V_{GS1}/V_{GS2}	Differential gate to source voltage at a fixed operating point (ID) often referred to as the offset.
Yfs1/Yfs2	Common-source transadmittance ratio.
Yos1/Yos2	Output admittance differential. Expressed in micro-mhos (μmhos)

MEM 511

P-Channel Enhancement Mode MOSFET

FEATURES

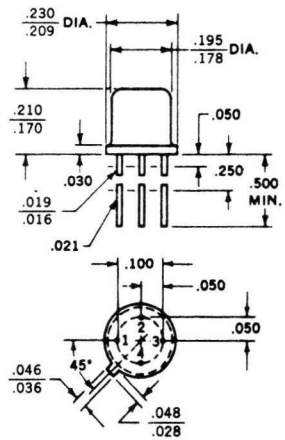
- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

(Designed Primarily For Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications.)

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers

TO-72



Bottom view

Note: All dimensions in inches.

MAXIMUM RATINGS

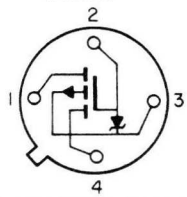
(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	−30V
Gate to Source Voltage	−30V
Gate to Drain Voltage	−30V
Drain Current	−50mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA
Storage Temperature	−50 to 150°C
Operating Junction Temperature	−50 to 125°C
Total Dissipation at 25°C Case Temperature	650mW
Total Dissipation at 25°C Ambient Temperature	225mW

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



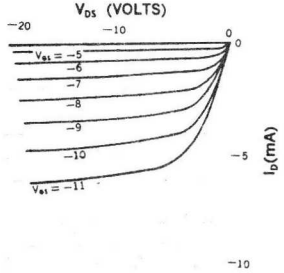
ELECTRICAL CHARACTERISTICS

(T_A = 25° C, unless otherwise specified — body grounded)

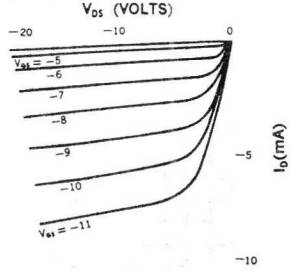
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−3		−6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		−0.5	−10	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current			−1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	−3	−6		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	−30			Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, $V_{GS} = V_{DS} = -10V$ 10MHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance			3	pF	$V_{GS} = V_{DS} = -10V$ f = 1mHz
C_{gd}	Gate to Drain Capacitance			2.5	pF	$V_{GS} = V_{DS} = -10V$ f = 1mHz
C_{ds}	Drain to Source Capacitance		.15		pF	$V_{GS} = V_{DS} = -10V$ f = 1mHz
$r_{DS(on)}$	Drain to Source Resistance		150	300	ohms	$V_{GS} = -15V$, $I_{DS} = -0.1mA$

TYPICAL CHARACTERISTIC CURVES

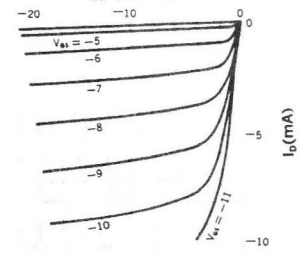
DRAIN CHARACTERISTICS AT 125°C



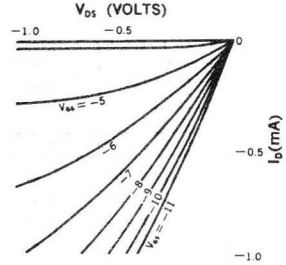
DRAIN CHARACTERISTICS AT 25°C



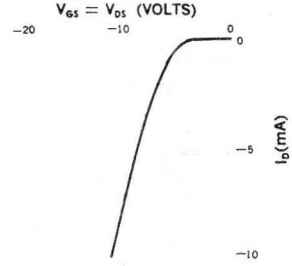
DRAIN CHARACTERISTICS AT −70°C



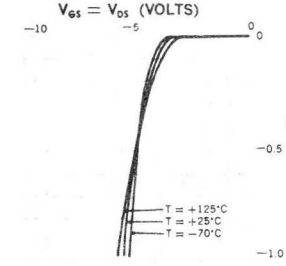
DRAIN CHARACTERISTICS AT 25°C



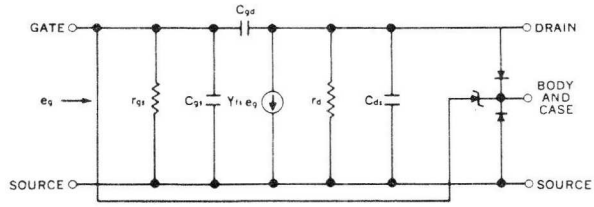
TURN-ON CHARACTERISTICS AT 25°C



TURN-ON CHARACTERISTICS



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 6$ mA



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

MEM 511A

P-Channel Enhancement Mode MOSFET

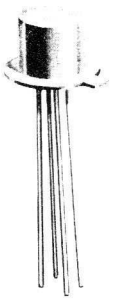
FEATURES

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

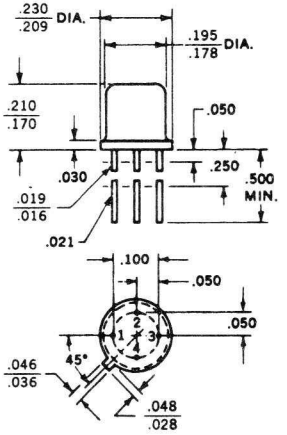
APPLICATIONS

(Designed Primarily For Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications.)

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers



TO-72



Bottom view

Note: All dimensions in inches.

MAXIMUM RATINGS

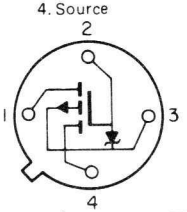
(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	−30V
Gate to Source Voltage	−30V
Gate to Drain Voltage	−30V
Drain Current	−50mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA
Storage Temperature	−50 to 150°C
Operating Junction Temperature	−50 to 125°C
Total Dissipation at 25°C Case Temperature	650mW
Total Dissipation at 25°C Ambient Temperature	225mW

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



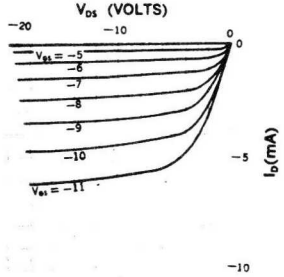
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

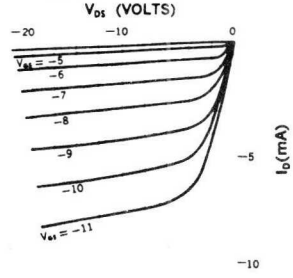
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−3		−6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		−0.5	−10	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current			−1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	−3	−6		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	−30			Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, $V_{GS} = V_{DS} = -10V$ 10MHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance			4	pF	$V_{GS} = V_{DS} = -10V$ f = 1mHz
C_{gd}	Gate to Drain Capacitance			2.5	pF	$V_{GS} = V_{DS} = -10V$ f = 1mHz
C_{ds}	Drain to Source Capacitance		.15		pF	$V_{GS} = V_{DS} = -10V$ f = 1mHz
$r_{DS(on)}$	Drain to Source Resistance			500	ohms	$V_{GS} = -15V$, $I_{DS} = -0.1mA$

TYPICAL CHARACTERISTIC CURVES

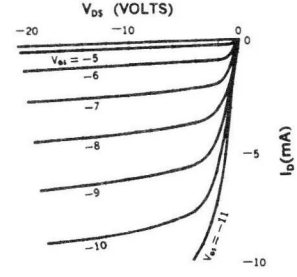
DRAIN CHARACTERISTICS AT 125°C



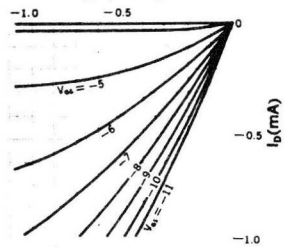
DRAIN CHARACTERISTICS AT 25°C



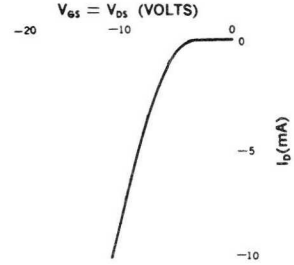
DRAIN CHARACTERISTICS AT −70°C



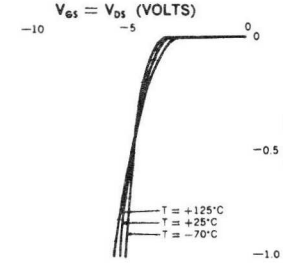
DRAIN CHARACTERISTICS AT 25°C



TURN-ON CHARACTERISTICS AT 25°C



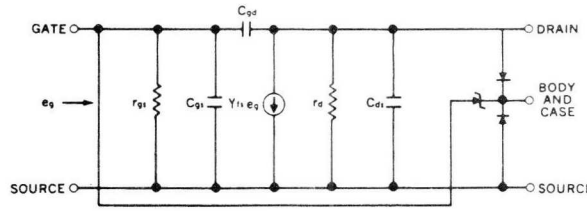
TURN-ON CHARACTERISTICS



SMALL SIGNAL EQUIVALENT CURRENT

(Conditions: V_{GS} = V_{DS} = −10V)

$I_D \approx 6$ mA



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

INDUSTRIAL/ MOSFET

MEM 511C

P-Channel Enhancement Mode MOSFET

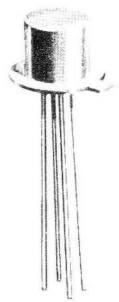
FEATURES

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

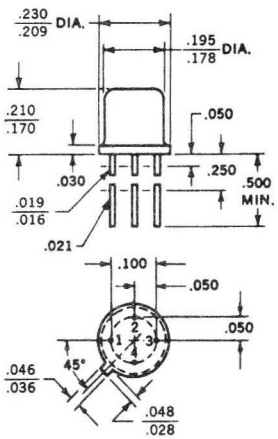
APPLICATIONS

(Designed Primarily For Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications.)

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers



TO-72



Bottom view

Note: All dimensions in inches.

MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	−25V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−50mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA
Storage Temperature	−50 to 125°C
Operating Junction Temperature	−50 to 100°C
Total Dissipation at 25°C Case Temperature	500mW
Total Dissipation at 25°C Ambient Temperature	175mW

ELECTRICAL CHARACTERISTICS

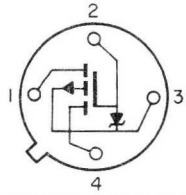
(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−3		−6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current			−10	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current			−1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	−3	−6		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	−25			Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, $V_{GS} = V_{DS} = -10V$ 10MHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance			4	pF	$V_{GS} = V_{DS} = -10V$, f = 1 MHz
C_{gd}	Gate to Drain Capacitance			4	pF	$V_{GS} = V_{DS} = -10V$, f = 1 MHz
C_{ds}	Drain to Source Capacitance		.15		pF	$V_{GS} = V_{DS} = -10V$, f = 1 MHz
$r_{DS(on)}$	Drain to Source Resistance		150		ohms	$V_{GS} = -15V$, $I_{DS} = -1mA$

TERMINAL DIAGRAM

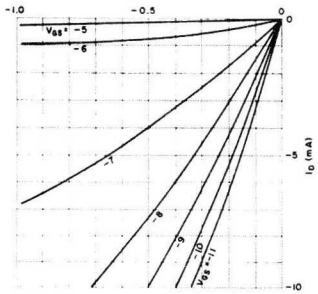
Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source

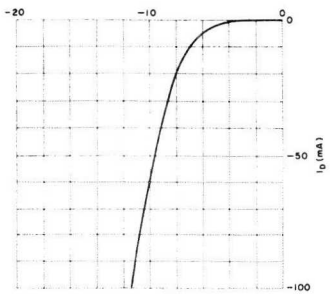


TYPICAL CHARACTERISTIC CURVES

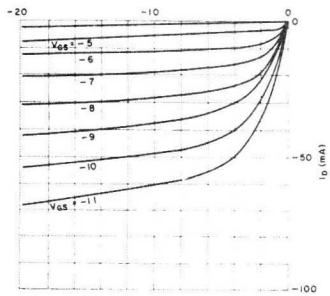
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



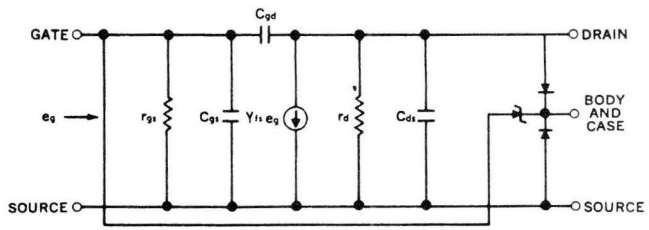
TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 6$ mA



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

MEM 517

P-Channel Enhancement Mode MOSFET

FEATURES

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

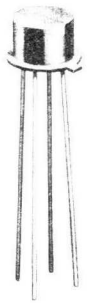
(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

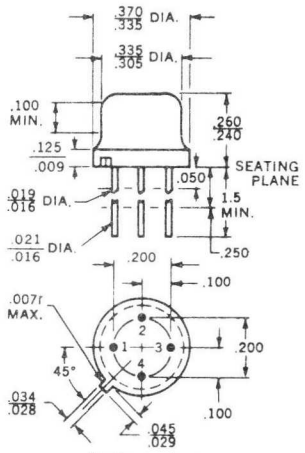
MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	−30V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−250mA
Gate Current (Forward Direction for Zener Clamp)	+1.0mA
Storage Temperature	−50 to 150°C
Operating Junction Temperature	−50 to 125°C
Total Dissipation at 25°C Case Temperature	2.0 Watts
Total Dissipation at 25°C Ambient Temperature	0.6 Watt



TO-33



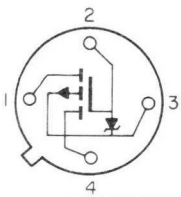
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



ELECTRICAL CHARACTERISTICS

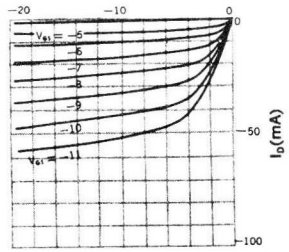
(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−2.5		−5	Volts	V_{GS} = V_{DS}, I_D = −10μA
I_{DSS}	Drain Leakage Current		−0.8	−50	nA	V_{DS} = −20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current		−0.1	−1	nA	V_{GS} = −15V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−25	−60		mA	V_{GS} = V_{DS} = −10V
BV_{DSS}	Drain-Source Breakdown	−30	−50		Volts	I_D = −10μA, V_{GS} = 0V
BV_{GSS}	Gate to Source Breakdown	−25	−40		Volts	I_{GS} = −10μA, V_{DS} = 0V
Y_{fs}	Transadmittance		12000		μmho	1 kHz, V_{GS} = V_{DS} = −10V
C_{gs}	Gate to Source Capacitance		10		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{gd}	Gate to Drain Capacitance		10		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{ds}	Drain to Source Capacitance		0.15		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
$r_{DS(on)}$	Drain to Source on Resistance		25		Ohms	V_{GS} = −20V, I_{DS} = −10mA
$r_{DS(on)}$	Drain to Source on Resistance		45		Ohms	V_{GS} = −10V, I_{DS} = −10mA

TYPICAL CHARACTERISTIC CURVES

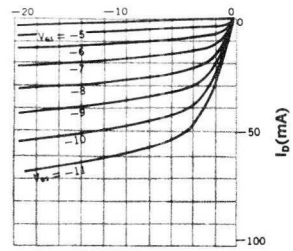
DRAIN CHARACTERISTICS AT 125°C

V_{DS} (VOLTS)



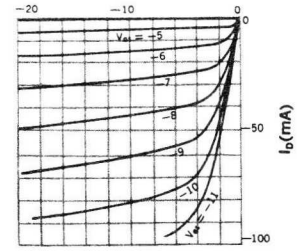
DRAIN CHARACTERISTICS AT 25°C

V_{DS} (VOLTS)



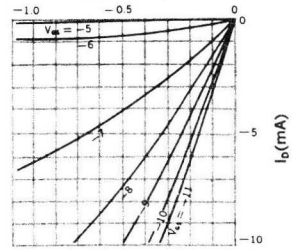
DRAIN CHARACTERISTICS AT −70°C

V_{DS} (VOLTS)



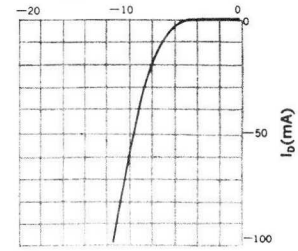
DRAIN CHARACTERISTICS AT 25°C

V_{DS} (VOLTS)



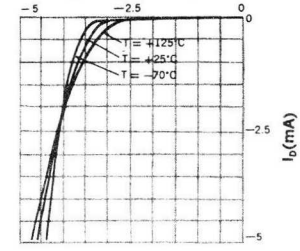
TURN-ON CHARACTERISTICS AT 25°C

$V_{GS} = V_{DS}$ (VOLTS)



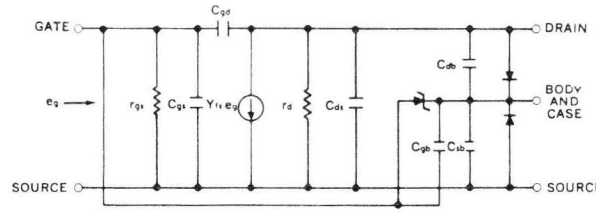
TURN-ON CHARACTERISTICS

$V_{GS} = V_{DS}$ (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT

(Conditions: $V_{DS} = V_{DS} = -10V$
$I_D \approx 60mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	10	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	0.15	pF
C_{gb}	Gate to body capacitance	6	pF
C_{db}	Drain to body capacitance	10	pF
C_{sb}	Source to body capacitance	20	pF
Y_{fs}	Forward transadmittance	12000	μmho

MEM 517A

P-Channel Enhancement Mode MOSFET

FEATURES

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

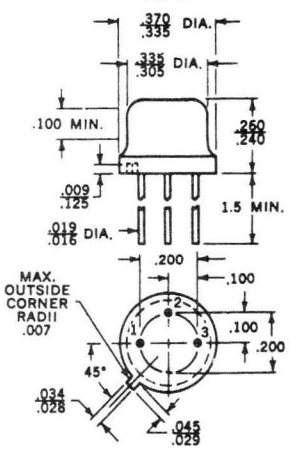
Drain to Source Voltage	−30V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−250mA
Gate Current (Forward Direction for Zener Clamp)	+1.0mA
Storage Temperature	−50 to 150°C
Operating Junction Temperature	−50 to 125°C
Total Dissipation at 25°C Case Temperature	2.0 Watts
Total Dissipation at 25°C Ambient Temperature	0.6 Watt

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−2.5		−5	Volts	V_{GS} = V_{DS}, I_D = −10μA
I_{DSS}	Drain Leakage Current		−0.8	−50	nA	V_{DS} = −20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current		−0.1	−1	nA	V_{GS} = −15V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−25	−60		mA	V_{GS} = V_{DS} = −10V
BV_{DSS}	Drain-Source Breakdown	−30	−50		Volts	I_D = −10μA, V_{GS} = 0V
BV_{GSS}	Gate to Source Breakdown	−25	−40		Volts	I_{GS} = −10μA, V_{DS} = 0V
Y_{fs}	Transadmittance		12000		μmho	1 kHz, V_{GS} = V_{DS} = −10V
C_{gs}	Gate to Source Capacitance		10		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{gd}	Gate to Drain Capacitance		10		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{ds}	Drain to Source Capacitance		0.15		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
$r_{DS(on)}$	Drain to Source on Resistance		25		Ohms	V_{GS} = −20V, I_{DS} = −10mA
$r_{DS(on)}$	Drain to Source on Resistance		45		Ohms	V_{GS} = −10V, I_{DS} = −10mA

TO-5



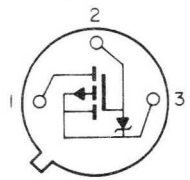
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

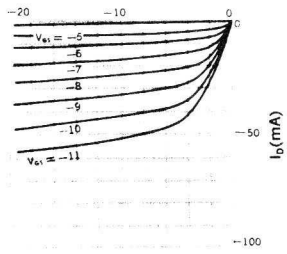
Lead

1. Drain
2. Gate
3. Source & Body (Case)

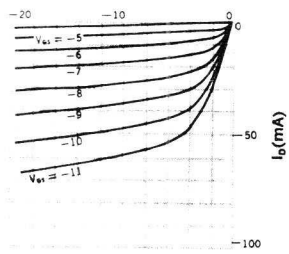


TYPICAL CHARACTERISTIC CURVES

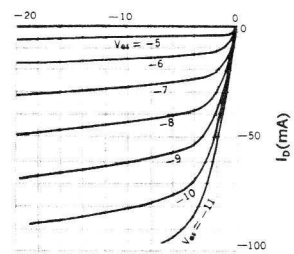
DRAIN CHARACTERISTICS AT 125°C



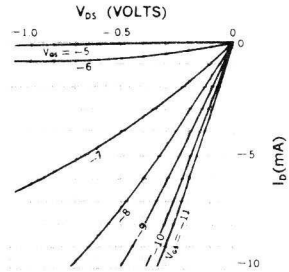
DRAIN CHARACTERISTICS AT 25°C



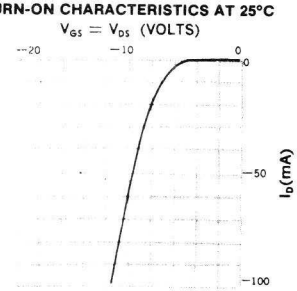
DRAIN CHARACTERISTICS AT −70°C



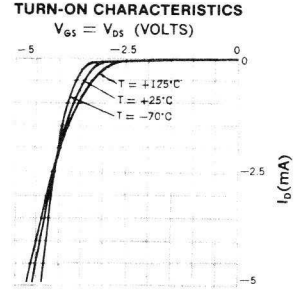
DRAIN CHARACTERISTICS AT 25°C



TURN-ON CHARACTERISTICS AT 25°C



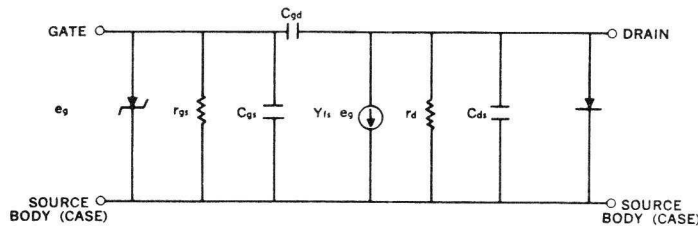
TURN-ON CHARACTERISTICS



SMALL SIGNAL EQUIVALENT CIRCUIT

(Conditions: V_{GS} = V_{DS} = −10V)

$I_D \approx$ 60mA



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	16	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	10	pF
Y_{fs}	Forward transadmittance	12000	μmho

MEM 517C

P-Channel Enhancement Mode MOSFET

FEATURES

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS

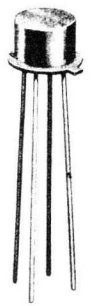
(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	−25V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−250mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA
Storage Temperature	−50 to 125°C
Operating Junction Temperature	−50 to 100°C
Total Dissipation at 25°C Case Temperature	1.5 WATTS
Total Dissipation at 25°C Ambient Temperature	0.45 WATT

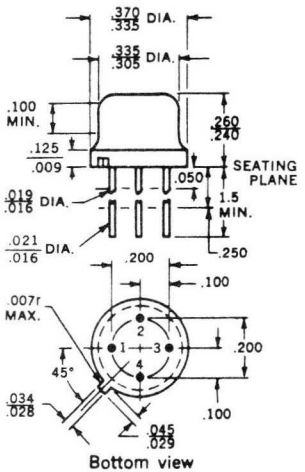
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−2.5		−5	Volts	V_{GS} = V_{DS}, I_D = −10μA
I_{DSS}	Drain Leakage Current			−50	nA	V_{DS} = −20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current			−1	nA	V_{GS} = −15V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−20	−50		mA	V_{GS} = V_{DS} = −10V
BV_{DSS}	Drain-Source Breakdown	−25	−40		Volts	I_D = −10μA, V_{GS} = 0V
BV_{GSS}	Gate to Source Breakdown	−25	−40		Volts	I_{GS} = −10μA, V_{DS} = 0V
Y_{fs}	Transadmittance		12000		μmho	1 kHz, V_{GS} = V_{DS} = −10V
C_{gs}	Gate to Source Capacitance		10	15	pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{gd}	Gate to Drain Capacitance		10	15	pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{ds}	Drain to Source Capacitance		0.15	0.2	pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
$r_{DS(on)}$	Drain to Source on Resistance		25	50	Ohms	V_{GS} = −20V, I_{DS} = −10mA
$r_{DS(on)}$	Drain to Source on Resistance		45	100	Ohms	V_{GS} = −10V, I_{DS} = −10mA



TO-33



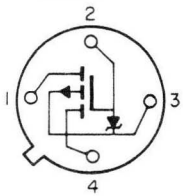
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

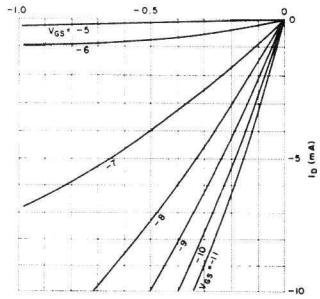
Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source

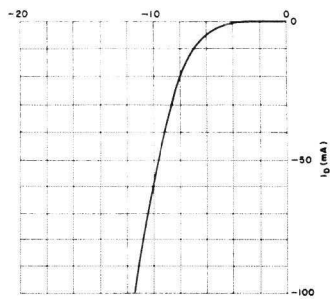


TYPICAL CHARACTERISTIC CURVES

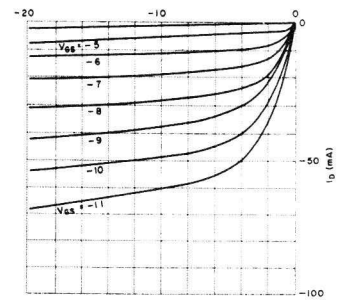
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



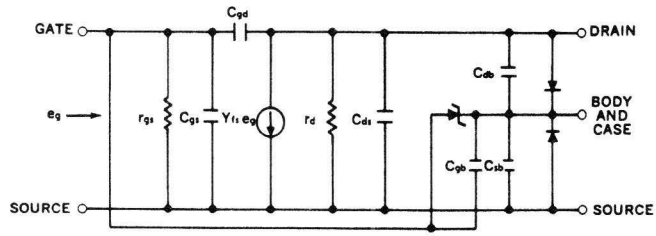
TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)



DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 60mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	10	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	0.15	pF
C_{gb}	Gate to body capacitance	6	pF
C_{db}	Drain to body capacitance	10	pF
C_{sb}	Source to body capacitance	20	pF
Y_{fs}	Forward transadmittance	12000	μmho

MEM 520

P-Channel Enhancement Mode MOSFET

FEATURES

- 10^{15} ohms input resistance
- Normally off with zero gate voltage
- Square Law linear transfer characteristics

APPLICATIONS

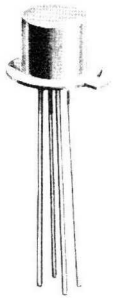
(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Very high input impedance amplifiers
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- RF and IF amplifiers
- Multiplexers

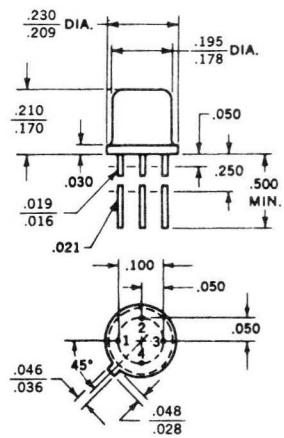
MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	—30V
Gate to Source Voltage	—40V
Gate to Drain Voltage	—40V
Drain Current	—50mA
Storage Temperature	—50 to 150°C
Operating Junction Temperature	—50 to 125°C
Total Dissipation at 25°C Case Temperature	650mW
Total Dissipation at 25°C Ambient Temperature	225mW



TO-72



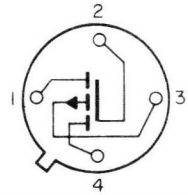
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



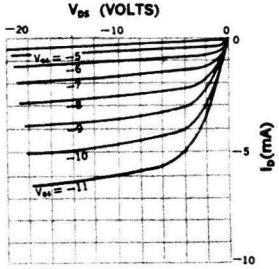
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

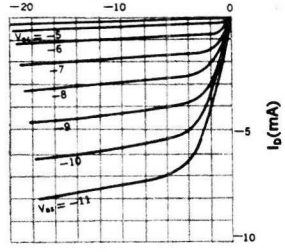
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	—3		—6	Volts	V_{GS} = V_{DS}, I_D = —10μA
I_{DSS}	Drain Leakage Current		—0.5	—10	nA	V_{DS} = —20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current		—.03	—3	pA	V_{GS} = —40V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	— 3			mA	V_{GS} = V_{DS} = —10V
BV_{DSS}	Drain-Source Breakdown	—30			Volts	I_D = —10μA, V_{GS} = 0V
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, V_{GS} = V_{DS} = —10V 10MHz, V_{GS} = V_{DS} = —10V
C_{gs}	Gate to Source Capacitance			3	pF	V_{GS} = V_{DS} = —10V, f = 1 MHz
C_{gd}	Gate to Drain Capacitance			2.5	pF	V_{GS} = V_{DS} = —10V, f = 1 MHz
C_{ds}	Drain to Source Capacitance		.15		pF	V_{GS} = V_{DS} = —10V, f = 1 MHz
$r_{DS(on)}$	Drain to Source Resistance		150		ohms	V_{GS} = —15V, I_{DS} = —1mA

TYPICAL CHARACTERISTIC CURVES

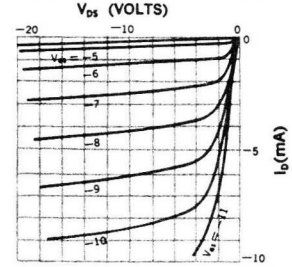
DRAIN CHARACTERISTICS AT 125°C



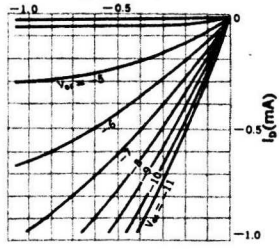
DRAIN CHARACTERISTICS AT 25°C



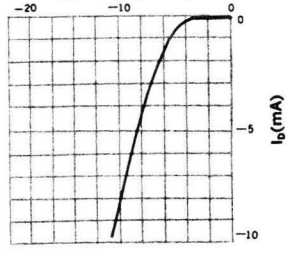
DRAIN CHARACTERISTICS AT −70°C



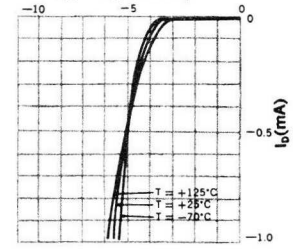
DRAIN CHARACTERISTICS AT 25°C



TURN-ON CHARACTERISTICS AT 25°C



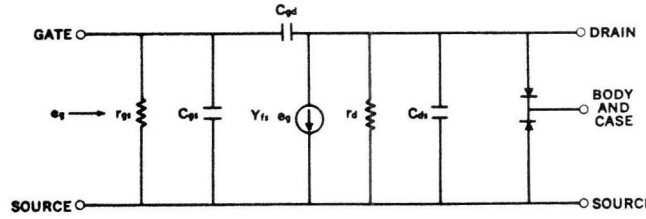
TURN-ON CHARACTERISTICS



SMALL SIGNAL EQUIVALENT CIRCUIT

(Conditions: $V_{GS} = V_{DS} = -10V$)

$I_D \approx 6mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance	10^{15}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

MEM 520C

P-Channel Enhancement Mode MOSFET

FEATURES

- 10^{15} ohms input resistance
- Normally off with zero gate voltage
- Square Law linear transfer characteristics

APPLICATIONS

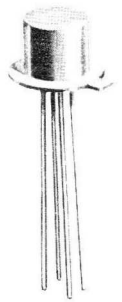
(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Very high input impedance amplifiers
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- RF and IF amplifiers
- Multiplexers

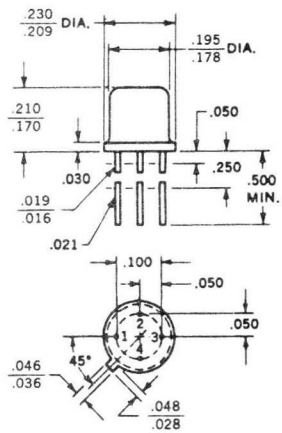
MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	−25V
Gate to Source Voltage	−25V
Gate to Drain Voltage	−25V
Drain Current	−50mA
Storage Temperature	−50 to 125°C
Operating Junction Temperature	−50 to 100°C
Total Dissipation at 25°C Case Temperature	500mW
Total Dissipation at 25°C Ambient Temperature	175mW



TO-72



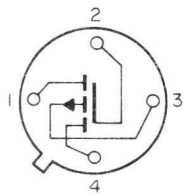
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



ELECTRICAL CHARACTERISTICS

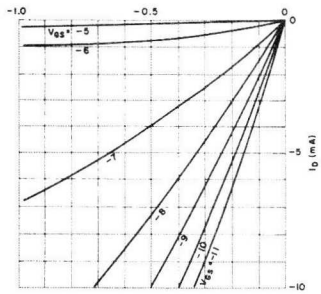
(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{GS(T)}$	Gate-Source Threshold Voltage	−3		−6	Volts	V_{GS} = V_{DS}, I_D = −10μA
I_{DSS}	Drain Leakage Current			−10	nA	V_{DS} = −25V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current			−3	pA	V_{GS} = −25V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−3			mA	V_{GS} = V_{DS} = −10V
BV_{DSS}	Drain-Source Breakdown	−25			Volts	I_D = −10μA, V_{GS} = 0V
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1kHz, V_{GS} = V_{DS} = −10V 10MHz, V_{GS} = V_{DS} = −10V
C_{gs}	Gate to Source Capacitance			4	pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{gd}	Gate to Drain Capacitance			4	pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
C_{ds}	Drain to Source Capacitance		.15		pF	V_{GS} = V_{DS} = −10V, f = 1 MHz
$r_{DS(on)}$	Drain to Source Resistance		150		ohms	V_{GS} = −15V, I_{DS} = −1mA

TYPICAL CHARACTERISTIC CURVES

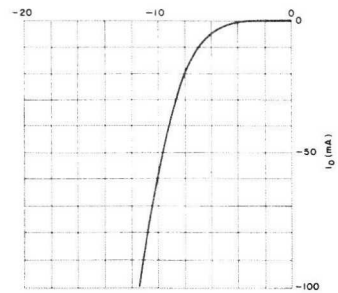
DRAIN CHARACTERISTICS AT 25°C

V_{DS} (VOLTS)



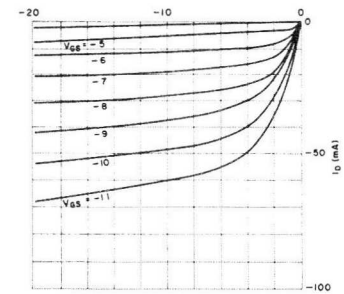
TURN-ON CHARACTERISTICS AT 25°C

$V_{GS} = V_{DS}$ (VOLTS)



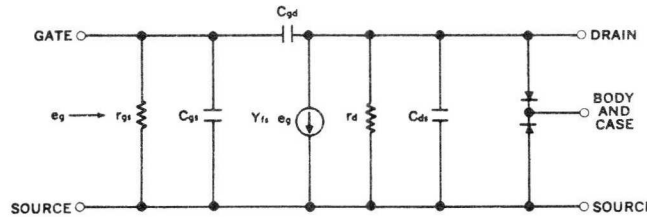
DRAIN CHARACTERISTICS AT 25°C

V_{DS} (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT

(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 6mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance	10^{15}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_{gs}	Gate to source capacitance	2.25	pF
C_{gd}	Gate to drain capacitance	1.5	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	2500	μmho

MEM 550 **MEM 550C**
MEM 551 **MEM 551C**

Dual P-Channel Enhancement Mode MOSFETS

FEATURES

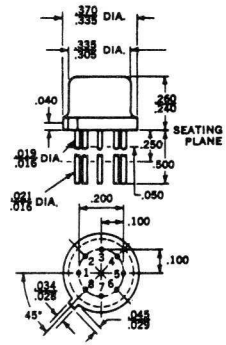
- 10^{10} ohms input resistance (MEM 550 Series)
- 10^{15} ohms input resistance (MEM 551 Series)
- Integrated zener clamp protects the gate (MEM 550 Series)
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers
- Very high input impedance amplifiers (MEM 551 Series)

Actual Size

TO-77



Bottom View

Note: All dimensions in inches

MAXIMUM RATINGS

	MEM 550	MEM 551	MEM 550C	MEM 551C
Drain to Source Voltage	−30V	−30V	−25V	−25V
Source to Drain Voltage	−30V	−30V	−25V	−25V
Gate to Source Voltage	−30V	−30V	−25V	−25V
Gate to Drain Voltage	−30V	−30V	−25V	−25V
Gate Current (Forward Direction for Zener Clamp)	+0.1mA	—	+0.1mA	—
Drain Current	−25mA each side		−25mA each side	
Storage Temperature	−50 To 150°C		−50 To 125°C	
Operating Junction Temperature	−50 To 125°C		−50 To 100°C	
Total Dissipation at 25°C Case Temperature	325mW each side		250mW each side	
Total Dissipation at 25°C Ambient Temperature	112mW each side		85mW each side	

ELECTRICAL CHARACTERISTICS (for each side — body grounded)

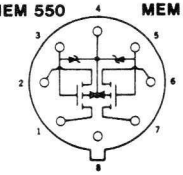
			MEM 550 MEM 551			MEM 550C MEM 551C			
SYMBOL	CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{GST}	Gate Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -10\mu A$	−3	—	−6	−3	—	−6	V
I_{DSS}	Drain Leakage Current	$V_{DS} = -20V$, $V_{GS} = 0V$	—	−0.2	−10	—	—	−10	nA
I_{SDS}	Source Leakage Current	$V_{DS} = -20V$, $V_{GS} = 0V$	—	−0.2	−10	—	—	−10	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = -15V$, $V_{DS} = 0V$ MEM 550	—	−0.1	−1	—	—	—	pA
		MEM 551	—	—	−1	—	—	—	
		MEM 550C	—	—	—	—	−.03	−4	
		MEM 551C	—	—	—	—	—	−10	
$I_{D(on)}$	Drain Current	$V_{GS} = V_{DS} = -10V$	−1.5	−5	—	−1.5	−5	—	mA
BV_{DSS}	Drain-Source Breakdown	$I_D = -10\mu A$, $V_{GS} = 0V$	−30	−50	—	−25	−50	—	V
BV_{SDS}	Source-Drain Breakdown	$I_S = -10\mu A$, $V_{GS} = 0V$	−30	−50	—	−25	−50	—	V
BV_{GSS}	Gate to Source Breakdown	$I_{GS} = -10\mu A$, $V_{DS} = 0V$	−30	−50	—	−25	−50	—	V
Y_{fs}	Transadmittance	1kHz, $V_{GS} = V_{DS} = -10V$	500	—	—	500	—	—	μmho
C_{GS}	Gate to Source Capacitance	$V_{GS} = V_{DS} = -10V$	—	1.1	—	—	—	4	pF
C_{gd}	Gate to Drain Capacitance	$V_{GS} = V_{DS} = -10V$	—	1.1	—	—	—	4	pF
C_{ds}	Drain to Source Capacitance	$V_{GS} = V_{DS} = -10V$	—	0.15	—	—	—	0.2	pF
$r_{DS\ (on)}$	Drain to Source on Resistance	$V_{GS} = -15V$, $V_{DS} = 0V$	—	250	—	—	—	400	ohms
Y_{fs1}/Y_{fs2}	Transadmittance Ratio	$V_{DS} = -10V$, $I_{DS} = 250\mu A$	0.8	—	1.0	0.8	—	1.0	mV
V_{GS1}-V_{GS2}	Gate Voltage Differential	$V_{DS} = -10V$, $I_{DS} = 250\mu A$	—	70	200	—	70	200	mV

TERMINAL DIAGRAM

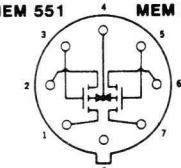
Lead

1. Drain 1
2. Source 1
3. Gate 1
4. Substrate (Body)
5. Gate 2
6. Source 2
7. Drain 2
8. Open

MEM 550 MEM 550C



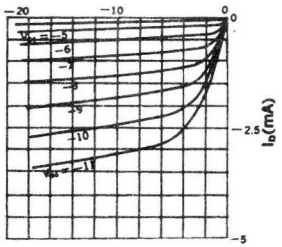
MEM 551 MEM 551C



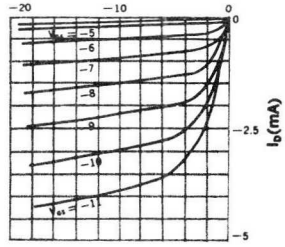
TYPICAL CHARACTERISTIC CURVES

MEM 550 / MEM 551

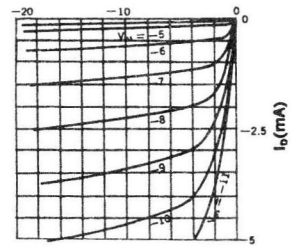
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)



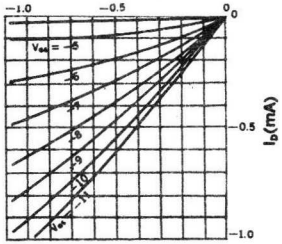
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



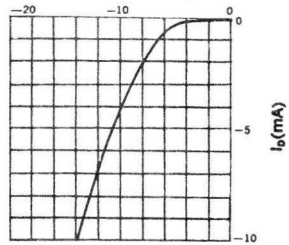
DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)



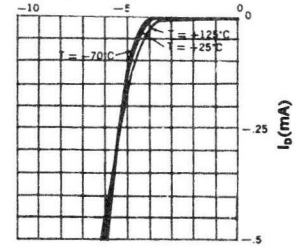
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

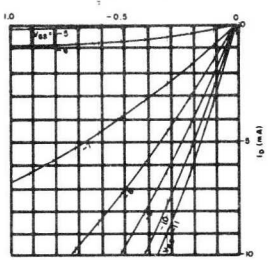


TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)

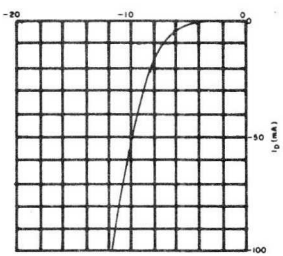


MEM 550C / MEM 551C

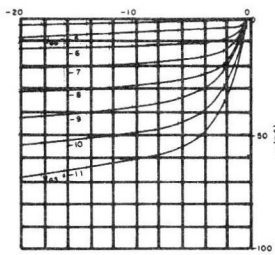
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

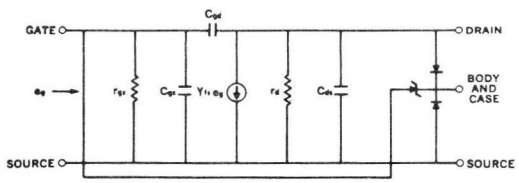


DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT FOR EACH SIDE

(Conditions: $V_{GS} = V_{DS} = 10V$)
$I_D \approx 3mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	18	Kohms
C_{gs}	Gate to source capacitance	1.1	pF
C_{gd}	Gate to drain capacitance	1.1	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	1400	μmho

MEM 554

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- 10^{15} ohms input resistance
- Dual Gate Cascode operation
- Low 3_{rd} order distortion
- Reverse AGC capability
- Linear mixing capability
- High gain — low noise through VHF range
- Low feedback capacitance — .025 pf typ.

APPLICATIONS

- TV Tuners (RF & Mixer)
- FM Tuners (RF & Mixer)
- IF Amplifiers
- Synchronous Detectors
- Wideband Amplifiers

MAXIMUM RATINGS ($T_A = 25°C$, unless otherwise specified)

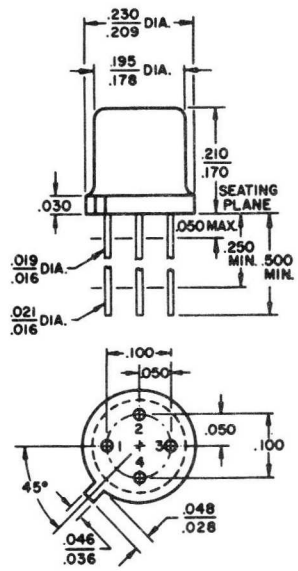
Drain-to-source voltage, V_{DS} ..... +20V
Gate No. 1-to-source voltage, V_{G1S} ..... +5 to −10V
Gate No. 2-to-source voltage, V_{G2S} ..... ±20V
Gate No. 1 and Gate No. 2 to all terminals
(non-recurring transients) ..... ±45V
Drain Current, I_D ..... Limited by Dissipation
Storage Temperature ..... −65 to +150°C
Operating Junction Temperature ..... −65 to +125°C
Total Dissipation at 25°C Case Temperature ..... 450 mw
Total Dissipation at 25°C Ambient Temperature ..... 225 mw
at 100°C Ambient Temperature ..... 150 mw
Derate Linearly from 100°C to 125°C at 6 mW/°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage drain to source	20	—	—	V	$V_{G1} = V_{G2} = -4V$, $I_D = 100uA$
I_{G1SS}	Gate No. 1 Leakage Current	—	—	.10	nA	$V_{G1S} = -20V$, $V_{G2S} = V_{DS} = 0V$
I_{G2SS}	Gate No. 2 Leakage Current	—	—	.10	nA	$V_{G2S} = -20V$, $V_{G1S} = V_{DS} = 0V$
$I_{D(off)}$	Drain to Source Leakage Current	—	—	100	uA	$V_{DS} = +20V$, $V_{G1} = V_{G2} = -4.0V$
$V_{G1S(off)}$	Gate No. 1-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G2S} = +4.0V$
$V_{G2S(off)}$	Gate No. 2-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G1S} = 0V$
I_{DSS}	Zero signal Gate voltage drain current	3	—	30	mA	$V_{DS} = +15V$, $V_{G2} = +4.0V$ $V_{G1} = 0V$
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	5.0	—	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 44 MHz
C_{oss}	Small-signal, short circuit drain-to-source capacitance	—	2.5	3.5	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 44 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	.02	—	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 1 MHz
G_{fs1}	Forward trans-conductance of gate No. 1	10,000	13,000	—	umhos	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 1 kHz
G_{ps}	Power gain (See fig. 1 for measurements circuits)	18	—	—	db.	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 200 MHz
NF	Noise Figure** (See Fig. 1 for Measurement Circuit)	—	2.8	3.5	db.	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 200 MHz
E_{int}	Interefering signal level at gate for 1% Cross Modulation Distortion	—	120	—	mV	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ Desired frequency = 200 MHz Undesired frequency = 150 MHz Input unturned

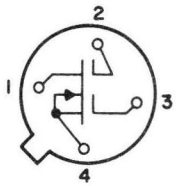
*V_{G1S} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72



Bottom view
NOTE: All dimensions in inches

TERMINAL DIAGRAM



LEAD

1. Drain
2. Gate No. 2
3. Gate No. 1
4. Source, substrate and case

Fig. 1 200 MHz Power Gain and Noise Figure Test Circuit

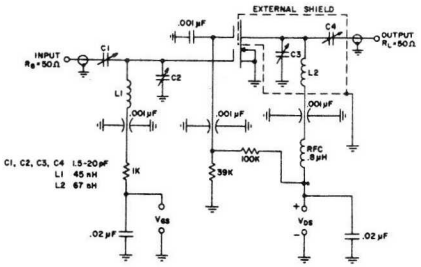


Fig. 2 Power Gain vs. Drain Current

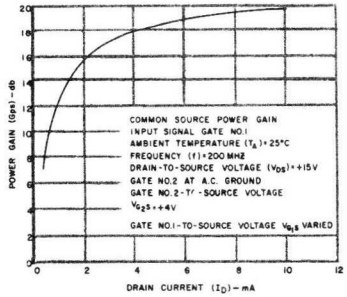


Fig. 3 Noise Figure vs. Drain Current

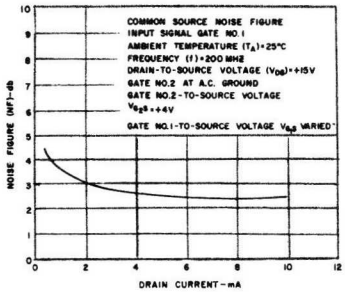


Fig. 4 Gate No. 2 Gain Control Curve

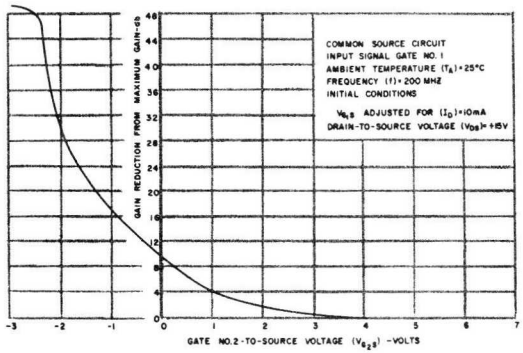


Fig. 5 Noise Figure vs. Gate No. 2-to-source voltage

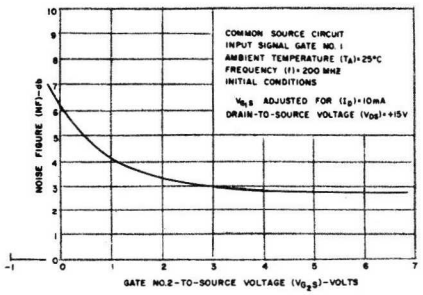
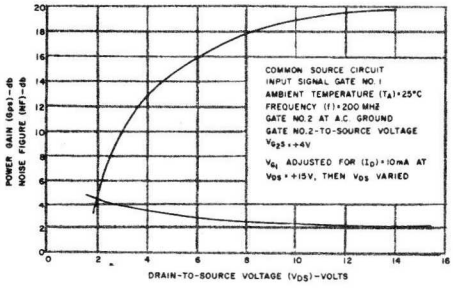


Fig. 6 Power Gain and Noise Figure vs. V_{DS}



MEM 554C

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- 10^{15} ohms input resistance
- Dual Gate Cascode operation
- Low 3rd order distortion
- Reverse AGC capability
- Linear mixing capability
- High gain — low noise through VHF range
- Low feedback capacitance — .025 pf typ.

APPLICATIONS

- TV Tuners (RF & Mixer)
- FM Tuners (RF & Mixer)
- IF Amplifiers
- Synchronous Detectors
- Wideband Amplifiers

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain-to-source voltage, V_{DS}	+20V
Gate No. 1-to-source voltage, V_{G1S}	+5 to −10V
Gate No. 2-to-source voltage, V_{G2S}	±10V
Gate No. 1 and Gate No. 2 to all terminals (non-recurring transients)	±45V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−65 to +150°C
Operating Junction Temperature	−65 to +125°C
Total Dissipation at 25°C Case Temperature	450 mw
Total Dissipation at 25°C Ambient Temperature	225 mw
at 100°C Ambient Temperature	150 mw

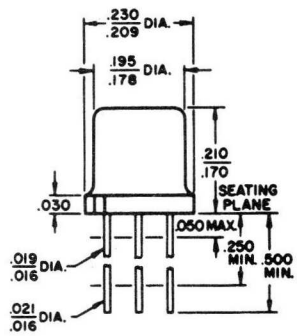
Derate Linearly from 100°C to 125°C at 6 mW/°C

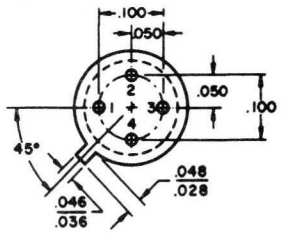
ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage drain to source	20	—	—	V	$V_{G1} = V_{G2} = -4V$, $I_D = 100uA$
I_{G1SS}	Gate No. 1 Leakage Current	—	—	1.0	nA	$V_{G1S} = -20V$, $V_{G2S} = V_{DS} = 0V$
I_{G2SS}	Gate No. 2 Leakage Current	—	—	1.0	nA	$V_{G2S} = -20V$, $V_{G1S} = V_{DS} = 0V$
$I_{D(off)}$	Drain to Source Leakage Current	—	—	100	uA	$V_{DS} = +20V$, $V_{G1} = V_{G2} = -4.0V$
$V_{G1S(off)}$	Gate No. 1-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G2S} = +4.0V$
$V_{G2S(off)}$	Gate No. 2-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G1S} = 0V$
I_{DSS}	Zero signal Gate voltage drain current	3	—	30	mA	$V_{DS} = +15V$, $V_{G2} = +4.0V$ $V_{G1} = 0V$
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	5.0	—	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 44 MHz
C_{oss}	Small-signal, short circuit drain-to-source capacitance	—	2.5	3.5	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f =44 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	.02	—	pF	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$, f = 1 MHz
G_{fs}	Forward trans-conductance of gate No. 1	8000	11,000	—	umhos	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 1 kHz
G_{ps}	Power gain (See fig. 1 for measurements circuits)	16	18	—	db.	$V_{GS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 200 MHz
NF	Noise Figure** (See Fig. 1 for Measurement Circuit)	—	3.5	4.5	db.	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ f = 200 MHz
E_{int}	Interefering signal level at gate for 1% Cross Modulation Distortion	—	120	—	mV	$V_{DS} = +15V$, $I_D = 10$ mA,* $V_{G2S} = +4.0V$ Desired frequency = 200 MHz Undesired frequency = 150 MHz Input unturned

*V_{G1S} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72

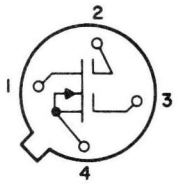




Bottom view

NOTE: All dimensions in inches

TERMINAL DIAGRAM



LEAD

1. Drain
2. Gate No. 2
3. Gate No. 1
4. Source, substrate and case

Fig. 1 200 MHz Power Gain and Noise Figure Test Circuit

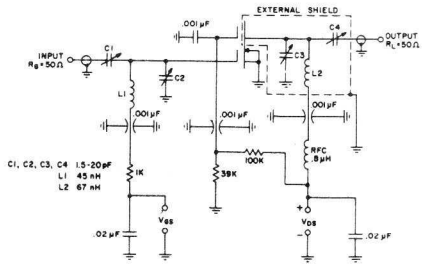


Fig. 2 Power Gain vs. Drain Current

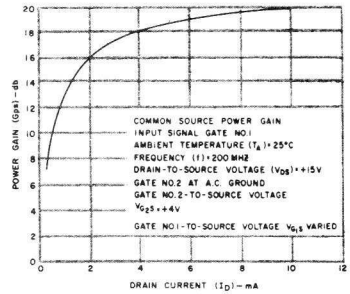


Fig. 3 Noise Figure vs. Drain Current

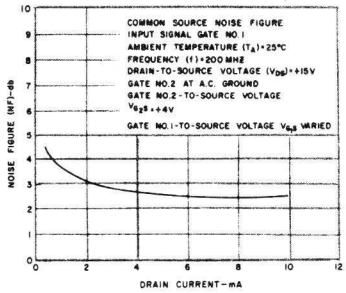


Fig. 4 Gate No. 2 Gain Control Curve

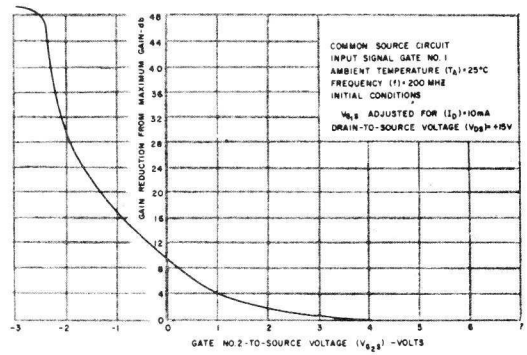


Fig. 5 Noise Figure vs. Gate No. 2-to-source voltage

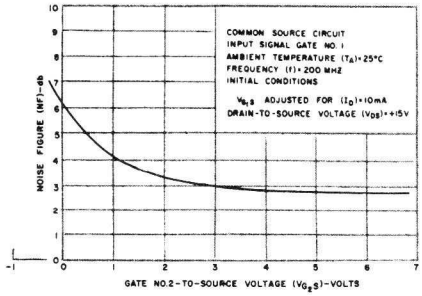
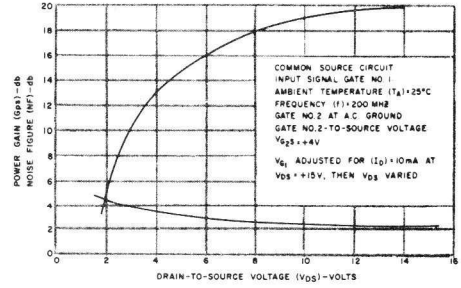


Fig. 6 Power Gain and Noise Figure vs. V_{DS}



MEM 556 MEM 556C

P-Channel Enhancement Mode MOSFETS

FEATURES

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics
- High Drain, Source and Gate breakdown voltages
- High off to on ratio

APPLICATIONS

(Designed Primarily For Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications.)

- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Multiplexers

MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

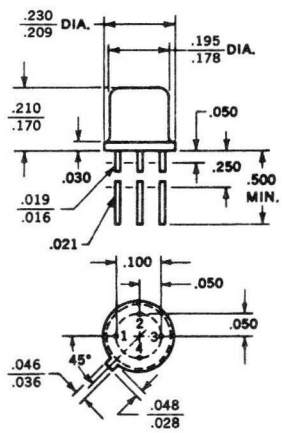
	MEM 556	MEM 556C
Drain to Source Voltage	−50V	−45V
Gate to Source Voltage	−50V	−45V
Gate to Drain Voltage	−50V	−45V
Drain Current	−20mA	−20mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA	+0.1mA
Storage Temperature	−50 to 150°C	−50 to 125°C
Operating Junction Temperature	−50 to 125°C	−50 to 100°C
Total Dissipation at 25°C Case Temperature	275mW	
Total Dissipation at 25°C Ambient Temperature	100mW	100mW
Derating Factor	1mW/°C	1.33 mW/°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

		MEM 556			MEM 556C				
SYM	CHARACTERISTIC	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(T)}$	Gate Source Cutoff Voltage	−3.0	—	−6.0	−3.0	—	−6.0	Volts	V_{DS} = −10V, I_D = −10μA
I_{DSS}	Drain Leakage Current	—	−0.1	−1.0	—	—	−10	nA	V_{DS} = −20V, V_{GS} = 0V
I_{SDS}	Source Leakage Current	—	−0.1	−1.0	—	—	−10	nA	V_{SD} = −20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	—	−0.1	−1.0	—	—	−1.0	nA	V_{GS} = −20V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−3.0	−7.0	—	−3.0	−7.0	—	mA	V_{GS} = V_{DS} = −15V
BV_{DSS}	Drain-Source Breakdown	−50	−65	—	−45	—	—	Volts	I_D = −10μA, V_{GS} = 0V
BV_{SDS}	Source-Drain Breakdown	−50	−65	—	−45	—	—	Volts	I_S = −10μA, V_{GS} = 0V
BV_{GSS}	Gate-Source Breakdown	−50	−70	—	−45	—	—	Volts	I_G = −10μA
Y_{fs}	Transadmittance	800	950	—	700	950	—	μmho	V_{DS} = −20V, f = 1kHz I_{DS} = −5mA
C_{gs}	Gate to Source Capacitance	—	0.3	0.5	—	—	0.7	pF	V_{GS} = V_{DS} = −10V, f = 1MHz
C_{gd}	Gate to Drain Capacitance	—	0.3	0.5	—	—	0.7	pF	V_{GS} = V_{DS} = −10V, f = 1MHz
C_{ds}	Drain to Source Capacitance	—	.08	—	—	.08	—	pF	V_{GS} = V_{DS} = −10V, f = 1MHz
$r_{DS(on)}$	Drain to Source Resistance	—	700	1000	—	700	1200	ohms	V_{GS} = −15V, I_{DS} = −100μA

TO-72



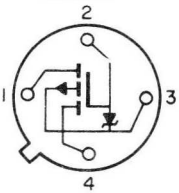
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

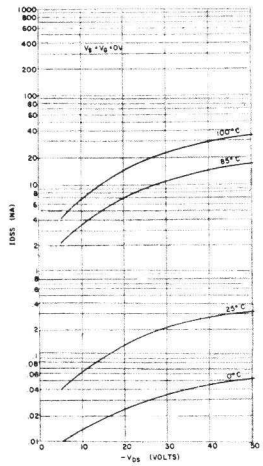
Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source

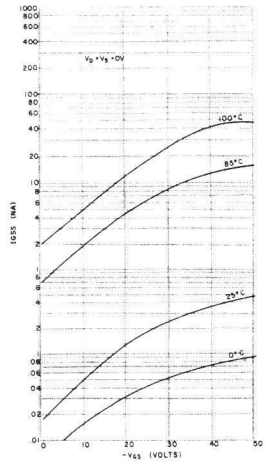


TYPICAL CHARACTERISTIC CURVES

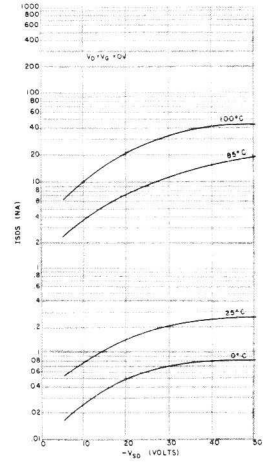
DRAIN LEAKAGE vs DRAIN VOLTAGE



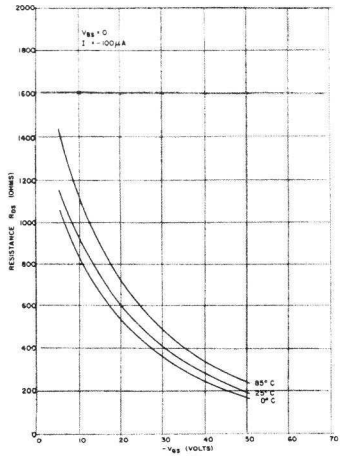
GATE LEAKAGE vs GATE VOLTAGE



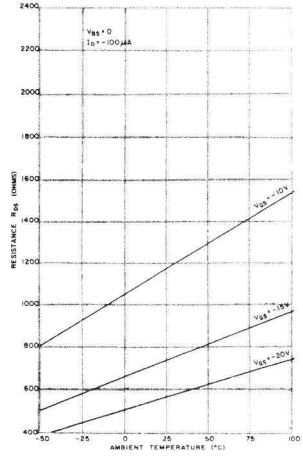
SOURCE LEAKAGE vs SOURCE VOLTAGE



DRAIN RESIRTANCE vs GATE VOLTAGE



DRAIN RESISTANCE vs TEMPERATURE



INDUSTRIAL/ MOSFET

MEM 557

N-Channel Depletion Mode MOSFET

FEATURES

- 10^{15} ohms input resistance
- Low 3_{rd} order distortion
- High gain — low noise through VHF range
- Low feedback capacitance 0.32 pF typ.
- Square law response

APPLICATIONS

- TV Tuners
- FM Tuners
- IF Amplifiers
- SSB Amplifiers
- Wideband Amplifiers
- High Frequency Analog Switching

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain-to-Source voltage, V_{DS}	+20V
Gate-to-Source voltage, V_{GS}	±30V
Gate-to-Drain voltage, V_{DG}	±30V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−65 to +150°C
Operating Junction Temperature	−65 to +150°C
Total Dissipation at 25°C Case Temperature	300 mW
Total Dissipation at 25°C Ambient Temperature	150 mW
at 100°C Ambient Temperature	150 mW

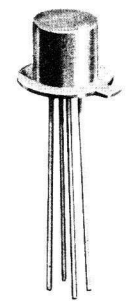
Derate Linearly from 100°C to 150°C at 3 mW/°C

ELECTRICAL CHARACTERISTICS

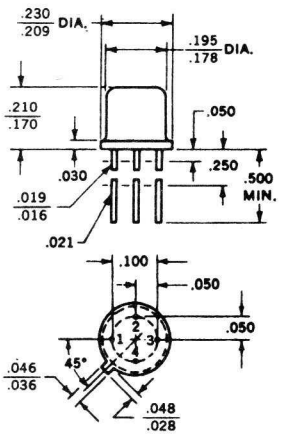
(T_A = 25°C, unless otherwise specified — body grounded)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage drain to source	20	—	—	V	V_{GS} = −4V, I_D = 100μA
I_{GSS}	Gate Leakage Current	—	—	0.10	nA	V_{GS} = ±10V
I_D (off)	Drain to Source Leakage Current	—	—	100	μA	V_{DS} = +15V, V_{GS} = −4.0V
I_{DSS}	Zero signal Gate voltage drain current	3.0	—	30	mA	V_{DS} = +15V, V_{GS} = 0V
V_G (off)	Gate-Source Cutoff Voltage	−0.3	−2.0	−4.0	V	V_{DS} = +15V, I_D = 100 .A
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	3.0	5.0	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{oss}	Small-signal, short circuit drain-to-source	—	2.0	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	0.32	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 1 MHz
G_{fs}	Forward trans-conductance	8000	10000	—	μmhos	V_{DS} = +15V, I_D = 10mA*, f = 1 kHz
G_{ps}	Power gain for measurements circuits	16	18	—	dB	V_{DS} = +15V, V_{GS} = 1.7V, f = 200 MHz, R_s = 270Ω
NF	Noise Figure**	—	2.5	4.0	dB	V_{DS} = +15V, V_{GS} = 1.7V, f = 200 MHz, R_s = 270Ω
$rd_{s(on)}$	Drain to Source on resistance	—	200	300	Ω	V_{GS} = 0V I_D = 0.1mA

*V_{GIS} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.



TO-72



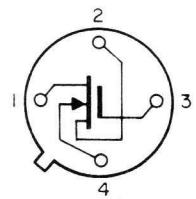
Bottom view

Note: All dimensions in inches.

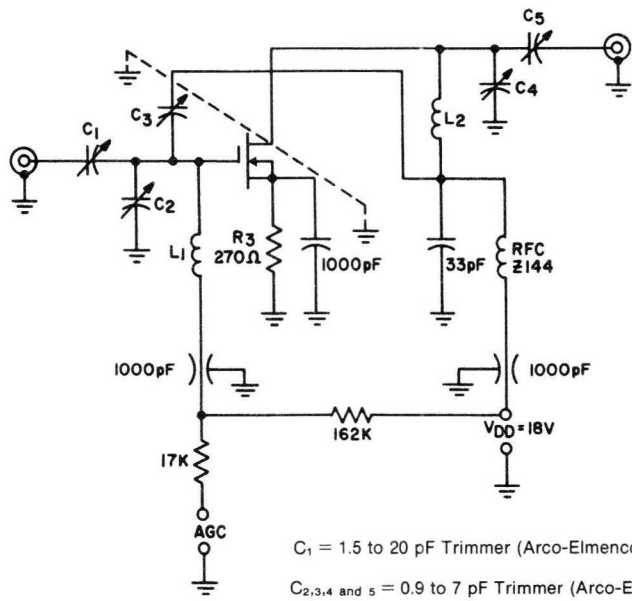
TERMINAL DIAGRAM

LEAD

1. Drain
2. Source
3. Gate
4. Substrate and case



POWER GAIN TEST JIG @ 200MHz FOR MEM 557 WITH NEUTRALIZING



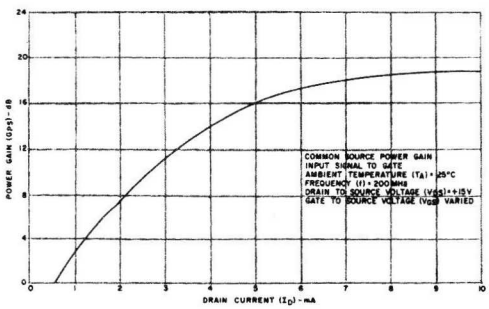
C_1 = 1.5 to 20 pF Trimmer (Arco-Elmenco #400)

$C_{2,3,4 \text{ and } 5}$ = 0.9 to 7 pF Trimmer (Arco-Elmenco #402)

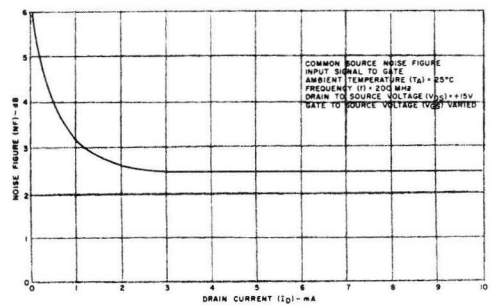
L_1 = 5 Turns #22 Wire 1/8" Dia. & 1/8" Spacing

L_2 = 4 Turns #22 Wire 1/4" Dia. & 1/8" Spacing

POWER GAIN vs DRAIN CURRENT



NOISE FIGURE vs DRAIN CURRENT



MEM 557C

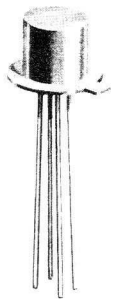
N-Channel Depletion Mode MOSFET

FEATURES

- 10^{15} ohms input resistance
- Low 3_{rd} order distortion
- High gain — low noise through VHF range
- Low feedback capacitance 0.32 pF typ.
- Square law response

APPLICATIONS

- TV Tuners
- FM Tuners
- IF Amplifiers
- SSB Amplifiers
- Wideband Amplifiers
- High Frequency Analog Switching



MAXIMUM RATINGS (T_A = 25° C, unless otherwise specified)

Drain-to-Source Voltage	+20V
Gate-to-Source Voltage	±30V
Gate-to-Drain Voltage	±30V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−50 to +150°C
Operating Junction Temperature	−50 to +125°C
Total Dissipation at 25°C Case Temperature	300 mW
Total Dissipation at 25°C Ambient Temperature	150 mW
at 100°C Ambient Temperature	150 mW

Derate Linearly from 100°C to 125°C at 6 mW/°C

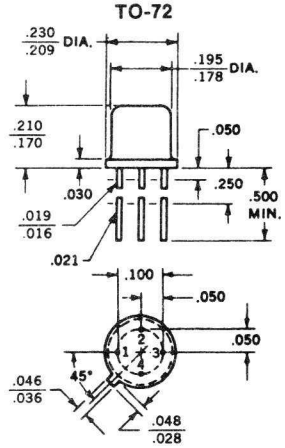
ELECTRICAL CHARACTERISTICS

(T_A = 25° C, unless otherwise specified — body grounded)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage Drain-to-Source	20	—	—	V	V_{GS} = −4V, I_D = 100μA
I_{GSS}	Gate Leakage Current	—	—	0.10	nA	V_{GS} = ±10V
$I_{D(off)}$	Drain-to-Source Leakage Current	—	—	100	μA	V_{DS} = +15V, V_{GS} = −4.0V
I_{DSS}	Zero signal Gate voltage drain current	3.0	—	30	mA	V_{DS} = +15V, V_{GS} = 0V
$V_{G(off)}$	Gate-Source Cutoff Voltage	−0.3	−2.0	−4.0	V	V_{DS} = +15V, I_D = 100μA
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	3.0	5.0	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{oss}	Small-signal, short circuit drain-to-source	—	2.0	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	0.32	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 1 MHz
G_{fs}	Forward trans-conductance	6000	8000	—	μmhos	V_{DS} = +15V, I_D = 10mA*, f = 1 kHz
G_{ps}	Power gain for measurements circuits	15	17	—	dB	V_{DS} = +15V, V_{GS} = +1.7V, f = 200 MHz, R_S = 270Ω
NF	Noise Figure**	—	3.0	4.5	dB	V_{DS} = +15V, V_G = +1.7V, f = 200 MHz, R_S = 270Ω
$R_{DS(ON)}$	Drain to Source on resistance	—	200	300	ohms	V_{GS} = 0V, I_D = 0.1mA

*V_{GIS} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72



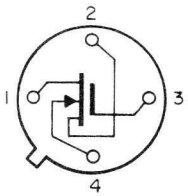
Bottom view

Note: All dimensions in inches.

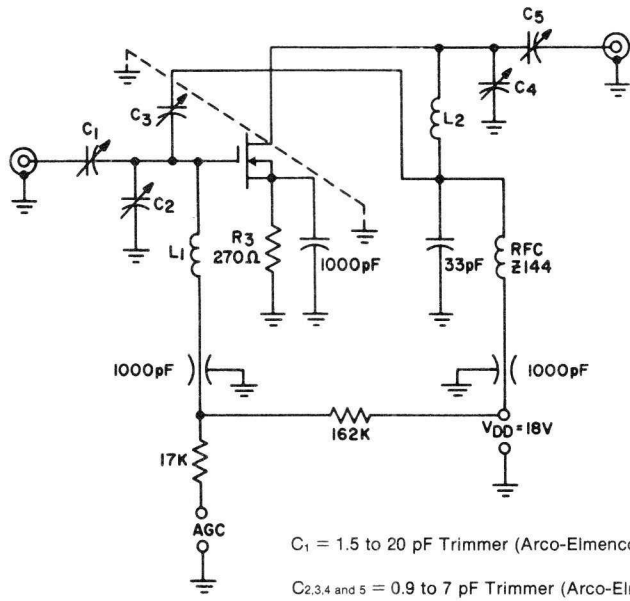
TERMINAL DIAGRAM

LEAD

1. Drain
2. Source
3. Gate
4. Substrate and case



POWER GAIN TEST JIG @ 200 MC FOR MEM 557 C WITH NEUTRALIZING



C_1 = 1.5 to 20 pF Trimmer (Arco-Elmenco #400)

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L_1 = 5 Turns #22 Wire 1/8" Dia. & 1/8" Spacing

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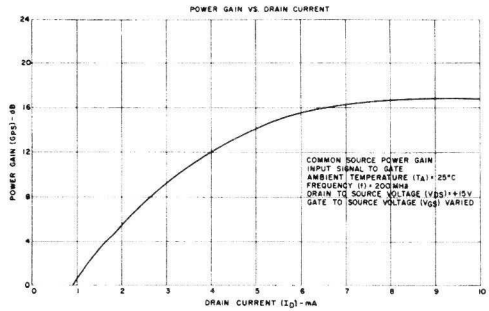
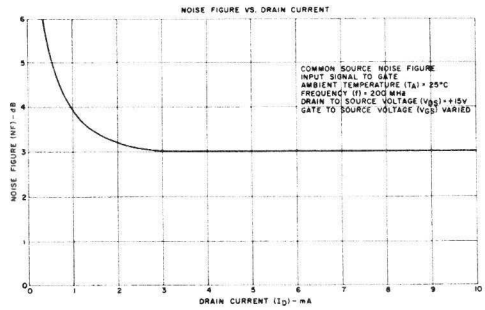
POWER GAIN vs DRAIN CURRENT



NOISE FIGURE vs DRAIN CURRENT



INDUSTRIAL/ MOSFET

P-Channel Enhancement Mode MOSFETS

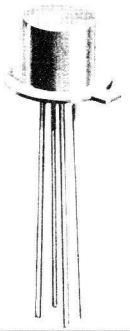
FEATURES

- Low Threshold Voltage
- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

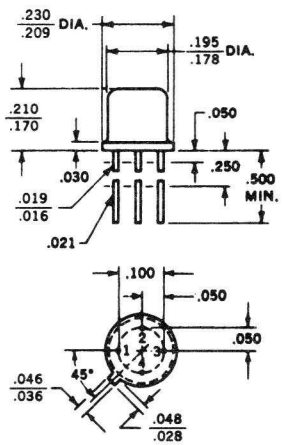
APPLICATIONS

(Designed Primarily for Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications.)

- Analog switches
- Series and Shunt Choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers



TO-72



Bottom view

Note: All dimensions in inches.

MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified)

	MEM 560	MEM 560C
Drain-to-Source Voltage	−35V	−30V
Gate-to-Source Voltage	−35V	−30V
Gate-to-Drain Voltage	−35V	−30V
Drain Current	−50mA	−50mA
Gate Current (Forward Direction for Zener Clamp)	+0.1mA	+0.1mA
Storage Temperature	−65 to+150°C	−50 to +125°C
Operating Junction Temperature	−65 to+125°C	−50 to +100°C
Total Dissipation at 25°C Case Temperature	900mW	600mW
Total Dissipation at 25°C Ambient Temperature	300mW	200mW

ELECTRICAL CHARACTERISTICS

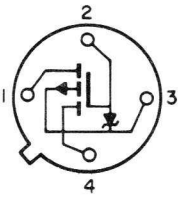
(T_A = 25°C, unless otherwise specified — body grounded)

		MEM 560			MEM 560C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Units	Conditions
$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5	−2.0	−3.0	−1.0	−2.5	−3.5	V	V_{DS} = V_{DS}, I_D = −10μA, V_{BS} = 0V
I_{DSS}	Drain Leakage Current	—	—	−5.0	—	—	−10	nA	V_{DS} = −20V, V_{GSB} = 0V
I_{SDS}	Source Leakage Current	—	—	−5.0	—	—	−10	nA	V_{SD} = −20V, V_{GDB} = 0V
I_{GSS}	Gate Leakage Current	—	—	−500	—	—	−1000	pA	V_{GS} = −20V, V_{DSB} = 0V
BV_{DSS}	Drain-Source Breakdown Voltage	−35	—	—	−30	—	—	V	I_D = −10μA, V_{GSB} = 0V
BV_{SDS}	Source-Drain Breakdown Voltage	−35	—	—	−30	—	—	V	I_S = −10μA, V_{GDB} = 0V
BV_{GSS}	Gate-Source Breakdown Voltage	−35	—	—	−30	—	—	V	I_G = −10μA, V_{DSB} = 0V
$I_{D(ON)}$	Drain Current	−15	−20	—	−10	−15	—	mA	V_{GS} = V_{DS} = −10V, V_{BS} = 0V
$R_{ds(on)}$	Drain-Source Resistance	—	100	150	—	175	250	ohms	V_{GS} = −15V, I_{DS} = −0.1mA, V_{BS} = 0V
Y_{fs}	Transadmittance	2000	3500	—	2000	3000	—	umhos	V_{DS} = −10V, I_D = −5mA, V_{BS} = 0V, f = 1kHz
C_{iss}	Input Capacitance	—	7.5	9.0	—	—	11	pF	V_{DS} = −10V, I_D = −5mA, V_{BS} = 0V, f = 1MHz
C_{oss}	Output Capacitance	—	5.5	6.5	—	—	8.5	pF	V_{DS} = −10V, I_D = −5mA, V_{BS} = 0V, f = 1MHz
C_{gd}	Drain-Gate Capacitance	—	3.0	3.5	—	—	4.5	pF	V_{DS} = −10V, I_D = −5mA, V_{BS} = 0V, f = 1MHz

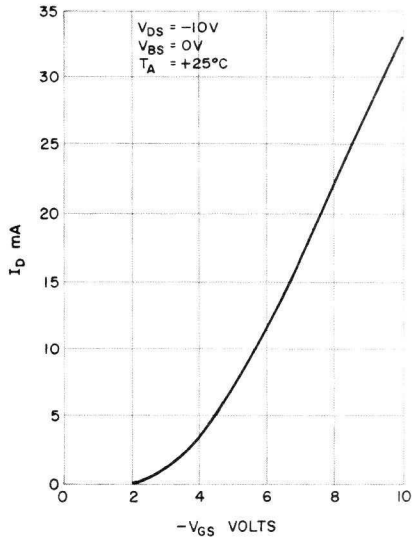
TERMINAL DIAGRAM

Lead

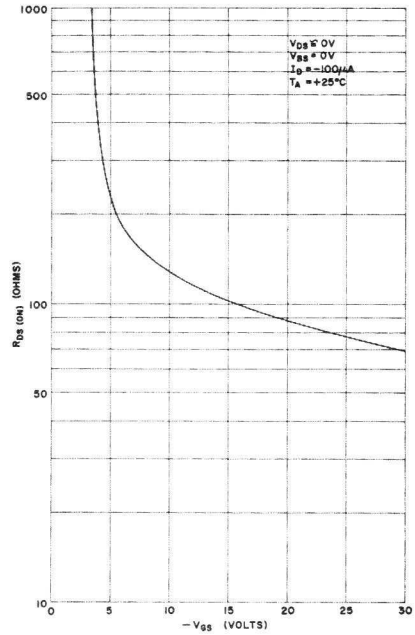
1. Drain
2. Gate
3. Substrate (Case)
4. Source



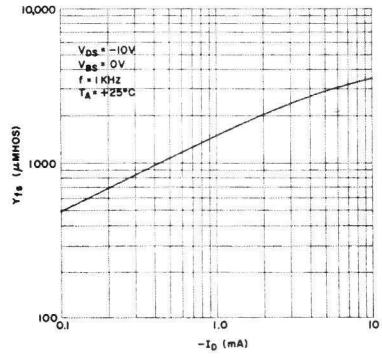
DRAIN CURRENT vs GATE VOLTAGE TRANSFER CHARACTERISTICS



DRAIN RESISTANCE vs GATE VOLTAGE



FORWARD TRANSADMITTANCE vs DRAIN CURRENT



MEM 561 **MEM 561C**

P-Channel Enhancement Mode MOSFETS

FEATURES

- Low Threshold Voltage
- 10^{15} ohms input resistance
- Normally off with zero gate voltage
- Square law transfer characteristics

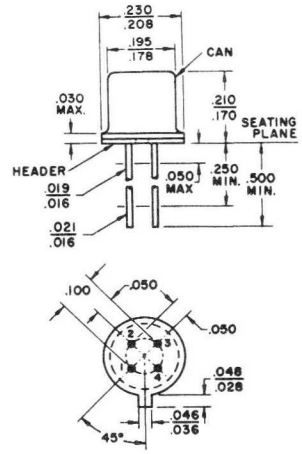
APPLICATIONS

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Multiplexes
- Sample and hold circuits
- Logic circuits
- Linear RF amplifiers

MAXIMUM RATINGS

	MEM 561	MEM 561C
Drain to Source Voltage	−30V	−25V
Source to Drain Voltage	−30V	−25V
Drain Current	−50mA	−50mA
Storage Temperature Range	−65 to +150°C	
Operating Temperature Range	−65 to +125°C	
Total Dissipation	225mW	

TO-72

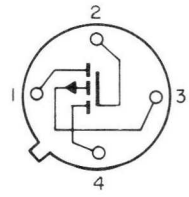


BOTTOM VIEW

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Substrate (Case)
4. Source



ELECTRICAL CHARACTERISTICS

		MEM 561			MEM 561C				
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Gate-Source Threshold Voltage	$V_{GS(th)}$	−1.5	−2.0	−3.0	−1.5	−2.0	−3.0	V	$V_{GS} = V_{DS}$, $I_D = -10ua$, $V_{BS} = 0V$
Drain Leakage Current	I_{DSS}	—	—	−5.0	—	−0.5	−10	nA	$V_{DS} = -20V$, $V_{GSB} = 0V$
Source Leakage Current	I_{SDS}	—	—	−5.0	—	−0.5	−10	nA	$V_{SD} = -20V$, $V_{GDS} = 0V$
Gate Leakage Current	I_{GSS}	—	—	−2.0	—	−0.5	−3	pA	$V_{GS} = -20V$, $V_{DSB} = 0V$
Drain-Source Breakdown Voltage	BV_{DSS}	−30	—	—	−25	−30	—	V	$I_D = -10uA$, $V_{GS} = 0V$
Source-Drain Breakdown Voltage	BV_{SDS}	−30	—	—	−25	−30	—	V	$I_S = -10uA$, $V_{GD} = 0V$
Drain Current	$I_{D(on)}$	−15	—	—	−10	−30	—	mA	$V_{GS} = V_{DS} = -10V$, $V_{BS} = 0V$
Drain-Source Resistance	$R_{ds(on)}$	—	—	150	—	150	200	Ohms	$V_{GS} = -15V$, $I_{DS} = 0.1mA$, $V_{BS} = 0V$, f = 1kHz
Transadmittance	Y_{fs}	2000	3500	—	2000	3500	—	μmhos	$V_{DS} = -10V$, $I_D = -10mA$, $V_{BS} = 0V$, f = 1kHz
Input Capacitance	C_{iss}	—	7.5	9.0	—	7.5	9.0	pF	$V_{DS} = -10V$, $I_D = -10mA$, $V_{BS} = 0V$, f = 1kHz
Output Capacitance	C_{oss}	—	5.5	6.5	—	5.5	6.5	pF	$V_{DS} = -10V$, $I_D = -10mA$, $V_{BS} = 0V$, f = 1kHz
Drain-Gate Capacitance	C_{gd}	—	3.0	3.5	—	3.0	3.5	pF	$V_{DS} = -10V$, $I_D = -10mA$, $V_{BS} = 0V$, f = 1kHz

N-Channel Enhancement Mode MOSFETS

FEATURES

- 10^{13} ohms input resistance
- Normally off with zero gate voltage
- Square Law transfer characteristics
- Low insertion loss
- Low input and output capacitance

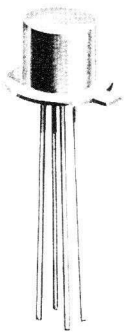
APPLICATIONS

- Logic circuits
- Switches
- Choppers
- Multiplexers
- Audio/RF Amplifier, Oscillators
- Operational Amplifiers

MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

	MEM 562	MEM 562C
Drain to Source Voltage	+20 Volts	+20 Volts
Gate to Source Voltage	±10 Volts	±10 Volts
Gate to Drain Voltage	±30 Volts	±30 Volts
Drain Current I_D	Limited by Dissipation	Limited by Dissipation
Storage Temperature	−65 to 150°C	−50 to 125°C
Operating Junction Temperature	−65 to 125°C	−50 to 100°C
Total Dissipation		
@ 25°C Ambient Temperature	225mW	175 mW
@ 25°C Case Temperature	650mW	500 mW
Derate Linearly From	T_a = 25°C to 125°C @ 2.25mW/°C T_c = 25°C to 125°C @ 6.5mW/°C	



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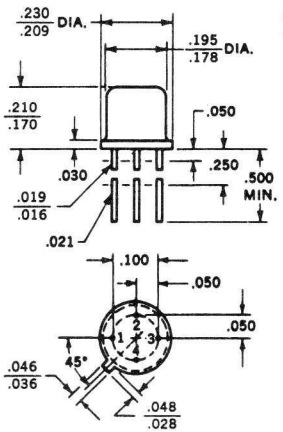


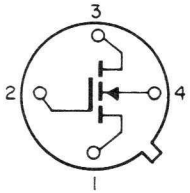
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

LEAD

1. Source
2. Gate
3. Drain
4. Substrate, case

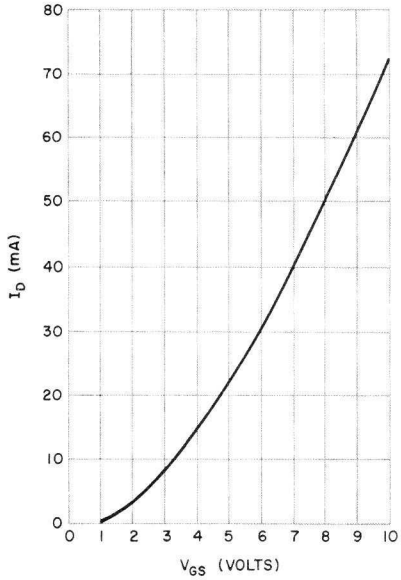


ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

		MEM 562			MEM 562C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Units	Conditions
$V_{GS(TH)}$	Gate to Source Threshold Voltage	0.50	1.5	4.0	0.50	1.5	4.0	V	$V_{DS} = V_{GS}$, $I_D = +10\mu A$
I_{DSS}	Drain Leakage Current	—	—	10	—	—	10	nA	$V_{DS} = +10V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current	—	—	10	—	—	100	pA	$V_{GS} = \pm 10V$, $V_{DS} = 0V$
BV_{DSS}	Drain Breakdown Voltage	20	—	—	20	—	—	V	$I_D \leq +10\mu A$, $V_{GS} = 0V$
$R_{DS(ON)}$	Drain to Source on Resistance	—	150	300	—	150	350	ohms	$V_{GS} = +10V$, $I_D = 0.1mA$
$I_{D(ON)}$	Drain Current	5	15	—	5.0	15	—	mA	$V_{DS} = V_{GS} = +10V$
Y_{fs}	Forward Transadmittance	1000	—	—	1000	—	—	μmhos	$V_{DS} = +10V$, $I_D = 2mA$, f = 1kHz
C_{iss}	Total Gate Input Capacitance	—	3.0	4.0	—	3.0	5.0	pF	$V_{GS} = 0V$, $V_{DS} = +10V$, f = 1 MHz
C_{oss}	Total Drain Output Capacitance	—	3.0	4.0	—	3.0	5.0	pF	$V_{GS} = 0V$, $V_{DS} = +10V$, f = 1 MHz
C_{dg}	Gate to Drain Capacitance	—	0.3	0.5	—	0.3	0.6	pF	$V_{GS} = 0V$, $V_{DS} = 0V$, f = 1 MHz
t_d	Turn on Delay Time	—	—	45	—	—	55	nS	See Figure 1
t_r	Rise Time	—	—	65	—	—	75	nS	See Figure 1
$t_{(off)}$	Turnoff Time	—	—	160	—	—	170	nS	See Figure 1

DRAIN CURRENT vs GATE VOLTAGE TRANSFER CHARACTERISTICS



DRAIN TO SOURCE RESISTANCE vs GATE VOLTAGE

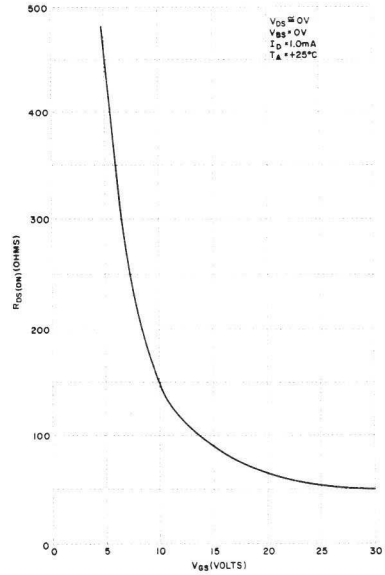
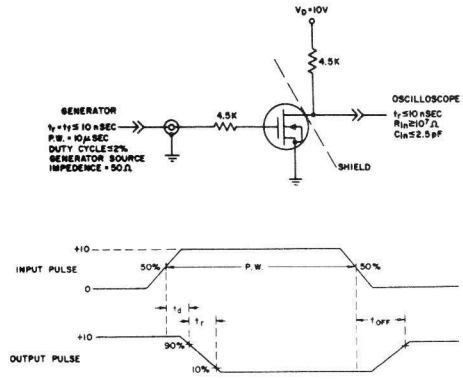
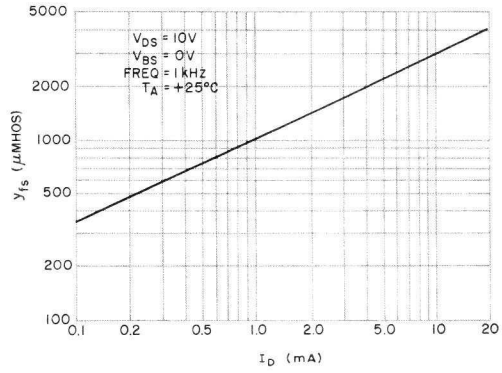


Fig. 1 SWITCHING TEST SET MEM 562/MEM 562C



FORWARD TRANSADMITTANCE vs DRAIN CURRENT



INDUSTRIAL/ MOSFET

MEM 563 **MEM 563C**

N-Channel Enhancement Mode MOSFETS

FEATURES

- Logic circuits
- Switches
- Choppers
- Multiplexers
- Audio/RF Amplifier, Oscillators
- Operational Amplifiers

APPLICATIONS

- 10^{13} ohms input resistance
- Normally off with zero gate voltage
- Square Law transfer characteristics
- Low insertion loss
- Low input and output capacitance

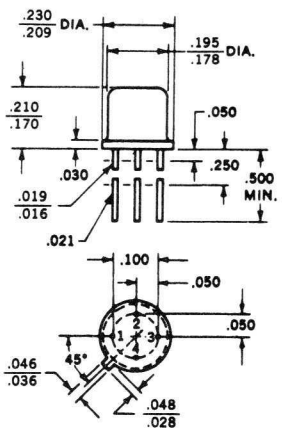
MAXIMUM RATINGS

Drain to Source Voltage ..... +20 V
Gate to Source Voltage ..... ±30 V
Gate to Drain Voltage ..... ±30 V
Drain Current I_D ..... Limited by Dissipation
Storage Temperature ..... −65 to 50°C
Operating Junction Temperature ..... −65 to 125°C
Total Dissipation @ 25°C Ambient Temperature 225mW
@ 25°C Case Temperature 650mW

ELECTRICAL CHARACTERISTICS

			MEM 563			MEM 563C			
Symbol	Characteristic	Conditions	Min	Typ	Max	Min	Typ	Max	Units
$V_{GX(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = +10\mu A$	0.50	1.5	4.0	0.50	1.5	4.0	V
I_{DSS}	Drain Leakage Current	$V_{DS} = +10V$, $V_{GS} = 0V$	—	—	10	—	—	10	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 10V$, $V_{DS} = 0V$	—	—	10	—	—	10	pA
BV_{DSS}	Drain Breakdown Voltage	$I_D \leq +10\ \mu A$, $V_{GS} = 0V$	20	—	—	20	—	—	V
$R_{DS(ON)}$	Drain-to-Source on Resistance	$V_{GS} = +10$, $I_D = 0.1mA$	—	50	100	—	—	150	Ω
$I_{D(ON)}$	Drain Current	$V_{DS} = V_{GS} = +10V$	15	40	—	15	40	—	mA
Y_{fs}	Forward Transadmittance	$V_{DS} = +10V$, $I_D = 2mA$, $f = 1kHz$	2000	—	—	2000	—	—	μmhos
C_{iss}	Total Gate Input Capacitance	$V_{GS} = 0V$, $V_{DS} = +10V$, $f = 1$ MHz	—	4.0	5.0	—	—	6.0	pF
C_{oss}	Total Drain Output Capacitance	$V_{GS} = 0V$, $V_{DS} = +10V$, $f = 1$ MHz	—	3.5	4.5	—	—	5.0	pF
C_{GD}	Gate-to-Drain Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$, $f = 1$ MHz	—	0.3	0.6	—	—	0.8	pF
t_d	Turn on Delay Time	See Figure 1	—	—	15	—	—	25	ns
t_r	Rise Time	See Figure 1	—	—	25	—	—	35	ns
$t_{(off)}$	Turnoff Time	See Figure 1	—	—	120	—	—	140	ns

TO-72



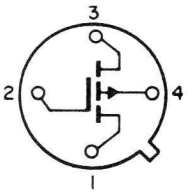
Bottom view

Note: All dimensions in inches.

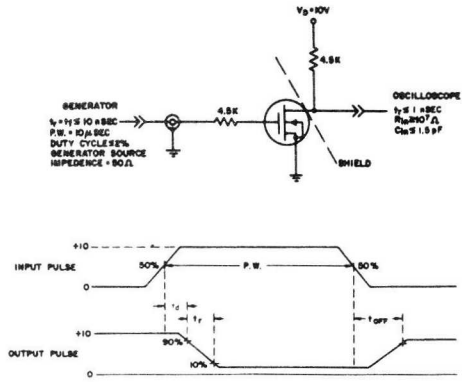
TERMINAL DIAGRAM

LEAD

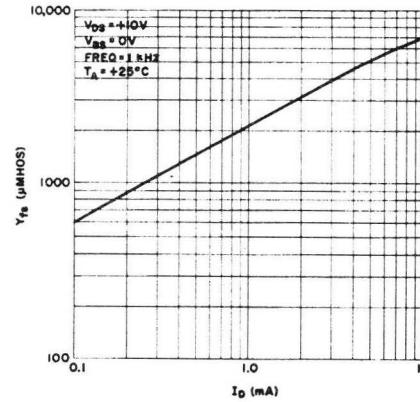
1. Source
2. Gate
3. Drain
4. Substrate, case



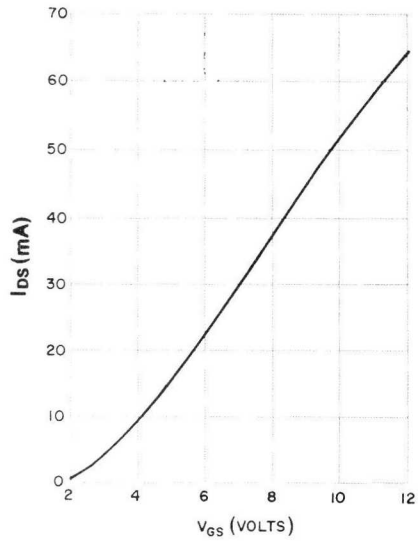
SWITCHING TEST SET MEM 563
FIGURE 1



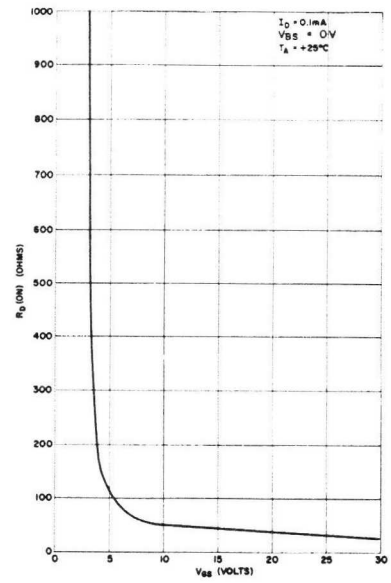
FORWARD TRANSADMITTANCE VS DRAIN CURRENT



DRAIN CURRENT VS GATE VOLTAGE TRANSFER CHARACTERISTICS



DRAIN TO SOURCE RESISTANCE VS GATE VOLTAGE



MEM 564C

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- Back-to-back zener diodes to protect gate
- Dual Gate Cascode operation
- Low 3rd order distortion
- Reverse AGC capability
- Linear mixing capability
- High gain—low noise through VHF range
- Low feedback capacitance—.025 pF typ.

APPLICATIONS

- TV Tuners (RF & Mixer)
- FM Tuners (RF & Mixer)
- IF Amplifiers
- Synchronous Detectors
- Wideband Amplifiers

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain-to-source voltage, V_{DS}	+20V
Gate No. 1-to-source voltage, V_{G1S}	±6.0V
Gate No. 2-to-source voltage, V_{G2S}	±6.0V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−50 to +150°C
Operating Junction Temperature	−50 to +125°C
Total Dissipation at 25°C Case Temperature	300mW
Total Dissipation at 25°C Ambient Temperature	225mW
at 100°C Ambient Temperature	150mW

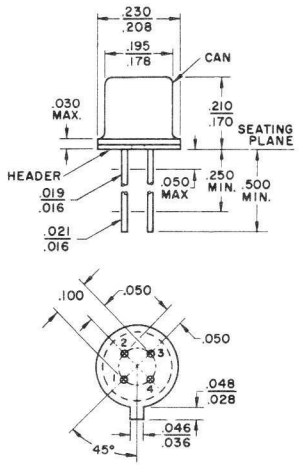
Derate Linearly from 100°C to 125°C at 6 mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage Drain-to-source	20	—	—	V	$V_{G1} = V_{G2} = -4.0V$, $I_D = 100uA$
BV_{G1SS}	Breakdown voltage Gate 1-to-source	±6.0	—	±15	V	$V_{DS} = V_{G2S} = 0V$, $I_{G1} = 100uA$
BV_{G2SS}	Breakdown voltage Gate 2-to-source	±6.0	—	±15	V	$V_{DS} = V_{G1S} = 0V$, $I_{G2} = 100uA$
I_{G1SS}	Gate No. 1 Leakage Current	—	—	10	nA	$V_{G1S} = \pm4.0V$, $V_{G2S} = V_{DS} = 0V$
I_{G2SS}	Gate No. 2 Leakage Current	—	—	10	nA	$V_{G2S} = \pm4.0V$, $V_{G1S} = V_{DS} = 0V$
$I_{D(off)}$	Drain-to-Source Leakage Current	—	—	100	µA	$V_{DS} = +20V$, $V_{G1} = V_{G2} = -4.0V$
$V_{G1S(off)}$	Gate No. 1-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G2S} = +4.0V$
$V_{G2S(off)}$	Gate No. 2-to-source cutoff voltage	—	−1.5	−4.0	V	$V_{DS} = +20V$, $I_D = 200uA$ $V_{G1S} = 0V$
I_{DSS}	Zero Signal Gate voltage drain current	3.0	—	30	mA	$V_{DS} = +15V$, $V_{G2} = +4.0V$ $V_{G1} = 0V$
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	5.0	8.0	pF	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$, f = 1.0MHz
C_{oss}	Small-signal, short circuit drain-to-source capacitance	—	2.5	—	pF	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$, f = 1.0MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	0.02	—	pF	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$, f = 1.0MHz
G_{fs}	Forward transconductance of gate No. 1	8000	12000	—	µmhos	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$, f = 1.0kHz
G_{ps}	Power gain (See Fig. 1 for measurements circuits)	15	17	—	dB	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$, f = 200MHz
NF	Noise Figure** (See Fig. 1 for Measurements Circuit)	—	3.5	5.0	dB	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$, f = 200MHz
E_{int}	Interfering signal level at gate for 1% Cross Modulation Distortion	—	120	—	mW	$V_{DS} = +15V$, $I_D = 10mA$* $V_{G2S} = +4.0V$ Desired frequency = 200MHz Undesired frequency = 150MHz Input untuned.

*V_{G1S} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

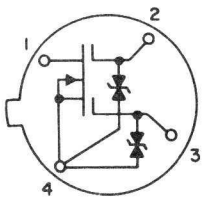
TO-72



Bottom view

NOTE: All dimensions in inches

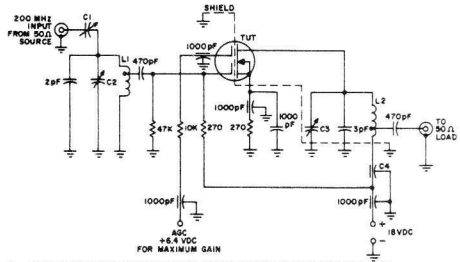
TERMINAL DIAGRAM



LEAD

1. Drain
2. Gate No. 2
3. Gate No. 1
4. Source, substrate and case

Fig. 1 200 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END.
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.
C1 0.4 TO 7pF (ARCO 400).
C2,C3 1.3 TO 9pF VARIABLE.
C4 1000pF BUTTON TYPE CAPACITOR.

Fig. 2 POWER GAIN vs. DRAIN CURRENT

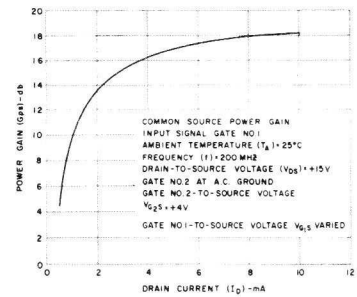


Fig. 3 NOISE FIGURE vs. DRAIN CURRENT

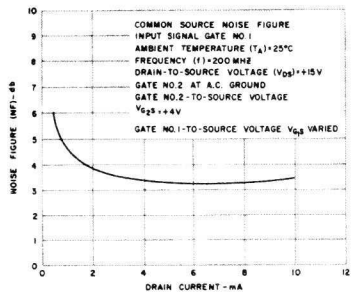


Fig. 4 GATE No. 2 GAIN CONTROL CURVE

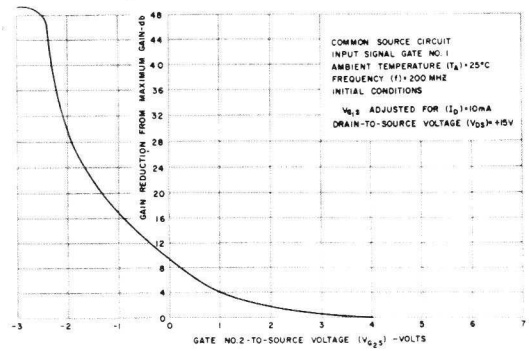


Fig. 5 NOISE FIGURE vs. GATE No. 2-TO-SOURCE VOLTAGE

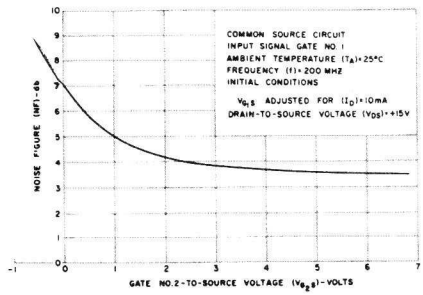
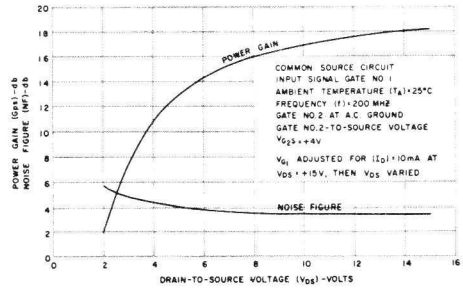


Fig. 6. POWER GAIN AND NOISE FIGURE vs. V_{DS}



INDUSTRIAL/ MOSFET

MEM 571C

N-Channel Depletion Mode MOSFET

FEATURES

- Back-to-Back Zener clamp to protect gate
- Low 3rd order distortion
- High gain—low noise through VHF range
- Low feedback capacitance 0.32 pF typ.
- Square law response

APPLICATIONS

- TV Tuners
- FM Tuners
- IF Amplifiers
- SSB Amplifiers
- Wideband Amplifiers
- High Frequency Analog Switching

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain-to-Source voltage, V_{DS}	+20V
Gate-to-Source voltage, V_{GS}	±6.0V
Drain-to-Gate voltage, V_{DG}	+30 to −6.0V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−65 to +150°C
Operating Junction Temperature	−65 to +150°C
Total Dissipation at 25°C Case Temperature	300 mW
Total Dissipation at 25°C Ambient Temperature	150 mW
at 100°C Ambient Temperature	150 mW

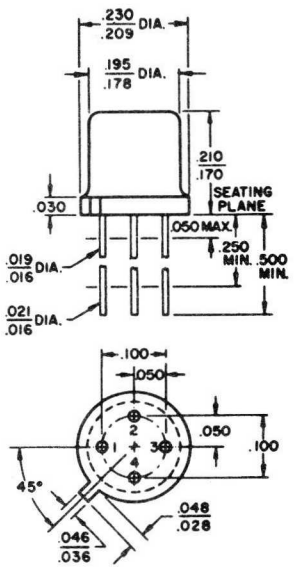
Derate Linearly from 100°C to 150°C at 3 mW/°C

ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Conditions
BV_{DSX}	Breakdown voltage drain to source	20	—	—	V	V_{GS} = −4.0V, I_D = 100μA
BV_{gss}	Breakdown voltage gate to source	±6.0	—	±15	V	V_{ds} = 0V, I_g = 100μA
I_{GSS}	Gate Leakage Current	—	—	±10	nA	V_{GS} = ±4.0V
$I_{D(off)}$	Drain to Source Leakage Current	—	—	100	μA	V_{DS} = +15V, V_{GS} = −4.0V
I_{DSS}	Zero signal Gate voltage drain current	3.0	—	30	mA	V_{DS} = +15V, V_{GS} = 0V
$V_{G(off)}$	Gate-Source Cutoff Voltage	−0.3	−2.0	−4.0	V	V_{DS} = +15V, I_D = 100μA
C_{iss}	Small-signal, short circuit gate Input Capacitance	—	4.0	6.0	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{oss}	Small-signal, short circuit drain-to-source	—	2.0	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	—	5.0	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
G_{fs}	Forward transconductance	8000	10000	—	μmhos	V_{DS} = +15V, I_D = 10mA*, f = 1.0 kHz
G_{ps}	Power gain for measurements circuits	15	17	—	dB	V_{DS} = +15V, V_{GS} = 1.7V, f = 200 MHz, R_L = 270Ω
NF	Noise Figure**	—	2.5	4.5	dB	V_{DS} = +15V, V_G = 1.7V, f = 200 MHz, R_L = 270Ω
$rd_{s(on)}$	Drain to Source on resistance	—	200	300	ohms	V_{GS} = 0V, I_D = 0.1mA

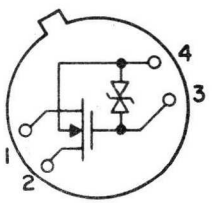
*V_{GS} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72



Bottom view
NOTE: All dimensions in inches

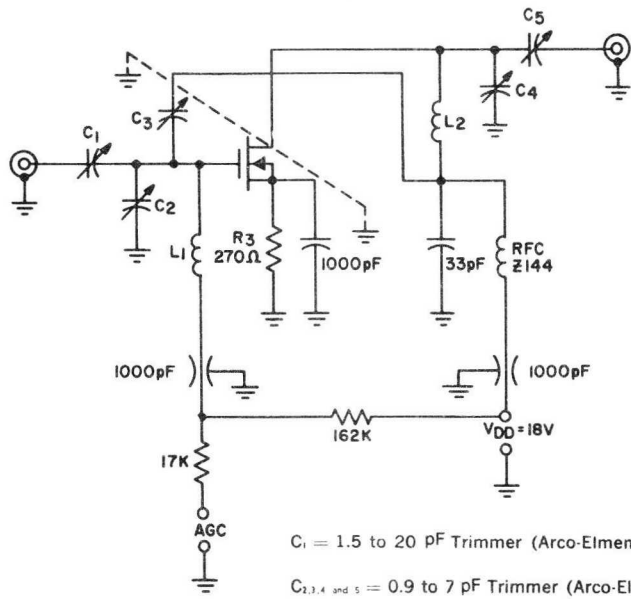
TERMINAL DIAGRAM



LEAD

1. Drain
2. Source
3. Gate
4. Substrate and case

Fig. 1 POWER GAIN TEST JIG @ 200 MHz FOR MEM 571C WITH NEUTRALIZING



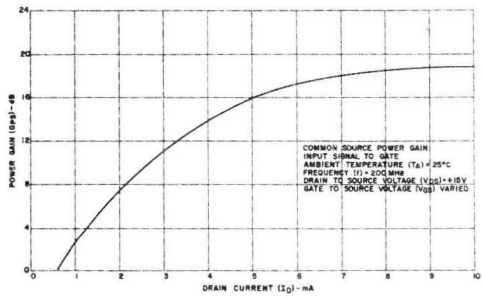
C_1 = 1.5 to 20 pF Trimmer (Arco-Elmenco #400)

$C_{2,3,4 \text{ and } 5}$ = 0.9 to 7 pF Trimmer (Arco-Elmenco #402)

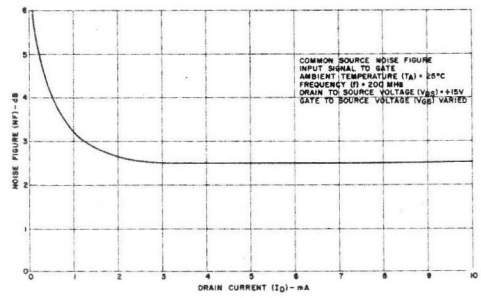
L_1 = 5 Turns #22 Wire 1/8" Dia. & 1/8" Spacing

L_2 = 4 Turns #22 Wire 1/4" Dia. & 1/8" Spacing

POWER GAIN VS. DRAIN CURRENT



NOISE FIGURE VS. DRAIN CURRENT



MEM 610

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain—Low Noise at HF
- Reverse AGC Capability
- Linear Mixers—Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

- CB Radio RF Amplifiers and Mixers
- CB Radio PLL Mixers
- IF Amplifiers

DESCRIPTION

The MEM 610 is an N-channel, Depletion-Mode Dual-Gate, Metal-Oxide semiconductor Field Effect Transistor. It is protected from excessive input voltages by integrated monolithic back-to-back diodes between the gates and source.

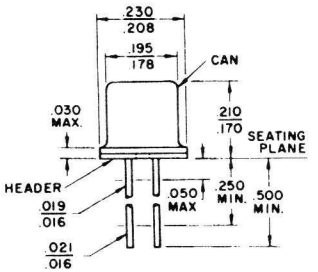
The MEM 639 is specially designed for use in CB radios as an RF amplifier or mixer where large signal handling capability, minimum cross-modulation and intermodulation distortion and low noise operation are required.

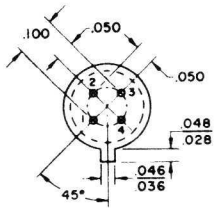
The MEM 610 is also recommended for use as a PLL mixer where large amplitude from a reference oscillator and VCO can be applied separately to the gates while exhibiting good isolation.

MAXIMUM RATINGS

DRAIN-SOURCE VOLTAGE	25V
DRAIN-GATE NO. 1 VOLTAGE	25V
DRAIN-GATE NO. 2 VOLTAGE	25V
DRAIN CURRENT	50mA
TRANSISTOR DISSIPATION, P_T AT 25°C	360mW
ABOVE 25°C, DERATE LINEARLY	2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS	265°C
STORAGE TEMPERATURE RANGE	−65°C to +175°C

TO-72

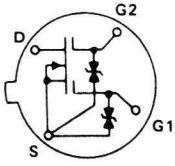




Bottom view

TERMINAL DIAGRAM

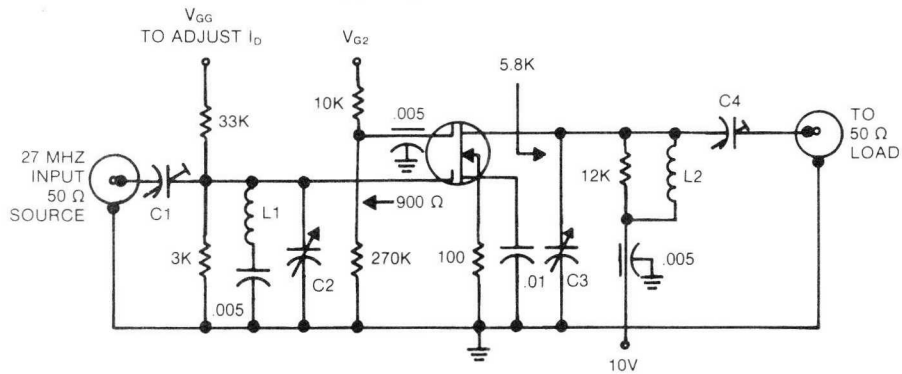
1–DRAIN
2–GATE #2
3–GATE #1
4–SOURCE/SUBSTRATE



ELECTRICAL CHARACTERISTICS

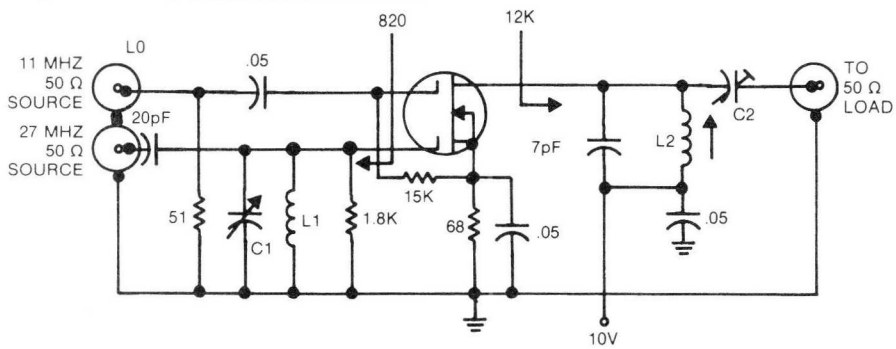
SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 100\mu A$, $V_{G1S} = V_{G2S} = 4V$	20	—	+15	v
BV_{G1SS}	Gate 1—Source Breakdown Voltage	$I_{G1S} = 10\mu A$, $V_{DS} = V_{G2S} = 0V$	+6	—	+15	v
BV_{G2SS}	Gate 2—Source Breakdown Voltage	$I_{G2S} = 10\mu A$, $V_{DS} = V_{G1S} = 0V$	+6	—	−6	v
$V_{G1S(off)}$	Gate 1—Source Cutoff Voltage	$I_D = 200\mu A$, $V_{DS} = 15V$, $V_{G2S} = 4V$	—	−1.5	−6	v
$V_{G2S(off)}$	Gate 2—Source Cutoff Voltage	$I_D = 200\mu A$, $V_{DS} = 15V$, $V_{G1S} = 0V$	—	−1.5	30	v
I_{DSS}	Gate 2—Voltage Drain Current	$V_{DS} = 15V$, $V_{G1S} = 0V$, $V_{G2S} = 4V$	10	10	—	mA
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, f = 1.0MHz	—	.03	7.0	pF
C_{iss}	Input Capacitance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, f = 1.0MHz	—	5.0	—	pF
C_{oss}	Output Capacitance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, f = 1.0MHz	—	2.5	—	pF
Y_{fs}	Magnitude of Fwd Transadmittance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, f = 1.0kHz	—	17	—	mmho
G_{ps}	Power Gain	See Figure 1, $I_D = 6mA$, $V_{G2} = 5V$	—	25	—	dB
N F	Noise Figure	See Figure 2 Injection voltage = 1V	—	4.5	—	dB
G_c	Conversion Power Gain	Injection voltage = 100mV	—	17	—	dB
			—	3		dB

Fig. 1—27 MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L_1 18 TURNS NO 24 ENAMEL WIRE ON 7/32" DIAM. CORE.
L_2 25 TURNS NO 24 ENAMEL WIRE ON 7/32" DIAM. CORE.
C_1, C_4 1.5 TO 2.0pF TRIMMER.
C_2, C_3 AIR VARIABLE CAPACITOR 20pF MAX.

Fig. 2—27 MHz TO 16 MHz CONVERSION GAIN TEST CIRCUIT



L_1 25 TURNS NO 24 ENAMEL WIRE ON 7/32" DIAM. CORE.
L_2 10.7 MHZ IF TRANSFORMER, R_t = 30K AT 16 MHZ.
C_1 AIR VARIABLE CAPACITOR 20 pF MAX.
C_2 1.5 TO 20pF TRIMMER.

MEM 614

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- Back-to-back zener diodes to protect gate
- Dual Gate Cascode operation
- Low 3rd order distortion
- Reverse AGC capability
- Linear mixing capability
- High gain—low noise through VHF range
- Low feedback capacitance—.025 pF typ.

APPLICATIONS

- FM Tuners (RF & Mixer)
- IF Amplifiers
- Synchronous Detectors
- Wideband Amplifiers
- Use in commercial FM, CB, Aircraft and Marine Receivers, CATV & MATV

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain-to-source voltage, V_{DS}	+20V
Gate No. 1-to-source voltage, V_{G1S}	±6.0V
Gate No. 2-to-source voltage, V_{G2S}	±6.0V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−50 to +150°C
Operating Junction Temperature	−50 to +150°C
Total Dissipation at 25°C Case Temperature	300mW
Total Dissipation at 25°C Ambient Temperature	225mW
at 100°C Ambient Temperature	150mW
Derate Linearly from 100°C to 150°C at 3mW/°C	

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage Drain-to-source	20	—	—	V	$V_{G1} = V_{G2} = -4.0V$, $I_D = 100uA$
BV_{G1SS}	Breakdown voltage Gate 1-to-source	±6.0	—	—	V	$V_{DS} = V_{G2S} = 0V$, $I_{G1} = 10\mu A$
BV_{G2SS}	Breakdown voltage Gate 2-to-source	±6.0	—	—	V	$V_{DS} = V_{G1S} = 0V$, $I_{G2} = 10\mu A$
$V_{G1S(off)}$	Gate No. 1-to-source cutoff voltage	—	−1.0	−4.0	V	$V_{DS} = +15V$, $I_D = 200\mu A$ $V_{G2S} = +4.0V$
$V_{G2S(off)}$	Gate No. 2-to-source cutoff voltage	—	−1.0	−4.0	V	$V_{DS} = +15V$, $I_D = 200\mu A$ $V_{G1S} = 0V$
I_{DSS}	Zero Signal Gate voltage drain current	1.0	4.0	20.0	mA	$V_{DS} = +15V$, $V_{G2} = +4.0V$ $V_{G1} = 0V$
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	5.0	8.0	pF	$V_{DS} = +15V$, $I_D = 5mA$* $V_{G2S} = +4.0V$, f = 1.0MHz
C_{oss}	Small-signal, short circuit drain-to-source capacitance	—	2.5	—	pF	$V_{DS} = +15V$, $I_D = 5mA$* $V_{G2S} = +4.0V$, f = 1.0MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	0.02	—	pF	$V_{DS} = +15V$, $I_D = 5mA$* $V_{G2S} = +4.0V$, f = 1.0MHz
G_{fs}	Forward transconductance of gate No. 1	6000	10,000	—	μmhos	$V_{DS} = +15V$, $I_D = 5mA$* $V_{G2S} = +4.0V$, f = 1.0kHz
G_{ps}	Power gain (See Fig. 1 for measurement circuit)	18	22	—	dB	$V_{DD} = +20V$, $V_{GG} = +9.6V$, f = 105MHz
NF	Noise Figure** (See Fig. 1 for measurement circuit)	—	—	4.5	dB	$V_{DD} = +20V$, $V_{GG} = +9.6V$, f = 105MHz

*V_{G1S} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

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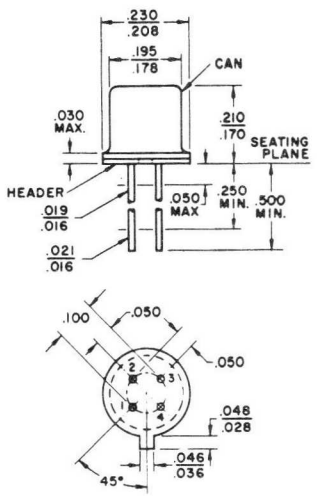
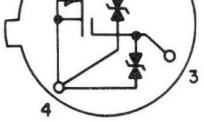


Bottom view
NOTE: All dimensions in inches

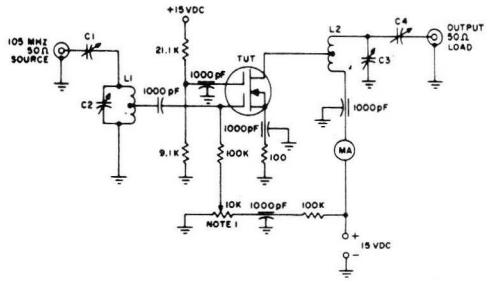
TERMINAL DIAGRAM



LEAD

1. Drain
2. Gate No. 2
3. Gate No. 1
4. Source, substrate and case

Fig. 1 105 MHz Power Gain and Noise Figure Test Circuit



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 4-1/2T. C_t = 17.8pF R_t = 15K AT 100MHz, MOUNTED.

L2 SAME AS L1, BUT R_t = 30K MOUNTED.

C1,C4 0.9 TO 7.0pF TRIMMER.

C2,C3 AIR VARIABLE CAPACITOR 20pF MAX.

NOTE 1: ADJUST 10K POT. FOR 6mA I_D.

Fig. 2 Power Gain vs. Drain Current

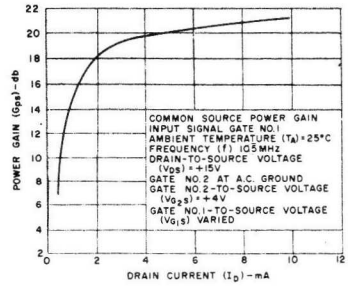


Fig. 3 Noise Figure vs. Drain Current

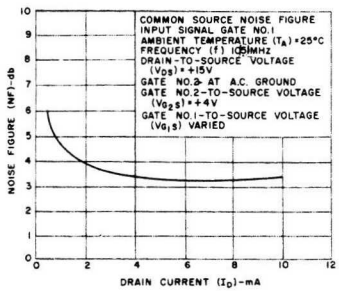


Fig. 4 Gate No. 2 Gain Control Curve

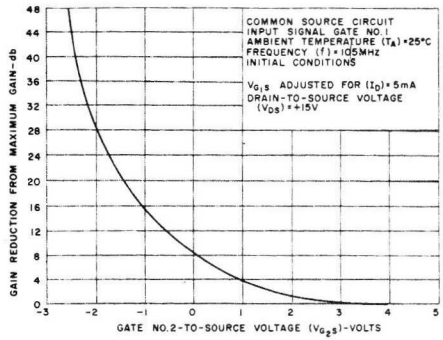


Fig. 5 Noise Figure vs. Gate No. 2-to-source voltage

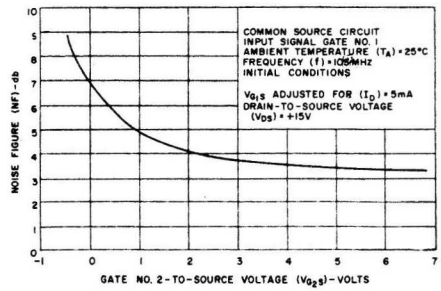
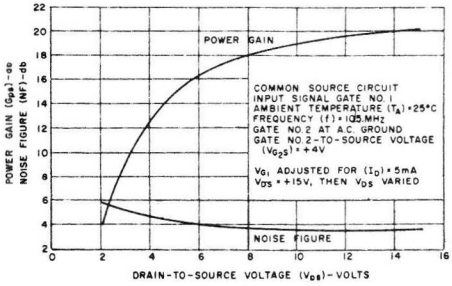


Fig. 6 Power Gain and Noise Figure vs. V_{DS}



MEM 616 MEM 617
MEM 618

Dual Gate N-Channel Depletion Mode MOSFETS

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain–Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers–Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

DESCRIPTION

The MEM 616 / MEM 617 / MEM 618 are N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

The MEM 616 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

The MEM 617 is intended for use in VHF mixers in television tuners where minimized cross-modulation, and inter-modulation distortion and low noise operation are required.

The MEM 618 is intended for use in tuned high frequency amplifiers such as TV IF. The low feedback capacitance permits high single stage gain and stability without neutralization.

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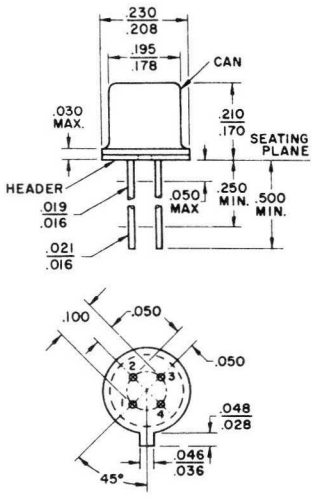
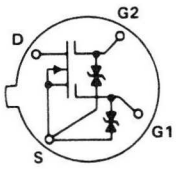


Bottom view

TERMINAL DIAGRAM

1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE/SUBSTRATE



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

DRAIN-SOURCE VOLTAGE, V_{DS} 25V
DRAIN-GATE NO. 1 VOLTAGE, V_{DG1} 25V
DRAIN-GATE NO. 2 VOLTAGE, V_{DG2} 25V
GATE NO. 1–SOURCE VOLTAGE, V_{G1S} ..... ±6V
GATE NO. 2–SOURCE VOLTAGE, V_{G2S} ..... ±6V
DRAIN CURRENT, I_D 50mA
TRANSISTOR DISSIPATION, P_T AT 25°C 360mW
ABOVE 25°C, DERATE LINEARLY ..... 2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS ..... 265°C
STORAGE TEMPERATURE RANGE ..... –65°C to +175°C

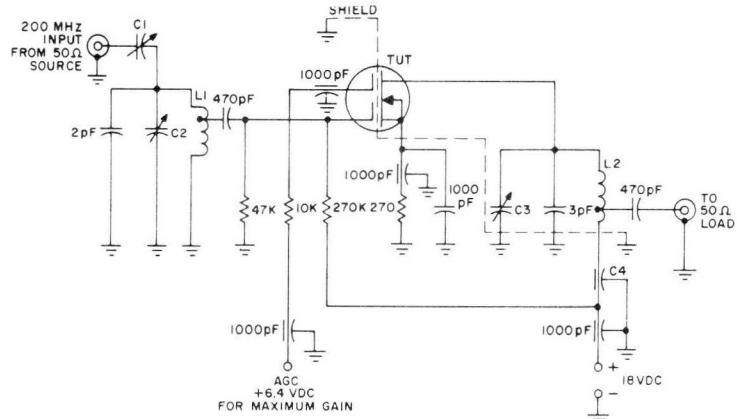
ELECTRICAL CHARACTERISTICS: (T_A = 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MEM 616			MEM 617			MEM 618			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=100μA, V_{G1S}=V_{G2S}=–4V	25	–	–	20	–	–	20	–	–	volts
BV_{G1SS}	Gate 1–Source Breakdown Voltage	I_{G1S}=10μA, V_{DS}=V_{G2S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	volts
BV_{G2SS}	Gate 2–Source Breakdown Voltage	I_{G2S}=10μA, V_{DS}=V_{G1S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	volts
$V_{G1S(off)}$	Gate 1–Source Cutoff Voltage	I_D=50μA, V_{DS}=15V, V_{G2S}=4V	–	–1.5	–	–	–1.0	–	–	–1.5	–	volts
$V_{G2S(off)}$	Gate 2–Source Cutoff Voltage	I_D=50μA, V_{DS}=15V, V_{G1S}=0V	–	–	–4.0	–	–	–4.0	–	–	–4.0	volts
I_{DSS}	Gate 2–Voltage Drain Current	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V	5.0[7]	–	30	2.0[7]	–	15	3.0[7]	–	20	mA
I_{G1SS}	Gate 1–Leakage Current	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
I_{G2SS}	Gate 2–Leakage Current	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz	.005	.02	.03	–	–	–	.005	.02	.03	pF
C_{iss}	Input Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	4.0	5.4	6.0	–	6.0	–	–	5.1	–	pF
C_{oss}	Output Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.2	–	–	2.5	–	–	2.5	–	pF
r_{iss}	Input Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	790	–	–	670	–	–	15k	–	Ω
r_{oss}	Output Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	1.25	–	–	17	–	–	18	–	kΩ
$\|Y_{fs}\|$	Magnitude of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	12	18	–	–	4.4	–	10	14	–	mmho
θ	Angle of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, see	–	–55	–	–	–	–	–	–13.6	–	degree
$\|Y_{rs}\|$	Magnitude of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, notes	–	30	–	–	–	–	–	5.5	–	μmho
θrs	Angle of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, 4,5,6	–	–30	–	–	–	–	–	90	–	degree
MAG	Maximum Available Power Gain	V_{DS}=+15V, V_{G2S}=+4V,	–	21	–	–	17.3[2]	–	–	39	–	dB
G_{ps}	Power Gain	V_{DS}=+15V, V_{G2S}=+4V,	16	18[1]	–	–	–	–	–	–	–	dB
MUG	Maximum Usable Power Gain	V_{DS}=+15V, V_{G2S}=+4V,	–	–	–	–	–	–	–	30[3]	–	dB
N.F.	Noise Figure	V_{DS}=+15V, V_{G2S}=+4V,	–	3.5	4.5	–	–	–	–	–	–	dB

NOTES:
1. See Figure 1.
2. Signal and local oscillator voltages, both are applied on Gate 1 with injection level equal to 500MV RMS (see Figure 2).
3. Unneutralized maximum usable gain for one stage (see Figure 3).
4. MEM 616 (RF AMP) I_D=10mA, f=200MHz.
5. MEM 617 (MIXER) V_{G1S}=0.1V, f=200MHz/44MHz.
6. MEM 618 (IF AMP) I_D=5mA, f=44MHz.
7. In addition to the standard range of I_{DSS}, the following I_{DSS} ranges are available:

Device	I_{DSS} Range (mA)	Color Code	Suggested Source Resistor (ohms)	Suggested Biasing (volts)
MEM616	5-13	Black Dot	150	V_{G1} = +1.5
R.F. Amplifier	11-22	Blue Dot	180	V_{G2S}= +4.0
	20-30	Red Dot	200	
MEM617	2-9	Black Dot	100	V_{G1} = +0.5
Mixer	7-15	Blue Dot	100	V_{G2} = +1.5
MEM618	3-9	Black Dot	270	V_{G1} = +1.0
I.F. Amplifier	7-14	Blue Dot	270	V_{G2S}= +4.0
	12-20	Red Dot	270	

Fig. 1 — 200MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END.

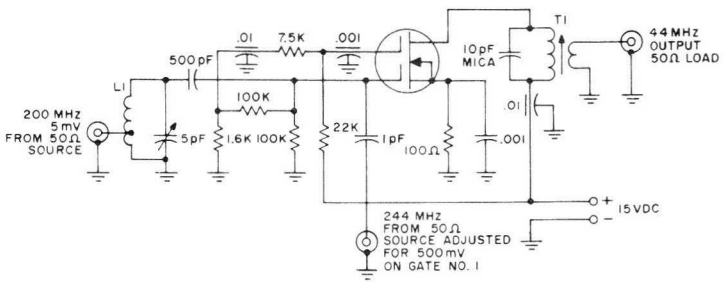
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.

C1 0.4 TO 7pF (ARCO 400).

C2,C3 1.3 TO 5pF VARIABLE.

C4 1000pF BUTTON TYPE CAPACITOR.

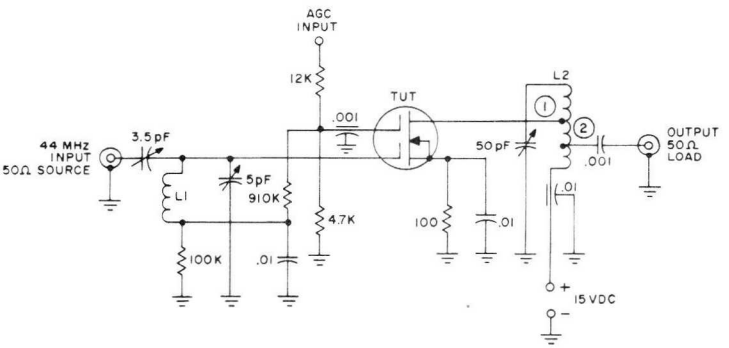
Fig. 2 — 200MHz TO 44MHz MIXER TEST CIRCUIT



L1 3T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG TAP AT 3/4T FROM COLD END.

T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM.
SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO.

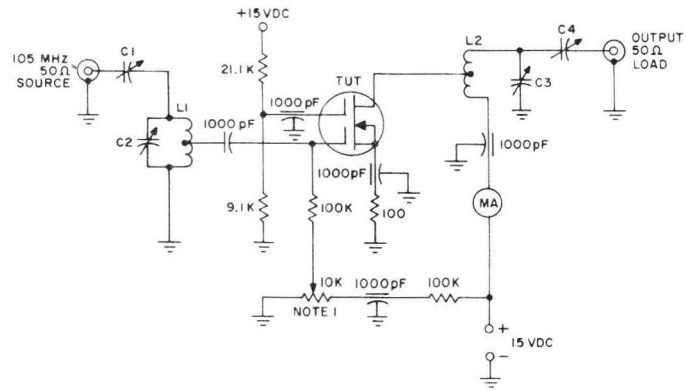
Fig. 3 — 44MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 14T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM. FORM.

L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG.
(1) DRAIN TAP 2-1/2T FROM COLD END.
(2) LOAD TAP 0.4T FROM COLD END.

Fig. 4 — 105MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 6T NO. 18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 4-1/2T. C_t = 17.8pF R_t = 15K AT 100MHz, MOUNTED.

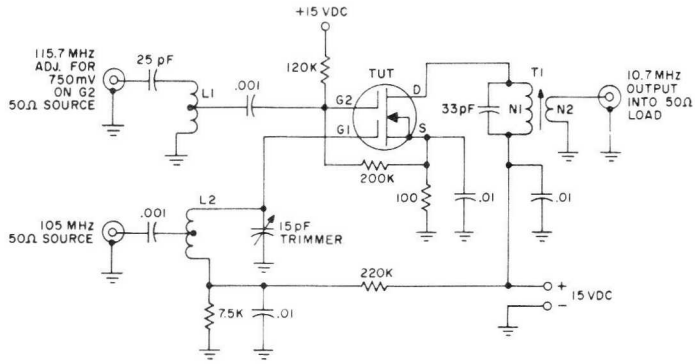
L2 SAME AS L1, BUT R_t = 30K MOUNTED.

C1, C4 0.9 TO 7.0pF TRIMMER.

C2, C3 AIR VARIABLE CAPACITOR 20pF MAX.

NOTE 1: ADJUST 10K POT. FOR 6mA I_D.

Fig. 5 — 105MHz to 10.7MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO. 18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 2T FROM COLD END.

L2 4T NO. 18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 3/8" LONG TAP AT 1T FROM COLD END.

T1 Q_O = 67 AT 10.7MHz, N1/N2 = 17.

MEM 619

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- Back to back zener diodes to protect gate
- Dual gate cascode operation
- Low 3rd. Order distortion
- High gain-low noise through medium frequency range
- Low feedback capacitance
- Excellent thermal stability
- Low output capacitance
- Specified for low V_D and low I_D operation

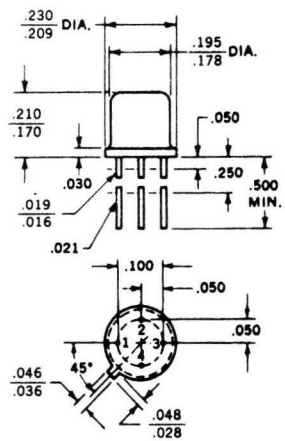
APPLICATIONS

Low power drain amplifier applications
Synchronous detectors
Wide band source followers
Linear and video amplifiers

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise specified)

Drain-source voltage V_{DS}	20V
Drain-gate No. 1 voltage, V_{DG1}	25V
Drain-gate No. 2 voltage, V_{DG2}	25V
Gate No. 1—source voltage, V_{G1S}	±6V
Gate No. 2—source voltage, V_{G2S}	±6V
Drain current, I_D	50mA
Transistor Dissipation, P_T at 25°C	360mW
Above 25°C, derate linearly	2.4mW/°C
Lead temperature distance 1/32 from the seated surface for 10 seconds	265°C
Storage temperature range	−65°C to +175°C

TO-72



Bottom view

Note: All dimensions in inches.

TERMINALS

1. DRAIN
2. GATE #2
3. GATE #1
4. SOURCE BASE

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Drain—Source Breakdown Voltage	BV_{DSS}	20	—	—	Volts	I_D=10μA, V_{G1S}=V_{G2S}=−0V
Gate 1—Source Breakdown Voltage	BV_{G1SS}	±6	—	—	Volts	I_{G1S}=10μA, V_{DS}=V_{G2S}=0V
Gate 2—Source Breakdown Voltage	BV_{G2SS}	±6	—	—	Volts	I_{G2S}=10μA, V_{DS}=V_{G1S}=0V
Gate 1—Source Cutoff Voltage	$V_{G1S(off)}$	−2.0	−1.5	—	Volts	I_D=50μA, V_{DS}=15V, V_{G2S}=4V
Gate 2—Source Cutoff Voltage	$V_{G2S(off)}$	—	—	0	Volts	I_D=50μA, V_{DS}=15V, V_{G1S}=0V
Zero Gate 1 Voltage Drain Current	I_{DSS}	1.5	—	20	mA	V_{DS}=5V, V_{G1S}=0V, V_{G2S}=4V
Gate 1—Leakage Current	I_{G1SS}	—	—	10	nA	V_{G1S}=±1V, V_{G2S}=V_{DS}=0V
Gate 2—Leakage Current	I_{G2SS}	—	—	50	nA	V_{G2S}=+4V, V_{G1S}=V_{DS}=0V
Transadmittance	Y_{fs}	4.0	—	—	μmho	V_{DS}=5V, I_D=2mA, V_{G2S}=+4V, f=1.0kHz
Small Signal, Short Circuit Reverse Transfer Capacitance	C_{rss}	—	.02	—	pF	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz
Small Signal, Short Circuit Gate 1—Source Input Capacitance	C_{iss}	5.0	—	7.0	pF	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=200MHz
Small Signal, Short Circuit Output Capacitance	C_{oss}	1.5	—	3.0	pF	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=200MHz

MEM 630 MEM 631
MEM 632

Dual Gate N-Channel Depletion Mode MOSFETS

FEATURES

- Low Cost Plastic Package
- Monolithic Gate Protection Diodes
- Low Feedback Capacitance
- Silicon Nitride Passivation for Long Term Stability

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

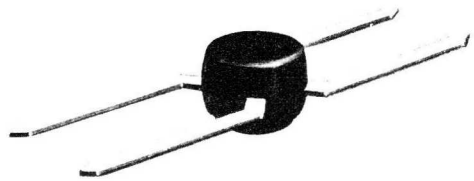
DESCRIPTION

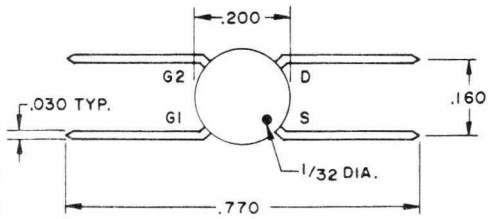
The MEM 630/ MEM 631/ MEM 632 are N-channel, Depletion Mode, Dual-Gate Metal Oxide Semiconductor transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

The MEM 630 is intended for use in high frequency RF amplifiers of FM radios. Typical Gps of 22 dB and noise figure of 2.5 dB at 105 MHz.

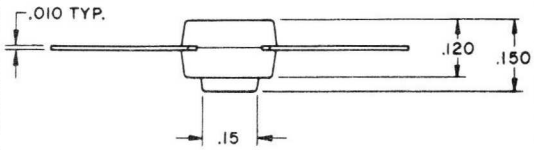
The MEM 631 is intended for use in VHF amplifiers and high frequency tuned amplifiers such as TV tuners and 44 MHz or 10.7 MHz IF amplifiers. Typical Gps of 19 dB and noise figure of 3.5 dB at 200 MHz. Typical Gps of 30 dB and noise figure of 2.5 dB at 44 MHz.

The MEM 632 is intended for use in HF and VHF mixers. The high conversion gain makes the MEM 632 ideal for TV or FM tuner mixer applications. 105 MHz to 10.7 MHz Conversion Gain of 20 dB. 200 MHz to 44 MHz Conversion Gain of 17 dB.





TOP VIEW

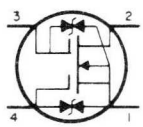


SIDE VIEW

LEADS CAN BE PREFORMED TO CUSTOMER SPECIFICATION.

LEAD CONFIGURATION

1. SOURCE
2. DRAIN
3. GATE 2
4. GATE 1



MAXIMUM RATINGS

Drain – Source Voltage	V_{DS}	25Vdc
Drain Current	I_D	30mAdc
Total Device Dissipation (Package Limitations)	P_D @ T_A = 25°C	500mW
Derate Above 25° C		5.0mW/°C
Operating and Storage Junction Temperature Range		–65 to +175°C

ELECTRICAL CHARACTERISTICS (T_A=25° C UNLESS OTHERWISE SPECIFIED)

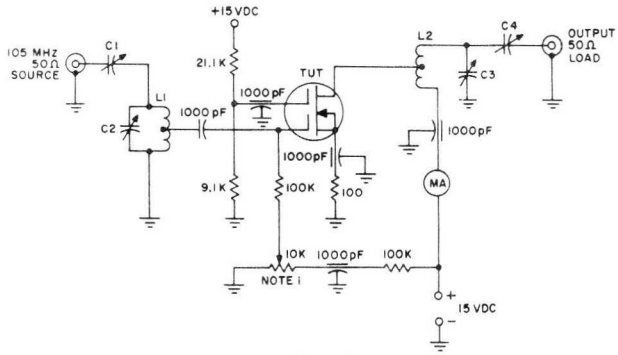
SYMBOLS	CHARACTERISTICS	TEST CONDITIONS		MEM630 Min	MEM630 Typ	MEM630 Max	MEM631 Min	MEM631 Typ	MEM631 Max	MEM632 Min	MEM632 Typ	MEM632 Max	UNITS
BV_{DSX}	Drain-Source Breakdown Voltage	I_D=10μA, V_S=0, V_{G1}=V_{G2}=–4.0V		20		–	20		–	20		–	volts
BV_{G1SO}	Gate 1-Source Breakdown Voltage	I_{G1}=±10μA, V_{G2S}=0		±6.0			±6.0			±6.0			volts
BV_{G2SO}	Gate 2-Source Breakdown Voltage	I_{G2}=±10μA, V_{G1S}=0		±6.0			±6.0			±6.0			volts
V_{G1S} (off)	Gate 1 to Source Cut off Voltage	V_{DS}=15V, V_{G2S}=4.0V, I_D=200μA		–		–4.0	–		–4.0	–		–4.0	volts
V_{G2S} (off)	Gate 2 to Source Cut off Voltage	V_{DS}=15V, V_{G1S}=4.0V, I_D=200μA		–		–2.0	–		–3.0	–		–2.0	volts
I_{G1SS}	Gate 1-Leakage Current	V_{G1S}=±4.0V V_{G2S}=0, V_{DS}=0		–		20	–		20	–		20	nAdc
I_{G2SS}	Gate 2-Leakage Current	V_{G2S}=±4.0V V_{G1S}=0 V_{DS}=0		–		20	–		20	–		20	nAdc
I_{DSS}	Zero-Gate Voltage Drain Current	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4.0V		2.0	Note 3	18	5.0	Note 3	30	2.0	Note 3	20	mAdc
Y_{fs1}	Fwd. Transadmittance (Gate 1 – Drain)	V_{DS}=15V, V_{G2S}=4.0V, I_D=10mA, f=1.0kHz		10		20	10		20	10		20	mmho
Ciss	Input Capacitance	V_{DS}=15V		–	–	7.0	–	–	6.0	–	–	7.0	pF
Coss	Output Capacitance	V_{G2S}=4.0V		–	–	3.0	–	–	3.0	–	–	3.0	pF
Crss	Reverse Transfer Capacitance	I_D=I_{DSS}, f=1.0MHz		–	.03	–	–	.03	–	–	–	–	pF
NF	Common Source Noise Figure (See Note #1)	V_{DS}=15V, V_{G2S}=4.0V,	f=105MHz	–	2.5	3.5	–	–	–	–	–	–	dB
		I_D=6.0mA,	f= 44MHz	–	–	–	–	2.5	3.0	–	–	–	dB
			f=200MHz	–	–	–	–	3.5	4.0	–	–	–	dB
Gps	Common Source Power Gain (See Note #2)	V_{DS}=15V, V_{G2S}=4.0V,	f=105MHz	17	22	–	–	–	–	–	–	–	dB
		I_D=6.0mA	f= 44MHz	–	–	–	–	30	–	–	–	–	dB
			f=200MHz	–	–	–	16	19	–	–	–	–	dB
Gc	Common Source Conversion Power Gain	V_{DD}=15V,		–	–	–	–	–	–	–	–	–	
		Signal Freq.=100MHz, Local Osc. f=110.7MHz		–	–	–	–	–	–	15	18	–	dB
		Signal Freq.=200MHz, Local Osc. f=244MHz		–	–	–	–	–	–	12	15	–	dB
riss	Input Resistance	V_{DS}=15V	f=105MHz	–	3.2	–	–	–	–	–	3.2	–	kΩ
		V_{G2S}=4.0V	f= 44MHz	–	–	–	–	15	–	–	–	–	kΩ
		I_D=6.0mA	f=200MHz	–	–	–	–	0.9	–	–	0.9	–	kΩ
ross	Output Resistance	V_{DS}=15V	f=105MHz	–	3.5	–	–	–	–	–	–	–	kΩ
		V_{G2S}=400V	f= 44MHz	–	–	–	–	18	–	–	17	–	kΩ
		I_D=6.0mA	f=200MHz	–	–	–	–	1.5	–	–	–	–	kΩ
			f=10.7MHz	–	–	–	–	–	–	–	30	–	kΩ
|Yfs|	Magnitude of Fwd Transadmittance	V_{DS}=15V I_D=6.0mA	f=105MHz	–	14	–	–	–	–	–	–	–	mmho
		V_{G2S}=4.0V	f=200MHz	–	–	–	–	16	–	–	–	–	mmho
|Yrs|	Magnitude of Rev Transadmittance	VDS=15V, I_D=6.0mA	f=105MHz	–	18	–	–	–	–	–	–	–	μmho
		V_{G2S}=4.0V	f=200MHz	–	–	–	–	36	–	–	–	–	μmho
θfs	Angle of Fwd Transadmittance	V_{DS}=15V, I_D=6.0mA	f=105MHz	–	–18	–	–	–	–	–	–	–	degree
		V_{G2S}=4.0V	f=200MHz	–	–	–	–	–35	–	–	–	–	degree
θrs	Angle of Rev Transadmittance	V_{DS}=15V, I_D=6.0mA	f=105MHz	–	90	–	–	–	–	–	–	–	degree
		V_{G2S}=4.0V	f=200MHz	–	–	–	–	–30	–	–	–	–	degree

NOTES:
1. Noise Figure: MEM630 See Fig. #1/MEM631 See Fig. #2 and #3
2. Power Gain: MEM630 See Fig. #1/MEM631 See Fig. #2 and #3

Device	I_{DSS} Range (mA)	Color Code	Suggested Source Resistor (ohms)	Suggested Biasing (volts)
MEM630	2-9	Black Dot	150	V_{G1} = +1.5
100 MHz R.F. Amplifier	7-18	Blue Dot	180	V_{G2S} = +4.0
MEM631	5-13	Black Dot	150*	V_{G1} = +1.5*
200 MHz R.F. Amplifier	11-22	Blue Dot	180*	V_{G2S} = +4.0*
	20-30	Red Dot	200*	
MEM632	2-9	Black Dot	100	V_{G1} = +0.5
Mixer	7-14	Blue Dot	100	V_{G2} = +1.5
	12-20	Red Dot	100	

*When the MEM631 is used as an I.F. amplifier, the suggested source resistor is 270 ohms with V_{G1} = +1.0 volts and V_{G2S}=+4.0 volts.

Fig. 1 — 105 MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 4-1/2T. C_t=17.8pF R_t=15K AT 100MHz, MOUNTED.

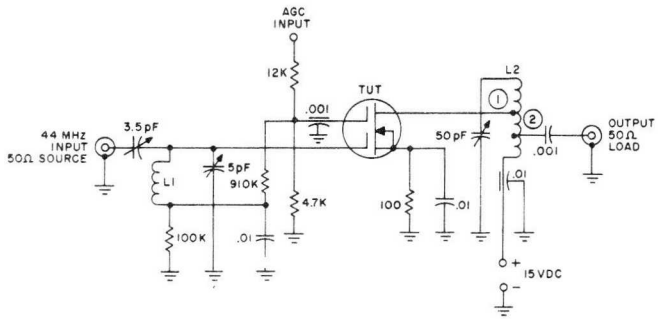
L2 SAME AS L1, BUT R_t=30K MOUNTED.

C1,C4 0.9 TO 7.0pF TRIMMER.

C2,C3 AIR VARIABLE CAPACITOR 20pF MAX.

NOTE 1: ADJUST 10K POT. FOR 6mA I_D.

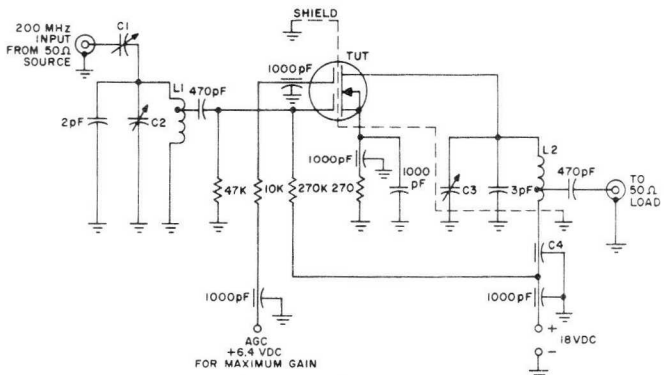
Fig. 2 — 44 MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 14T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM. FORM.

L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG.
(1) DRAIN TAP 2-1/2T FROM COLD END.
(2) LOAD TAP 0.4T FROM COLD END.

Fig. 3 — 200 MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END.

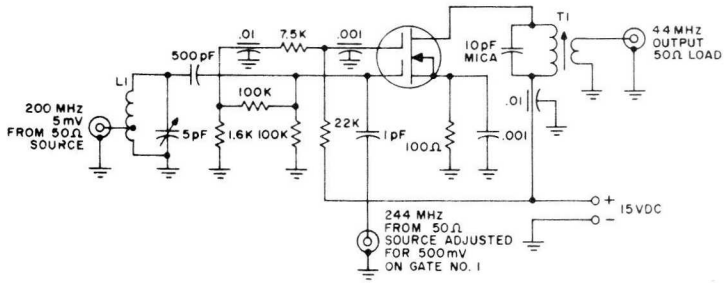
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.

C1 0.4 TO 7pF (ARCO 400).

C2,C3 1.3 TO 5pF VARIABLE.

C4 1000pF BUTTON TYPE CAPACITOR.

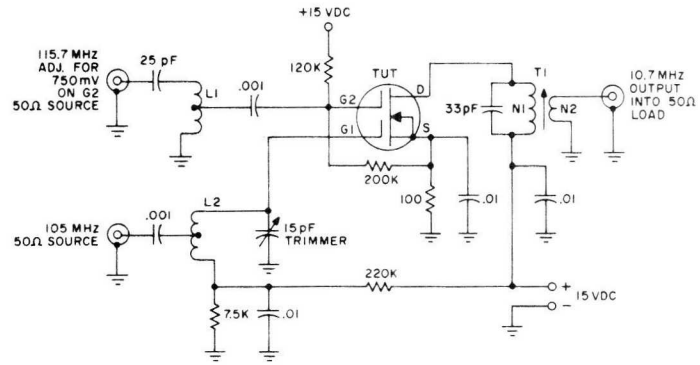
Fig. 4 — 200 MHz to 44 MHz MIXER TEST CIRCUIT



L1 3T NO. 16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG TAP AT 3/4T FROM COLD END.

T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM. SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO.

Fig. 5 — 105 MHz to 10.7 MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 2T FROM COLD END.

L2 4T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 3/8" LONG TAP AT 1T FROM COLD END.

T1 Q_0=67 AT 10.7MHz, N1/N2=17.

MEM 636 MEM 637
MEM 638

Dual-Gate N-Channel Depletion Mode MOSFETS

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain–Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers–Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

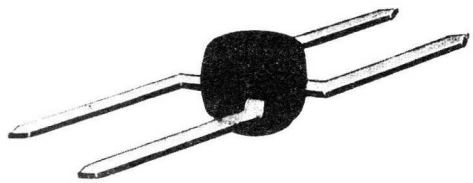
DESCRIPTION

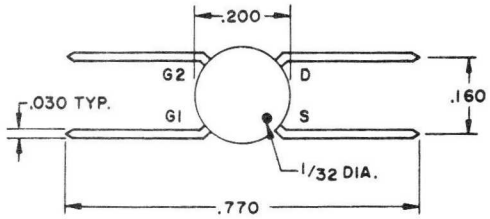
The MEM 636/MEM 637/MEM 638 are N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor field-effect transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

The MEM 636 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

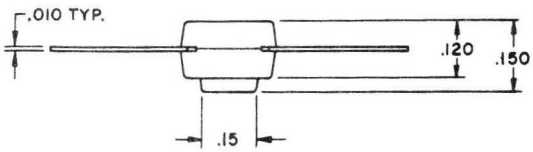
The MEM 637 is intended for use in VHF mixers where minimized cross-modulation, and inter-modulation distortion and low noise operation are required.

The MEM 638 is intended for use in tuned high frequency amplifiers such as TV IF. The low feedback capacitance permits high single stage gain and stability without neutralization.





TOP VIEW

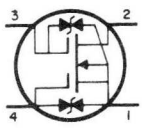


SIDE VIEW

LEADS CAN BE PREFORMED TO CUSTOMER SPECIFICATION.

TERMINAL DIAGRAM

1. SOURCE
2. DRAIN
3. GATE 2
4. GATE 1



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

DRAIN-SOURCE VOLTAGE, V_{DS} 25V
DRAIN-GATE NO. 1 VOLTAGE, V_{DG1} 25V
DRAIN-GATE NO. 2 VOLTAGE, V_{DG2} 25V
GATE NO. 1–SOURCE VOLTAGE, V_{G1S} ..... ±6V
GATE NO. 2–SOURCE VOLTAGE, V_{G2S} ..... ±6V
DRAIN CURRENT, I_D 50mA
TRANSISTOR DISSIPATION, P_T AT 25°C 350mW
ABOVE 25°C, DERATE LINEARLY ..... 2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS ..... 265°C
STORAGE TEMPERATURE RANGE ..... −65°C to +175°C

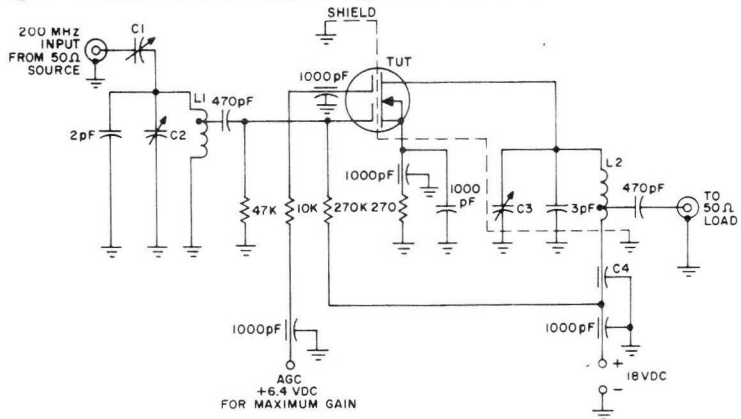
ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MEM 636 MIN	MEM 636 TYP	MEM 636 MAX	MEM 637 MIN	MEM 637 TYP	MEM 637 MAX	MEM 638 MIN	MEM 638 TYP	MEM 638 MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=100μA, V_{G1S}=V_{G2S}=−4V	20	–	–	20	–	–	20	–	–	V
BV_{G1SS}	Gate 1–Source Breakdown Voltage	I_{G1S}=10μA, V_{DS}=V_{G2S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
BV_{G2SS}	Gate 2–Source Breakdown Voltage	I_{G2S}=10μA, V_{DS}=V_{G1S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
$V_{G1S(off)}$	Gate 1–Source Cutoff Voltage	I_D=50μA, V_{DS}=15V, V_{G2S}=4V	–	−1.5	–	–	−1.0	–	–	−1.5	–	V
$V_{G2S(off)}$	Gate 2–Source Cutoff Voltage	I_D=50μA, V_{DS}=15V, V_{G1S}=0V	–	–	−4.0	–	–	−4.0	–	–	−4.0	V
I_{DSS}	Gate 2–Voltage Drain Current	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V	4.0[7]	–	30	2.0[7]	–	20	3.0[7]	–	20	mA
I_{G1SS}	Gate 1–Leakage Current	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
I_{G2SS}	Gate 2–Leakage Current	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz	.005	.02	.03	–	–	–	.005	.02	.03	pF
C_{iss}	Input Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	4.0	5.4	6.0	–	6.0	–	–	5.1	–	pF
C_{oss}	Output Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.2	–	–	2.5	–	–	2.5	–	pF
r_{iss}	Input Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	790	–	–	670	–	–	15k	–	Ω
r_{oss}	Output Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.00	–	–	17	–	–	18	–	kΩ
$\|Y_{fs}\|$	Magnitude of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	12	18	–	–	4.4[8]	–	10	14	–	mmho
θ	Angle of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, see	–	−55	–	–	–	–	–	−13.6	–	deg.
$\|Y_{rs}\|$	Magnitude of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, notes	–	30	–	–	–	–	–	5.5	–	μmho
θ_{rs}	Angle of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, 4,5,6	–	−30	–	–	–	–	–	90	–	deg.
G_c	Conversion Power Gain Fig. 2 200MHz, Fig. 5 105MHz	V_{DS}=+15V, V_{G2S}=+4V,	–	–	–	–	18	–	–	–	–	dB
Gps	Power Gain – 200MHz	Fig. 1	19	21	–	–	–	–	–	–	–	dB
Gps	Power Gain – 105MHz	Fig. 4	–	27	–	–	–	–	–	–	–	dB
MUG	Maximum Usable Power Gain – 44MHz	Fig. 3	–	–	–	–	–	–	–	30[3]	–	dB
N.F.	Noise Figure – 200MHz	Fig. 1	–	2.5	3.3	–	–	–	–	–	–	dB

NOTES:
1. See Figure 1.
2. Signal and local oscillator voltages, both are applied on Gate 1 with injection level equal to 500MV RMS (see Figure 2).
3. Unneutralized maximum usable gain for one stage (see Figure 3).
4. MEM 636 (RF AMP) I_D=10mA, f=200MHz.
5. MEM 637 (MIXER) V_{G1S}=0.1V, f=200MHz/44MHz.
6. MEM 638 (IF AMP) I_D=5mA, f=44MHz.
7. In addition to the standard range of I_{DSS}, the following I_{DSS} ranges are available:
8. Forward conversion transconductance.

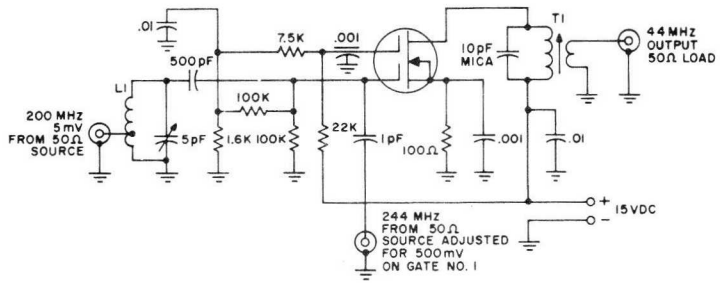
Device	I_{DSS} Range (mA)	Color Code	Suggested Source Resistor (Ω)	Suggested Biasing (V)
MEM 636	4-13	Yellow Dot	150	V_{G1} = +1.5
R.F. Amplifier	11-22	Blue Dot	180	V_{G2S}= +4.0
	20-30	Red Dot	200	
MEM 637	2-8	Yellow Dot	100	V_{G1} = +0.5
Mixer	6-12	Blue Dot	100	V_{G2} = +1.5
	10-20	Red Dot		
MEM 638	3-9	Yellow Dot	270	V_{G1} = +1.0
I.F. Amplifier	7-14	Blue Dot	270	V_{G2S}= +4.0
	12-20	Red Dot	270	

Fig. 1 — 200MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



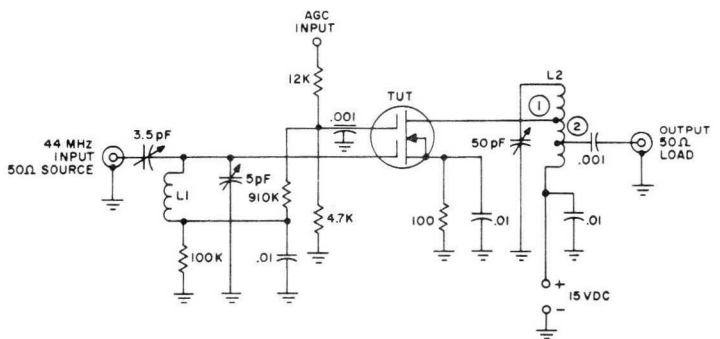
L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END.
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.
C1 0.4 TO 7pF (ARCO 400).
C2,C3 1.3 TO 5pF VARIABLE.
C4 1000pF BUTTON TYPE CAPACITOR.

FIG. 2 — 200MHz TO 44MHz MIXER TEST CIRCUIT



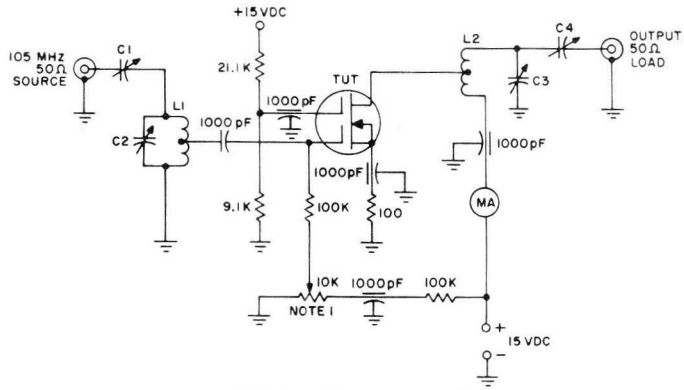
L1 3T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG, TAP AT 3/4T FROM COLD END.
T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM.
SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO.

Fig. 3 — 44MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 14T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM. FORM.
L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG.
(1) DRAIN TAP 2-1/2T FROM COLD END.
(2) LOAD TAP 0.4T FROM COLD END.

Fig. 4 — 105MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 4-1/2T. C_t = 17.8pF R_t = 15K AT 100MHz, MOUNTED.

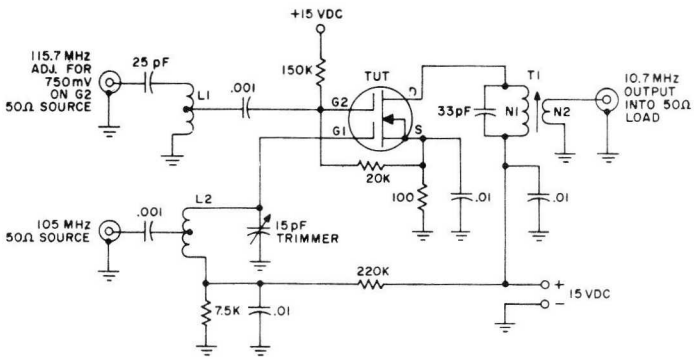
L2 SAME AS L1, BUT R_t = 30K MOUNTED.

C1,C4 0.9 TO 7.0pF TRIMMER.

C2,C3 AIR VARIABLE CAPACITOR 20pF MAX.

NOTE 1: ADJUST 10K POT. FOR 6mA I_D.

Fig. 5 — 105MHz TO 10.7MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 2T FROM COLD END.

L2 4T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 3/8" LONG TAP AT 1T FROM COLD END.

T1 Q_O = 67 AT 10.7MHz, N1/N2 = 17.

MEM 639

Dual-Gate N-Channel Depletion Mode MOSFET

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain—Low Noise at HF
- Reverse AGC Capability
- Linear Mixers—Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

- CB Radio RF Amplifiers and Mixers
- CB Radio PLL Mixers
- IF Amplifiers

DESCRIPTION

The MEM 639 is an N-channel, Depletion-Mode Dual-Gate, Metal-Oxide semiconductor Field Effect Transistor. It is protected from excessive input voltages by integrated monolithic back-to-back diodes between the gates and source.

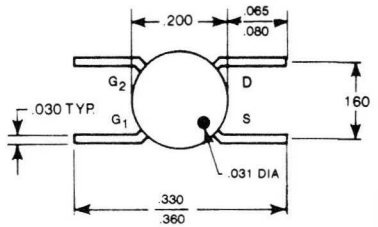
The MEM 639 is specially designed for use in CB radios as an RF amplifier or mixer where large signal handling capability, minimum cross-modulation and intermodulation distortion and low noise operation are required.

The MEM 639 is also recommended for use as a PLL mixer where large amplitude from a reference oscillator and VCO can be applied separately to the gates while exhibiting good isolation.

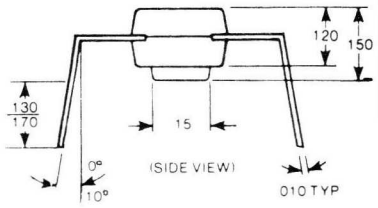
MAXIMUM RATINGS

DRAIN-SOURCE VOLTAGE	25V
DRAIN-GATE NO. 1 VOLTAGE	25V
DRAIN-GATE NO. 2 VOLTAGE	25V
DRAIN CURRENT,	50mA
TRANSISTOR DISSIPATION, P_T AT 25°C	360mW
ABOVE 25°C, DERATE LINEARLY	2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32	
FROM THE SEATED SURFACE FOR 10 SECONDS	265°C
STORAGE TEMPERATURE RANGE	−65°C to +175°C

Actual Size

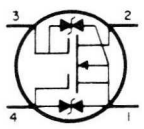


(TOP VIEW)



LEAD CONFIGURATION

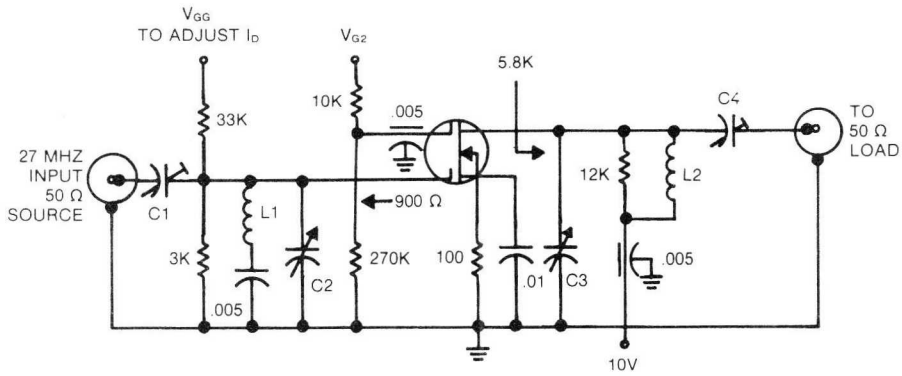
1. SOURCE
2. DRAIN
3. GATE 2
4. GATE 1



ELECTRICAL CHARACTERISTICS

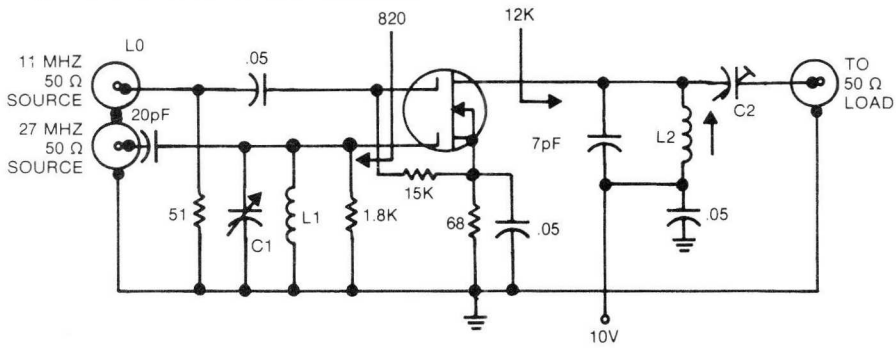
SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 100\mu A$, $V_{G1S} = V_{G2S} = -4V$	20	—	+15	V
BV_{G1SS}	Gate 1—Source Breakdown Voltage	$I_{G1S} = 10\mu A$, $V_{DS} = V_{G2S} = 0V$	+6	—	+15	V
BV_{G2SS}	Gate 2—Source Breakdown Voltage	$I_{G2S} = 10\mu A$, $V_{DS} = V_{G1S} = 0V$	+6	—	+6	V
$V_{G1S(off)}$	Gate 1—Source Cutoff Voltage	$I_D = 200\mu A$, $V_{DS} = 15V$, $V_{G2S} = 4V$	—	−1.5	−6	V
$V_{G2S(off)}$	Gate 2—Source Cutoff Voltage	$I_D = 200\mu A$, $V_{DS} = 15V$, $V_{G1S} = 0V$	—	−1.5	30	V
I_{DSS}	Gate 2—Voltage Drain Current	$V_{DS} = 15V$, $V_{G1S} = 0V$, $V_{G2S} = 4V$	1.0	10	—	mA
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, $f = 1.0MHz$	—	.03	7.0	pF
C_{iss}	Input Capacitance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, $f = 1.0MHz$	—	5.0	—	pF
C_{oss}	Output Capacitance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, $f = 1.0MHz$	—	2.5	—	pF
Y_{fs}	Magnitude of Fwd Transadmittance	$V_{DS} = +15V$, $V_{G2S} = +4V$, $I_D = 10mA$, $f = 1.0kHz$	—	17	—	mmho
G_{ps}	Power Gain	See Figure 1, $I_D = 6mA$, $V_{G2} = 5V$	—	25	—	dB
N.F	Noise Figure	See Figure 2, Injection voltage = 1V	—	4.5	—	dB
G_c	Conversion Power Gain	Injection voltage = 100mV	—	17	—	dB
			—	3		dB

Fig. 1—27 MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L_1 18 TURNS NO 24 ENAMEL WIRE ON 7/32" DIAM. CORE.
L_2 25 TURNS NO 24 ENAMEL WIRE ON 7/32" DIAM. CORE.
C_1, C_4 1.5 TO 2.0pF TRIMMER.
C_2, C_3 AIR VARIABLE CAPACITOR 20pF MAX.

Fig. 2—27 MHz TO 16 MHz CONVERSION GAIN TEST CIRCUIT



L_1 25 TURNS NO 24 ENAMEL WIRE ON 7/32" DIAM. CORE.
L_2 10.7 MHZ IF TRANSFORMER, R_t = 30K AT 16 MHZ.
C_1 AIR VARIABLE CAPACITOR 20 pF MAX.
C_2 1.5 TO 20pF TRIMMER.

MEM 655

N-Channel Depletion Mode MOSFET

FEATURES

- Back-to-Back Zener Clamp to protect gate
- Low 3rd order distortion
- High gain—low noise through VHF range
- Low feedback capacitance 0.32 pF typ.
- Square law response

APPLICATIONS

- TV Tuners
- FM Tuners
- IF Amplifiers
- SSB Amplifiers
- Wideband Amplifiers
- High Frequency Analog Switching

MAXIMUM RATINGS

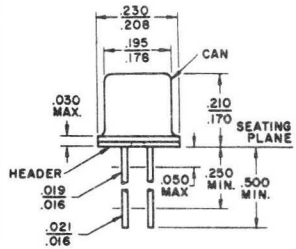
Drain-to-Source voltage ..... +20V
Gate-to-Source voltage ..... ±6.0V
Drain-to-Gate voltage ..... +30 to −6.0V
Drain Current ..... Limited by Dissipation
Storage Temperature ..... −65 to +150°C
Operating Junction Temperature ..... −65 to +150°C
Total Dissipation at 25°C Case Temperature 300mW
Total Dissipation at 25°C Ambient Temperature 225mW
at 100°C Ambient Temperature 150mW
Derate Linearly from 100°C to 150°C at 3 mW/°C

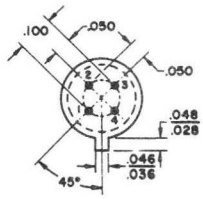
ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
BV_{DSX}	Breakdown voltage drain to source	$V_{GS} = -4.0V$ $I_D = 100\mu A$	20	—	—	V
BV_{gss}	Breakdown voltage gate to source	$V_{DS} = OV$, $1_g = 100\mu A$	±6.0	—	—	V
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 4.0V$	—	—	±100	nA
$I_{D(off)}$	Drain to Source Leakage Current	$V_{DS} = +15V$, $V_{GS} = -4.0V$	—	—	100	μA
I_{DSS}	Zero signal Gate voltage drain current	$V_{DS} = +15V$, $V_{GS} = OV$	1.0	4.0	20.0	mA
$V_{G(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = +15V$, $I_D = 100\mu A$	—	−1.0	−4.0	V
C_{iss}	Small-signal, short circuit input capacitance	$V_{DS} = +15V$, $I_D = 10mA$*, f = 44 MHz	—	4.0	7.0	pF
C_{oss}	Small-signal, short circuit output capacitance	$V_{DS} = +15V$, $I_D = 5mA$*, f = 44 MHz	—	2.0	—	pF
C_{rss}	Small-signal, short circuit reverse transfer capacitance	$V_{DS} = +15V$, $I_D = 5mA$*, f = 1.0 MHz	—	0.32	—	pF
G_{fs}	Forward transconductance	$V_{DS} = +15V$, $I_D = 5mA$*, f = 1.0 kHz	6000	10000	—	μmhos
G_{ps}	Power gain (See Fig. 1 for measurement circuit)	$V_{DD} = +18V$, f = 100 MHz, $R_s = 270\Omega$	18	22	—	dB
NF	Noise Figure ** (See Fig. 1 for measurement circuit)	$V_{DD} = +18V$, f = 100 MHz, $R_s = 270\Omega$	—	2.5	4.5	dB
$rd_{s(on)}$	Drain to Source on resistance	$V_{GS} = +6.0$, I_D 0.1mA	—	30	100	Ω

*V_{GS} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72





Bottom View

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Source
3. Gate
4. Substrate and case

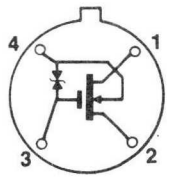
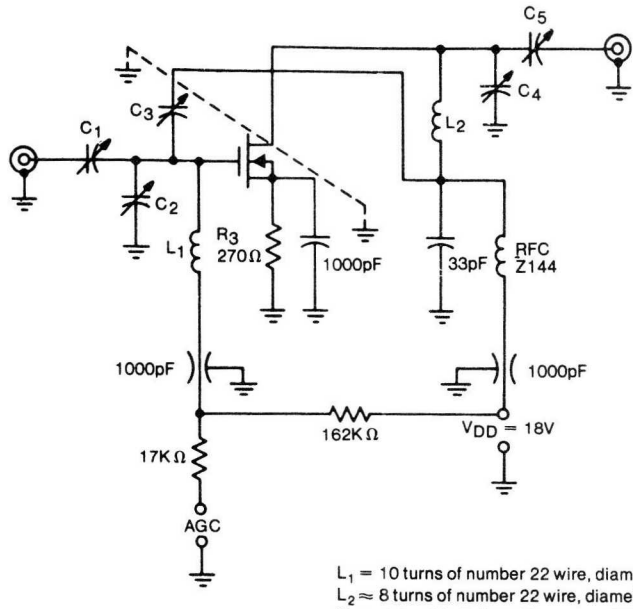


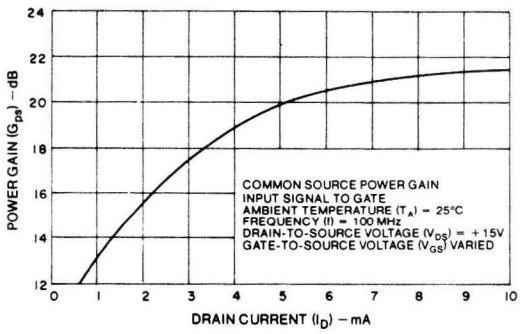
Fig. 1 — POWER GAIN TEST JIG @ 100MHz WITH NEUTRALIZING



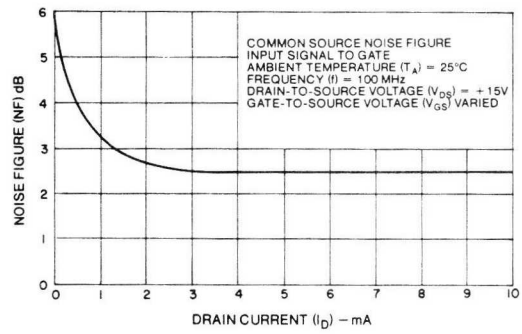
L_1 = 10 turns of number 22 wire, diameter of coil = .125 inch
L_2 ≈ 8 turns of number 22 wire, diameter of coil = .25 inch
C_1 ≈ 1.5 – 20 pF (Arco Elmenco # 400)
C_2 & C_3 = .9 to 7 pF (Arco Elmenco # 402)
C_4 & C_5 = .9 to 7 pF (Arco Elmenco # 402)

TYPICAL CHARACTERISTIC CURVES

POWER GAIN vs. DRAIN CURRENT



NOISE FIGURE vs. DRAIN CURRENT



MEM 660

N-Channel Depletion Mode MOSFET

FEATURES

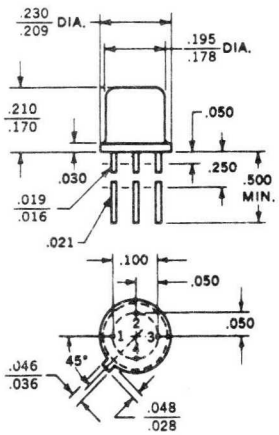
- Matched Low $r_{ds\ (on)}$
- Nanosecond switching times
- Low Cgd—.30pF typical
- High $I_{D\ (on)}$—60mA typical
- Low drive voltages—±6 volt
- Zener clamp (protection)

APPLICATIONS

- High speed multiplexers
- Memory Read/Write Gates
- Memory Read Gates

Actual Size

TO-72



Bottom View

Note: All dimensions in inches.

MAXIMUM RATINGS

Drain-to-source voltage	+20V
Gate-to-source voltage	+30V to −20V
Substrate-to-all terminals	−20 to +1.0V
Drain-to-gate voltage	+30 to −20V
Drain current	Limited by Dissipation
Storage temperature	−65 to +150°C
Operating junction temperature	−65 to +150°C
Total Dissipation at 25°C Case Temperature	300mW
Total Dissipation at 25°C Ambient Temperature	150mW
Derate linearly from 70°C to 150°C at 1.87	150mW

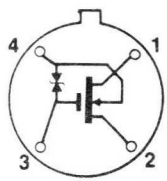
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
BV_{DSX}	Breakdown voltage drain-to-source	$V_{GS} = V_{BS} = -6V$, $I_D = 10\mu A$	12	—	—	—
I_{DSX}	Drain-to-source leakage current	$V_{DS} = +6V$, $V_{GS} = -6V$ $V_{BS} = 0V$	—	—	12.5	nA
I_{SDX}	Source-to-drain leakage current	$V_{SD} = +6V$, $V_{GD} = -6V$ $V_{BD} = 0V$	—	—	12.5	nA
$I_{D\ (on)}$	Drain-to-source current	$V_{GS} = +6V$, $V_{DS} = +3V$ $V_{BS} = -6V$	30	60	—	mA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = +12V$, $V_{BS} = -6V$ $V_{GS} = 0V$	—	—	10	mA
BVGB	Breakdown voltage gate-to-substrate	$I_{GB} = \pm 10\mu A$	+20 −6	— —	— —	V
I_{GS}	Leakage current gate-to-source	$V_{GS} = \pm 10V$, $V_{DS} = 0$	—	—	±10	nA
$r_{ds\ (on)}$	Drain-to-source on resistance	$V_{GS} = +6V$, $V_{BS} = -6V$ $I_D = 1.0mA$	10	—	30	Ω
C_{ISS}	Input capacitance	$V_{DS} = +12V$	—	4.5	7.0	pF
C_{RSS}	Feedback capacitance	$I_D = 10mA$	—	.30	1.0	pF
C_{OSS}	Output capacitance	f = 44MHz	—	2.0	5.0	pF

TERMINAL DIAGRAM

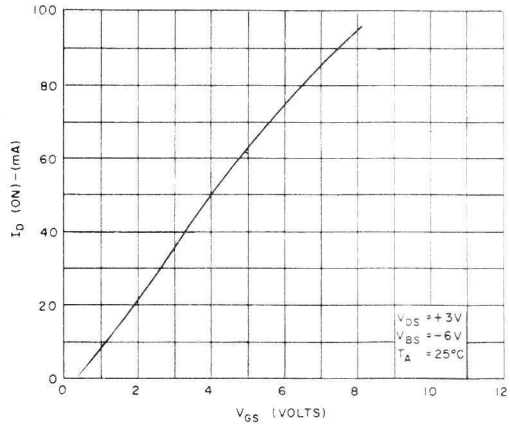
Lead

1. Drain
2. Source
3. Gate
4. Substrate and case

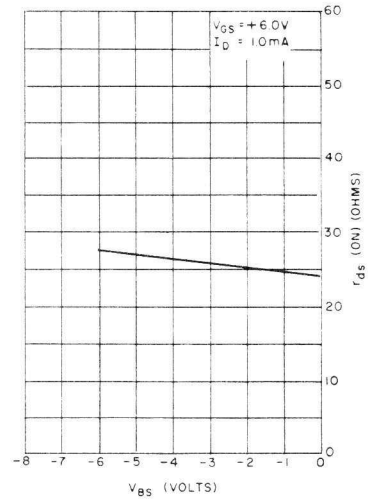


TYPICAL CHARACTERISTIC CURVES
MEM 660

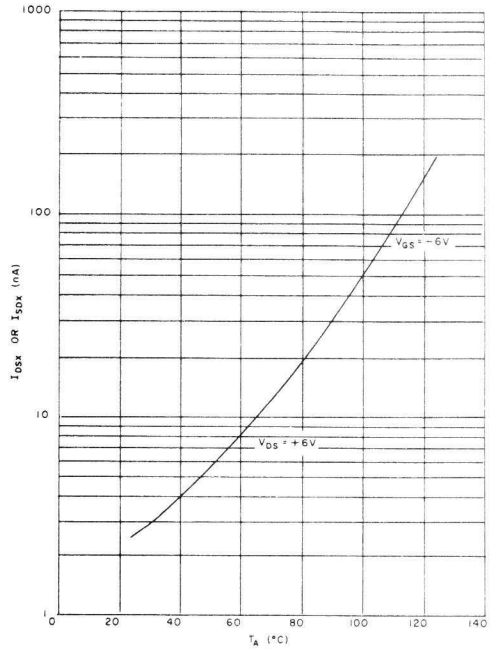
TYPICAL CURVES OF I_D vs. V_{GS}



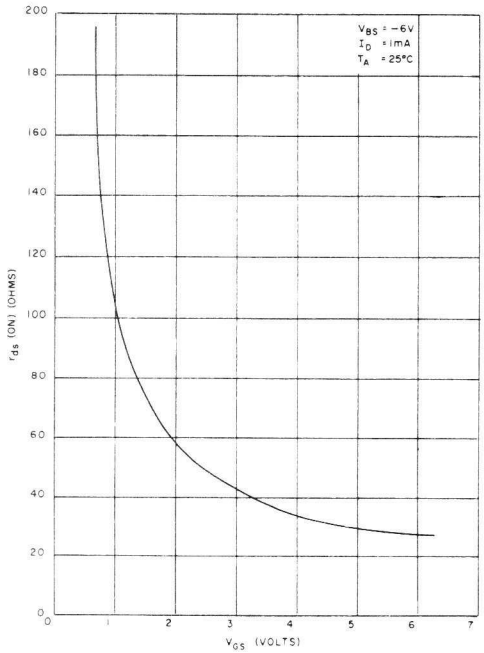
$r_{ds\ (on)}$ vs. SUBSTRATE VOLTAGE



TYPICAL I_{DSX} or I_{SDX} vs. TEMPERATURE



TYPICAL CURVES OF $r_{ds\ (on)}$ vs. V_{GS}



MEM 667

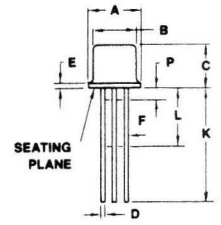
N-Channel Depletion Mode MOSFET

FEATURES

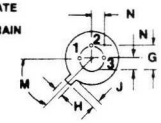
Femtoamp Gate Leakage
10^{15} Ohms Input Resistance
High Transient Gate Voltage Capability
Narrow I_{DSS} Range
Low Input Capacitance
Excellent Stability

APPLICATIONS

Smoke Detectors
Memory Modules
Electrometers
Alarm Systems



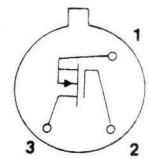
PIN 1 SOURCE SUBSTRATE CASE
2 GATE
3 DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E		0.762	—	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	—	1.27	—	0.050

LEAD CONFIGURATION

1 — SOURCE, SUBSTRATE AND CASE
2 — GATE
3 — DRAIN



DESCRIPTION

The MEM 667 is an N-channel, Depletion Mode, Metal Oxide Semiconductor Field Effect Transistor. This MOSFET exhibits very low gate leakage, extremely high input resistance, and is capable of handling very high gate to source voltage transients.

These features, combined with an excellent stability, make the MEM 667 ideally suited for smoke detector applications.

MAXIMUM RATINGS (T_A=25° C)

DRAIN-SOURCE VOLTAGE, V_{DS} 20V
DRAIN-GATE VOLTAGE, V_{GD} 20V
GATE-SOURCE VOLTAGE, V_{GS} .....± 100V
DRAIN CURRENT, I_D .....Limited by Dissipation
STORAGE TEMPERATURE RANGE .....−65°C to + 150°C
OPERATING TEMPERATURE RANGE .....−65°C to +125°C
POWER DISSIPATION (T_C=25°C) .....300 mW
POWER DISSIPATION (T_A=25°C) .....150 mW

ELECTRICAL CHARACTERISTICS

(T_A=25° C UNLESS OTHERWISE SPECIFIED)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)SDX}$	DRAIN-SOURCE BREAKDOWN	V_{GS}=−4V, I_D=10μA, V_{US}=0	20	45	—	volts
$V_{GS(off)}$	GATE-SOURCE CUTOFF VOLTAGE	V_{DS}=+15V, I_D=10μA	−0.3	−2.5	−4.0	volts
$I_{D(off)}$	DRAIN CUTOFF CURRENT	V_{DS}=+15V, V_{GS}=−4V, V_{US}=0	—	0.5	10	nA
I_{GSS}	GATE LEAKAGE CURRENT	V_{GS}=±10V, V_{DS}=V_{US}=0	—	.01	1.0	pA
Y_{fs}	FORWARD TRANSFer admittance	V_{DS}=+15V, I_D=2mA, V_{US}=0	—	2000	—	μmho
C_{iss}*	INPUT CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	—	2.0	5.0	pF
C_{oss}*	OUTPUT CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	—	2.0	5.0	pF
C_{rss}*	REVERSE TRANSFER CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	—	0.3	—	pF
I_{DSS}	ZERO GATE VOLTAGE DRAIN CURRENT	V_{DS}=+15V, V_{GS}=V_{US}=0	0.5		5.0	mA

NOTES: *V_{GS} ADJUSTED FOR I_D=10mA

MEM 670

N-Channel Depletion Mode MOSFET

FEATURES

- Femtoamp Gate Leakage
- 10^{15} Ohms Input Resistance
- High Transient Gate Voltage Capability
- Narrow I_{DSS} Range
- Low Input Capacitance
- Excellent Stability

APPLICATIONS

Smoke Detectors
Memory Modules
Electrometers
Alarm Systems

DESCRIPTION

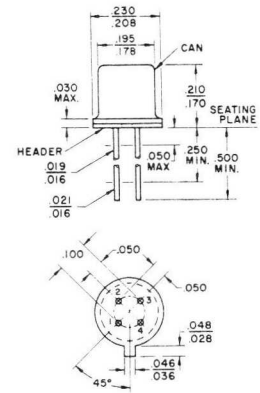
The MEM 670 is an N-channel, Depletion Mode, Metal Oxide Semiconductor Field Effect Transistor. This MOSFET exhibits very low gate leakage, extremely high input resistance, and is capable of handling very high gate to source voltage transients.

These features, combined with an excellent stability, make the MEM 670 ideally suited for smoke detector applications.

MAXIMUM RATINGS (T_A=25°C)

DRAIN-SOURCE VOLTAGE, V_{DS} 20V
DRAIN-GATE VOLTAGE, V_{GD} 20V
GATE-SOURCE VOLTAGE, V_{GS} ..... ±100V
DRAIN CURRENT, I_D ..... Limited by Dissipation
STORAGE TEMPERATURE RANGE ..... −65°C to +150°C
OPERATING TEMPERATURE RANGE ..... −65°C to +125°C
POWER DISSIPATION (T_C=25°C) ..... 300 mW
POWER DISSIPATION (T_A=25°C) ..... 150 mW

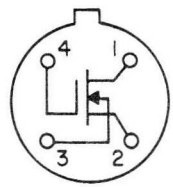
TO-72



BOTTOM VIEW
Note: All dimensions in inches.

LEAD CONFIGURATION

1 – DRAIN
2 – SOURCE
3 – SUBSTRATE AND CASE
4 – GATE



ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)SDX}$	DRAIN-SOURCE BREAKDOWN	V_{GS}=−4V, I_D=10μA, V_{US}=0	20	45	–	volts
$V_{GS(off)}$	GATE-SOURCE CUTOFF VOLTAGE	V_{DS}=+15V, I_D=10μA	−0.3	−2.5	−4.0	volts
$I_{D(off)}$	DRAIN CUTOFF CURRENT	V_{DS}=+15V, V_{GS}=−4V, V_{US}=0	–	0.5	10	nA
I_{GSS}	GATE LEAKAGE CURRENT	V_{GS}=±10V, V_{DS}=V_{US}=0	–	.01	1.0	pA
$\|Y_{fs}\|$	FORWARD TRANSFER ADMITTANCE	V_{DS}=+15V, I_D=2mA, V_{US}=0	–	2000	–	μmho
C_{iss}*	INPUT CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	–	2.0	5.0	pF
C_{oss}*	OUTPUT CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	–	2.0	5.0	pF
C_{rss}*	REVERSE TRANSFER CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	–	0.3	–	pF
I_{DSS}	ZERO GATE VOLTAGE DRAIN CURRENT	V_{DS}=+15V, V_{GS}=V_{US}=0				
		COLOR CODE – NONE	0.5	–	2.2	mA
		COLOR CODE – BLACK DOT	1.8	–	5.0	mA

NOTES: * V_{GS} ADJUSTED FOR I_D = 10mA

INDUSTRIAL/ MOSFET

MEM 680 MEM 681
MEM 682

Dual-Gate N-Channel Depletion Mode MOSFETS

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain–Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers–Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

DESCRIPTION

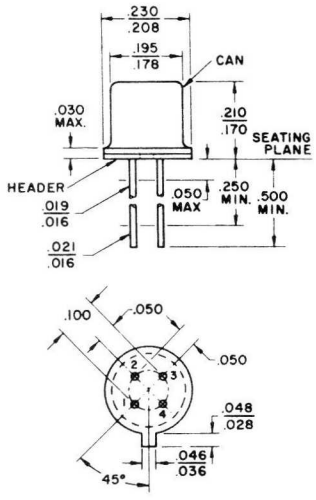
The MEM 680/MEM 681/MEM 682 are N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor field-effect transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

The MEM 680 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

The MEM 681 is intended for use in VHF mixers where minimized cross-modulation, and inter-modulation distortion and low noise operation are required.

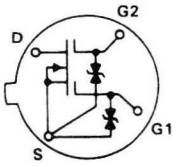
The MEM 682 is intended for use in tuned high frequency amplifiers such as TV IF. The low feedback capacitance permits high single stage gain and stability without neutralization.

TO-72



TERMINAL DIAGRAM

1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE/SUBSTRATE



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

@T_A=25°C UNLESS OTHERWISE SPECIFIED

DRAIN-SOURCE VOLTAGE, V_{DS}	25V
DRAIN-GATE NO. 1 VOLTAGE, V_{DG1}	25V
DRAIN-GATE NO. 2 VOLTAGE, V_{DG2}	25V
GATE NO. 1–SOURCE VOLTAGE, V_{G1S}	±6V
GATE NO. 2–SOURCE VOLTAGE, V_{G2S}	±6V
DRAIN CURRENT, I_D	50mA
TRANSISTOR DISSIPATION, P_T AT 25°C	360mW
ABOVE 25°C, DERATE LINEARLY	2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS	265°C
STORAGE TEMPERATURE RANGE	−65°C to +175°C

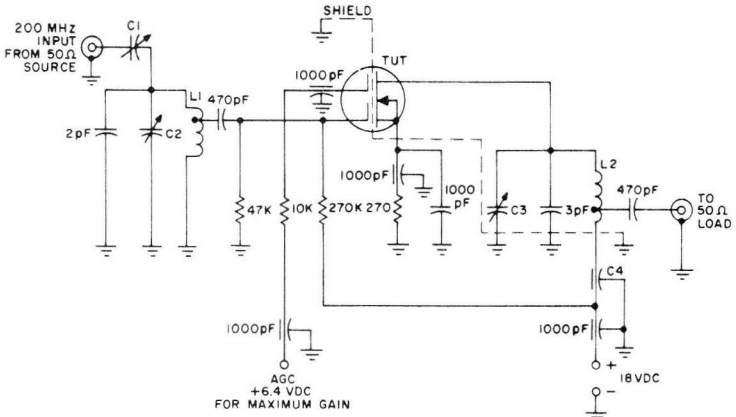
ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MEM 680 MIN	MEM 680 TYP	MEM 680 MAX	MEM 681 MIN	MEM 681 TYP	MEM 681 MAX	MEM 682 MIN	MEM 682 TYP	MEM 682 MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=100μA, V_{G1S}=V_{G2S}=−4V	20	–	–	20	–	–	20	–	–	V
BV_{G1SS}	Gate 1–Source Breakdown Voltage	I_{G1S}=10μA, V_{DS}=V_{G2S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
BV_{G2SS}	Gate 2–Source Breakdown Voltage	I_{G2S}=10μA, V_{DS}=V_{G1S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
$V_{G1S(off)}$	Gate 1–Source Cutoff Voltage	I_D=50μA, V_{DS}=15V, V_{G2S}=4V	–	−1.5	–	–	−1.0	–	–	−1.5	–	V
$V_{G2S(off)}$	Gate 2–Source Cutoff Voltage	I_D=50μA, V_{DS}=15V, V_{G1S}=0V	–	–	−4.0	–	–	−4.0	–	–	−4.0	V
I_{DSS}	Gate 2–Voltage Drain Current	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V	4.0[7]	–	30	2.0[7]	–	20	3.0[7]	–	20	mA
I_{G1SS}	Gate 1–Leakage Current	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
I_{G2SS}	Gate 2–Leakage Current	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz	.005	.02	.03	–	–	–	.005	.02	.03	pF
C_{iss}	Input Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	4.0	5.4	6.0	–	6.0	–	–	5.1	–	pF
C_{oss}	Output Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.2	–	–	2.5	–	–	2.5	–	pF
r_{iss}	Input Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	790	–	–	670	–	–	15k	–	Ω
r_{oss}	Output Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.00	–	–	17	–	–	18	–	kΩ
$\|Y_{fs}\|$	Magnitude of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	12	18	–	–	4.4[8]	–	10	14	–	mmho
θ	Angle of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, see	–	−55	–	–	–	–	–	−13.6	–	deg.
$\|Y_{rs}\|$	Magnitude of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, notes	–	30	–	–	–	–	–	5.5	–	μmho
θrs	Angle of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, 4,5,6	–	−30	–	–	–	–	–	90	–	deg.
G_C	Conversion Power Gain Fig. 2 200MHz, Fig. 5 105MHz	V_{DS}=+15V, V_{G2S}=+4V,	–	–	–	–	18	–	–	–	–	dB
Gps	Power Gain – 200MHz	Fig. 1	19	21	–	–	–	–	–	–	–	dB
Gps	Power Gain – 105MHz	Fig. 4	–	27	–	–	–	–	–	–	–	dB
MUG	Maximum Usable Power Gain – 44MHz	Fig. 3	–	–	–	–	–	–	–	30[3]	–	dB
N.F.	Noise Figure – 200MHz	Fig. 1	–	2.5	3.3	–	–	–	–	–	–	dB

NOTES:
1. See Figure 1.
2. Signal and local oscillator voltages, both are applied on Gate 1 with injection level equal to 500MV RMS (see Figure 2).
3. Unneutralized maximum usable gain for one stage (see Figure 3).
4. MEM 680 (RF AMP) I_D=10mA, f=200MHz.
5. MEM 681 (MIXER) V_{G1S}=0.1V, f=200MHz/44MHz.
6. MEM 682 (IF AMP) I_D=5mA, f=44MHz.
7. In addition to the standard range of I_{DSS}, the following I_{DSS} ranges are available:
8. Forward conversion transconductance.

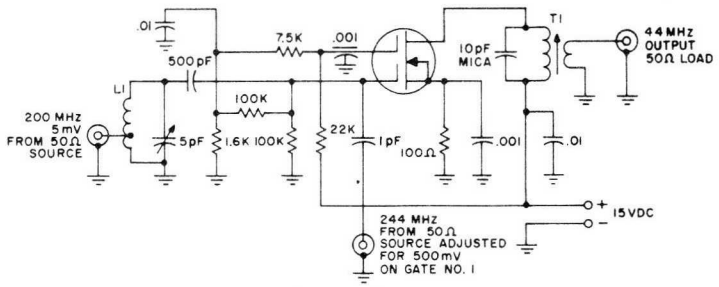
Device	I_{DSS} Range (mA)	Color Code	Suggested Source Resistor (Ω)	Suggested Biasing (V)
MEM 680	4-13	Yellow Dot	150	V_{G1} = +1.5
R.F. Amplifier	11-22	Blue Dot	180	V_{G2S}= +4.0
	20-30	Red Dot	200	
MEM 681	2-8	Yellow Dot	100	V_{G1} = +0.5
Mixer	6-12	Blue Dot	100	V_{G2} = +1.5
	10-20	Red Dot		
MEM 682	3-9	Yellow Dot	270	V_{G1} = +1.0
I.F. Amplifier	7-14	Blue Dot	270	V_{G2S}= +4.0
	12-20	Red Dot	270	

Fig. 1 — 200MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



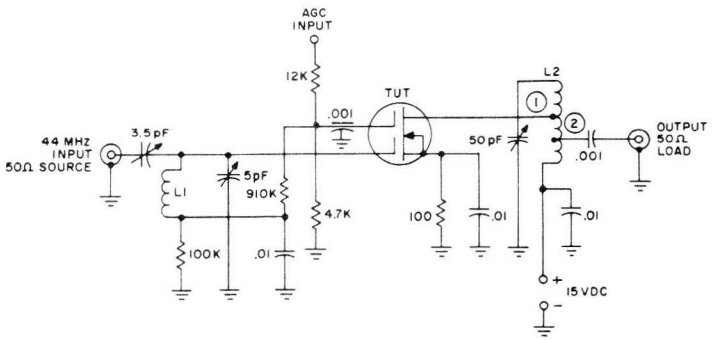
L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END.
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.
C1 0.4 TO 7pF (ARCO 400).
C2,C3 1.3 TO 5pF VARIABLE.
C4 1000pF BUTTON TYPE CAPACITOR.

Fig. 2 — 200MHz TO 44MHz MIXER TEST CIRCUIT



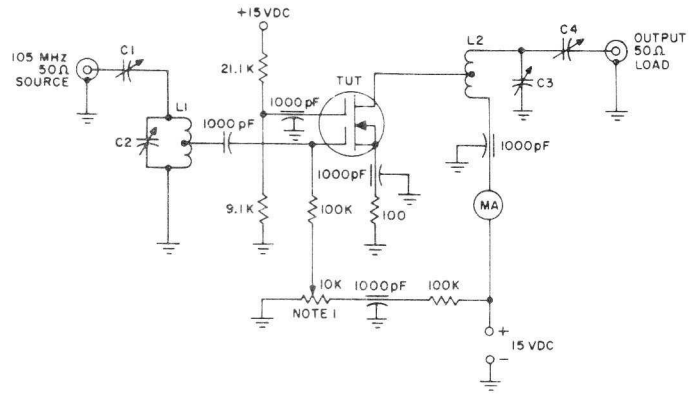
L1 3T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG TAP AT 3/4T FROM COLD END.
T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM.
SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO.

Fig. 3 — 44MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 14T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM. FORM.
L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG.
(1) DRAIN TAP 2-1/2T FROM COLD END.
(2) LOAD TAP 0.4T FROM COLD END.

Fig. 4 — 105MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 4-1/2T. C_t =17.8pF R_t =15K AT 100MHz, MOUNTED.

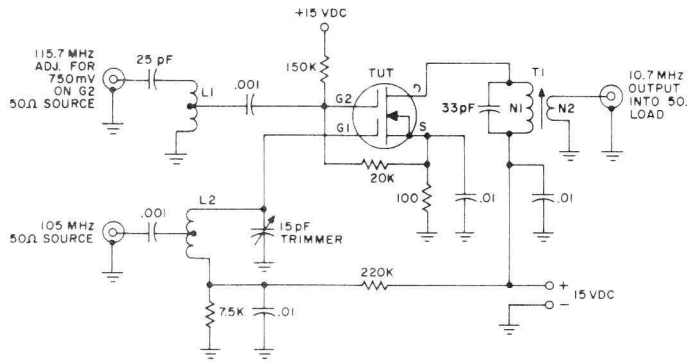
L2 SAME AS L1, BUT R_t = 30K MOUNTED.

C1,C4 0.9 TO 7.0pF TRIMMER.

C2,C3 AIR VARIABLE CAPACITOR 20pF MAX.

NOTE 1: ADJUST 10K POT. FOR 6mA I_D.

Fig. 5 — 105MHz TO 10.7MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 2T FROM COLD END.

L2 4T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 3/8" LONG TAP AT 1T FROM COLD END.

T1 Q_O = 67 AT 10.7MHz, N1/N2 = 17.

MEM 683

Dual Gate N-Channel Depletion Mode MOSFET

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain—Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers—Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

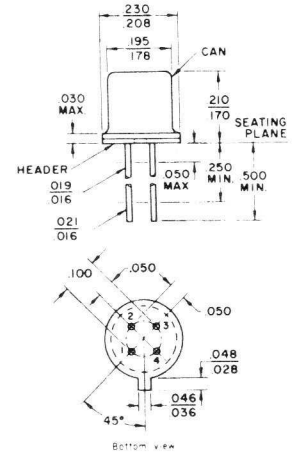
TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

DESCRIPTION

The MEM 683 is an N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor field-effect transistor. It is protected from excessive input voltage by monolithic back-to-back diodes between gates and source.

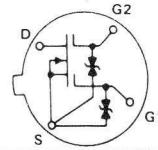
The MEM 683 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

TO-72



LEAD CONFIGURATION

1–DRAIN
2–GATE #2
3–GATE #1
4–SOURCE/SUBSTRATE

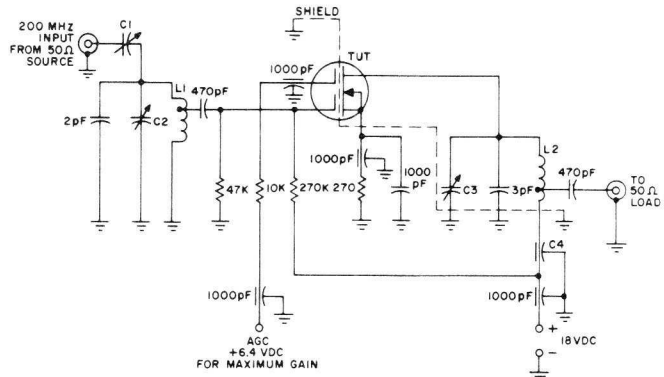


MAXIMUM RATINGS (@T_A=25°C unless otherwise specified)

Drain-source voltage, V_{DS} 25V
Drain-gate No. 1 voltage, V_{DG1} 25V
Drain-gate No. 2 voltage, V_{DG2} 25V
Drain current, I_D 50mA
Transistor dissipation, P_T at 25°C 360mW
Above 25°C, derate linearly ..... 2.4mW/°C
Lead temperature distance 1/32 from the seat surface for 10 seconds ..... 265°C
Storage temperature range ..... −65°C to +175°C

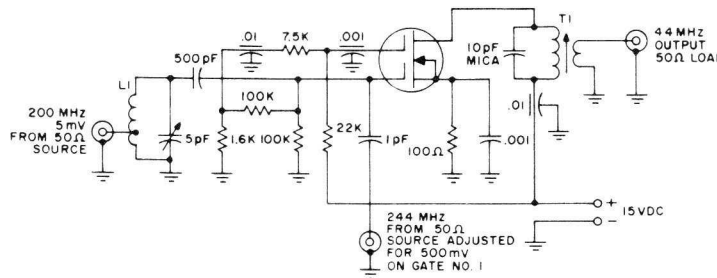
ELECTRICAL CHARACTERISTICS (@T_A=25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	I_D=100μA, V_{G1S}=V_{G2S}=−4V
Gate 1—Source Breakdown Voltage	BV_{G1SS}	±6.0	—	—	V	I_{G1S}=10μA, V_{DS}=V_{G2S}=0V
Gate 2—Source Breakdown Voltage	BV_{G2SS}	±6.0	—	—	V	I_{G2S}=10μA, V_{DS}=V_{G1S}=0V
Gate 1—Source Cutoff Voltage	$V_{G1S(off)}$	—	−1.5	—	V	I_D=50μA, V_{DS}=15V, V_{G2S}=4V
Gate 2—Source Cutoff Voltage	$V_{G2S(off)}$	—	—	−4.0	V	I_D=50μA, V_{DS}=15V, V_{G1S}=0V
Gate 2—Voltage Drain Current	I_{DSS}	0.2	—	25	mA	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V
Gate 1—Leakage Current	I_{G1SS}	—	—	50	nA	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V
Gate 2—Leakage Current	I_{G2SS}	—	—	50	nA	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V
Reverse Transfer Capacitance	C_{rss}	.005	.02	.03	pF	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz
Input Capacitance	C_{iss}	3.5	4.0	4.5	pF	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=200MHz
Output Capacitance	C_{oss}	—	2.5	—	pF	
Input Resistance	r_{iss}	—	1000	—	Ω	
Output Resistance	r_{oss}	—	3.5	—	kΩ	
Magnitude of Fwd Transadmittance	g_m	12	18	—	mmho	V_{DS}=+15V, V_{G2S}=+4V, f=1kHz
Conversion Power Gain Fig. 2 200MHz	G_c	—	20	—	dB	
Power Gain—200MHz	G_{ps}	20	22	—	dB	Fig. 1
Noise Figure—200MHz	N.F.	—	2.2	2.5	dB	Fig. 1



L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END.
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.
C1 0.4 TO 7pF (ARCO 400).
C2,C3 1.3 TO 5pF VARIABLE.
C4 1000pF BUTTON TYPE CAPACITOR.

Fig. 1 — 200 MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 3T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG TAP AT 3/4T FROM COLD END.
T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM.
SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO.

Fig. 2 — 200 MHz to 44 MHz MIXER TEST CIRCUIT

MEM 711

N-Channel Enhancement Mode MOSFET

FEATURES

- Monolithic Gate Protection Diode
- Low Feed-Through Capacitance
- Low ON Resistance
- Normally OFF with Zero Gate Drive

APPLICATIONS

- High Speed Analog Switches
- Linear Amplifiers
- Series-Shunt Choppers
- Synchronous Detectors
- Level Shifters
- High Input Impedance Buffers

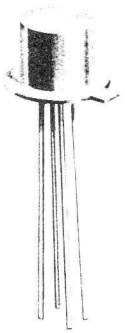
DESCRIPTION

The MEM 711 is an N-channel, Enhancement Mode, Metal Oxide Semiconductor Field Effect Transistor, protected from excessive input voltages by a monolithic zener diode between gate and substrate. This MOSFET features a low threshold limit of 1.5 volts making possible direct drive from low voltage TTL logic levels. The low ON resistance and low feed-through capacitance make the MEM 711 ideally suited for high speed analog switching.

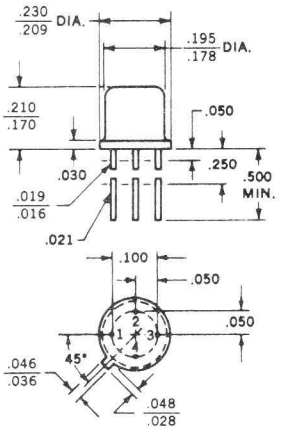
MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Drain to Source Voltage	V_{DS}	25 Volts
Gate to Source Voltage	V_{GS}	30 Volts
Gate to Drain Voltage	V_{GD}	30 Volts

Storage Temperature	−65 to 150°C
Operating Junction Temperature	−65 to 150°C
Total Dissipation @ 25°C Ambient Temperature	225 mW
@ 25°C Case Temperature	650 mW



TO-72



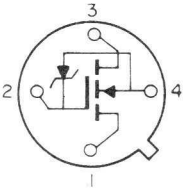
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

LEAD

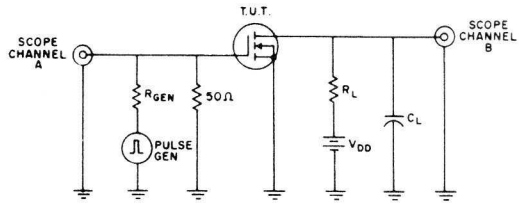
1. Source
2. Gate
3. Drain
4. Substrate, case



ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = +10V, I_D = +10μA, V_{BS} = 0V	0.50	–	1.5	V
I_{DSS}	Drain Leakage Current	V_{DS} = +10V, V_{GS} = 0V, V_{BS} = 0V	–	–	10	nA
I_{GSS}	Gate Leakage Current	V_{GS} = +10V, V_{DS} = 0V, V_{BS} = 0V	–	–	1.0	nA
BV_{DSS}	Drain Breakdown Voltage	I_D = +10μA, V_{GS} = 0V, V_{BS} = 0V	25	–	–	V
BV_{GSS}	Gate Breakdown Voltage	I_G = +10μA, V_{DS} = V_{BS} = 0V	30	–	–	V
$R_{DS(ON)}$	Drain-to-Source on Resistance	V_{GS} = +10V, I_D = 0.1mA, V_{BS} = 0V	–	–	100	ohms
$I_{D(ON)}$	Drain Current	V_{DS} = V_{GS} = +10V, V_{BS} = 0V	10	–	–	mA
Y_{fs}	Forward Transadmittance	V_{DS} = +10V, I_D = 2mA, f = 1kHz, V_{BS} = 0V	1000	–	–	μmhos
C_{iss}	Total Gate Input Capacitance	V_{GS} = 0V, V_{DS} = +10V, f = 1 MHz, V_{BS} = 0V	–	–	6.0	pF
C_{oss}	Total Drain Output Capacitance	V_{GS} = 0V, V_{DS} = +10V, f = 1 MHz, V_{BS} = 0V	–	–	5.0	pF
C_{gd}	Gate-Drain Capacitance	V_{GS} = 0V, V_{DS} = 0V, f = 1 MHz, V_{BS} = 0V	–	–	1.0	pF
$t_{d(on)}$	Turn on Delay Time	V_{DD} = 10V	–	–	3	ns
t_r	Rise Time	$I_{D(on)}$ = 10mA	–	–	5	ns
$t_{d(off)}$	Turnoff Delay Time	$V_{GS(on)}$ = 10V — See Figure 1	–	–	30	ns
t_f	Fall Time	$V_{GS(off)}$ = 0V	–	–	60	ns

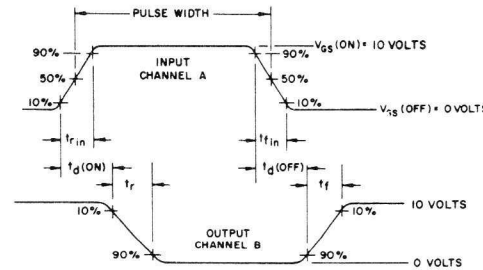
SWITCHING TEST CIRCUIT



GENERATOR:
- $t_r = t_f$ 1.5nSEC
- PULSE WIDTH 100μSEC
- DUTY CYCLE 2%
- R_{GEN} 50 OHMS

OSCILLOSCOPE:
- t_r 1nSEC
- R_{in} 10^7 OHMS
- C_{in} 1.5pF

LOAD:
- R_L 1K OHMS
- C_L 7pF INCLUDING SCOPE INPUT C
- V_{DD} 10VDC



MEM 712 MEM 712A

N-Channel Enhancement Mode MOSFET

FEATURES

- Low Cost Plastic Package
- Monolithic Gate Protection Diode
- Low Feed-Through Capacitance
- Low ON Resistance
- Normally Off with Zero Gate Drive
- Complementary Operation with MEM816

APPLICATIONS

- High Speed Analog Switches
- Linear Amplifiers
- Series-Shunt Choppers
- Synchronous Detectors
- Level Shifters
- High Input Impedance Buffers

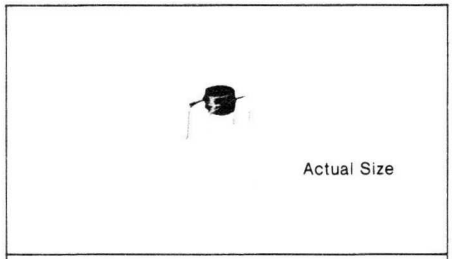
DESCRIPTION

The MEM712 is an N-channel, Enhancement Mode, Metal Oxide Semiconductor Field Effect Transistor, protected from excessive input voltages by a monolithic zener diode between gate and substrate. This MOSFET features a low threshold limit of 2.0 volts making possible direct drive from low voltage TTL logic levels. The low ON resistance, low feed-through capacitance and low cost plastic package make the MEM712 ideally suited for economical, high speed analog switching.

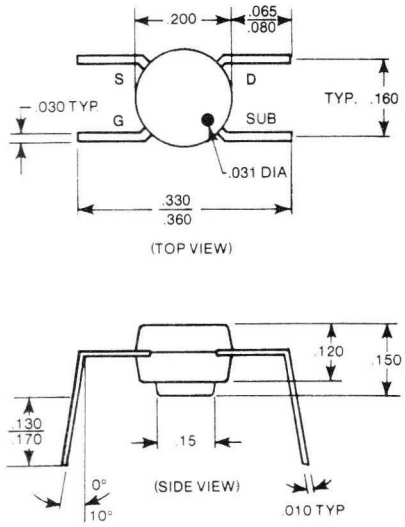
The MEM712 is a complement to General Instrument's MOSFET MEM816.

MAXIMUM RATINGS

	MEM 712	MEM 712A
Drain to Source Voltage...	25V	30V
Gate to Source Voltage ...	30V	30V
Gate to Drain Voltage.....	30V	30V
Drain Current	Limited by Dissipation	
Storage Temperature	−50 to 125°C	
Operating Junction Temperature	−50 to 85°C	
Total Dissipation	200mW	
Derate Linearly from 25°C at 3.3 mW/°C		



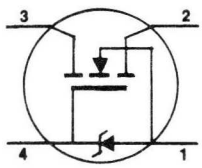
Actual Size



TERMINAL DIAGRAM

Lead

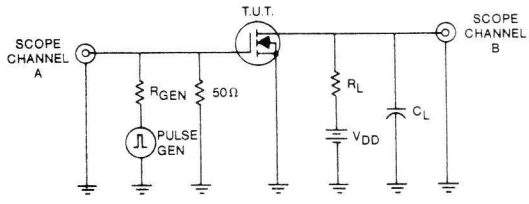
1. Substrate
2. Drain
3. Source
4. Gate



ELECTRICAL CHARACTERISTICS:

Symbol	Characteristic	Conditions	MEM 712			MEM 712A			Units
			Min	Typ	Max	Min	Typ	Max	
$V_{GS\ (th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = +10\mu A$ $V_{BS} = 0V$	0.50		2.0	0.50		2.0	V
I_{DSS}	Drain Leakage Current	$V_{DS} = +10V$, $V_{GBS} = 0V$	–	–	10	–	–	10	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = +10V$, $V_{DBS} = 0V$	–	–	1	–	–	1	nA
BV_{DSS}	Drain Breakdown Voltage	$I_D = +10\mu A$, $V_{GBS} = 0V$	20	–	–	30	–	–	V
BV_{GSS}	Gate Breakdown Voltage	$I_G = \pm 10\mu A$, $V_{DS} = V_{BS} = 0V$	30			30			V
$R_{DS\ (ON)}$	Drain-to-Source on Resistance	$V_{GS} = +10V$ $I_D = 0.1mA$ $V_{BS} = 0V$	–	50	100	–		50	Ω
$I_{D\ (ON)}$	Drain Current	$V_{DS} = V_{GS} = +10V$, $V_{BS} = 0V$	10	40	–	10	40	–	mA
Y_{fs}	Forward Transadmittance	$V_{DS} = +10V$, $I_D = 2mA$, $f = 1kHz$ $V_{BS} = 0V$	2000	–	–	2000	–	–	μmhos
C_{iss}	Total Gate Input Capacitance	$V_{GBS} = 0V$, $V_{DS} = +10V$, $F = 1MHz$	–	4.5	6.0	–	4.5	6.0	pF
C_{oss}	Total Drain Output Capacitance	$V_{GBS} = 0V$, $V_{DS} = +10V$, $f = 1MHz$	–	3.5	5.0	–	3.5	5.0	pF
C_{rss}	Feedback Capacitance	$V_{DS} = V_{GBS} = 0V$	–	0.5	0.8	–	0.5	0.8	pF
$t_{d\ (on)}$	Turn on Delay Time	$V_{DD} = 10V$	–	1.5		–	1.5		ns
t_r	Rise Time	$I_{D\ (on)} = 10mA$	–	2		–	2		ns
$t_{d\ (off)}$	Turnoff Delay Time	$V_{GS\ (on)} = 10V$	–	25		–	25		ns
t_f	Fall Time	$V_{GS\ (off)} = 0V$	–	35		–	35		ns

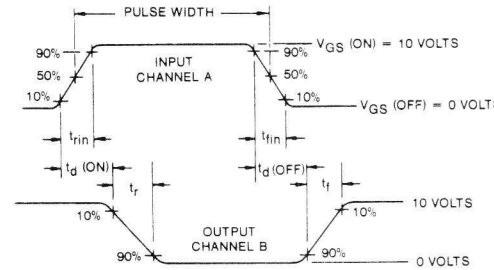
SWITCHING TEST CIRCUIT



GENERATOR:
- $t_r = t_f$ 1.5 nS
- PULSE WIDTH 100μS
- DUTY CYCLE 2%
- R_{GEN} 50 Ω

OSCILLOSCOPE:
- t_r 1 nS
- R_{in} 10^7 Ω
- C_{in} 1.5 pF

LOAD:
- R_L 1KΩ
- C_L 7pF INCLUDING SCOPE INPUT C
- V_{DD} 10 VDC



INDUSTRIAL/ MOSFET

MEM 713

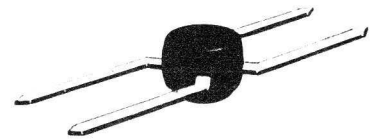
N-Channel Enhancement Mode MOSFET

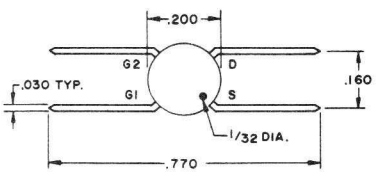
FEATURES

- 10^{13} ohms input resistance
- Normally off with zero gate voltage
- Square Law transfer characteristics
- Low insertion loss
- Low input and output capacitance

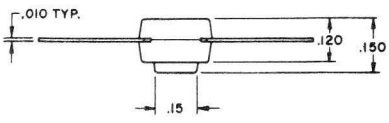
APPLICATIONS

- Logic circuits
- Switches
- Choppers
- Multiplexers
- Audio/RF Amplifier, Oscillators
- Operational Amplifiers





TOP VIEW



SIDE VIEW

LEADS CAN BE PREFORMED TO CUSTOMER SPECIFICATION.

MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

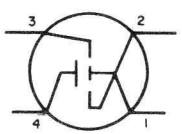
Drain to Source Voltage ..... +20 Volts
Gate to Source Voltage ..... ±10 Volts
Gate to Drain Voltage..... ±30 Volts
Drain Current I_D ..... Limited by Dissipation
Storage Temperature .....−65 to 150°C
Operating Junction Temperature .....−65 to 125°C
Total Dissipation @ 25°C Ambient Temperature 225mW
@ 25°C Case Temperature 650mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

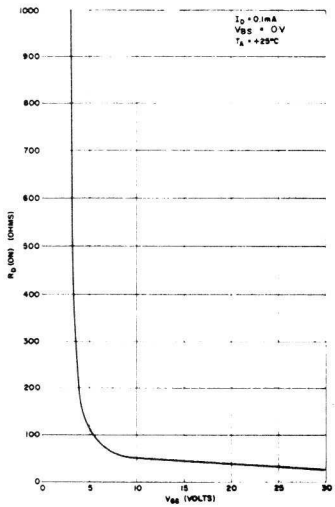
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	0.50	1.5	4.0	V	$V_{DS} = V_{GS}$, $I_D = +10\mu A$
Drain Leakage Current	I_{DSS}	—	—	10	nA	$V_{DS} = +10V$, $V_{GS} = 0V$
Gate Leakage Current	I_{GSS}	—	—	10	pA	$V_{GS} = \pm 10V$, $V_{DS} = 0V$
Drain Breakdown Voltage	BV_{DSS}	20	—	—	V	$I_D \leq +10\mu A$, $V_{GS} = 0V$
Drain-to-Source on Resistance	$R_{DS\ (ON)}$	—	—	150	ohms	$V_{GS} = +10$, $I_D = 0.1mA$
Drain Current	$I_{D\ (ON)}$	15	—	—	mA	$V_{DS} = V_{GS} = +10V$
Forward Transadmittance	Y_{fs}	2000	—	—	μmhos	$V_{DS} = +10V$, $I_D = 2mA$, f = 1kHz
Total Gate Input Capacitance	C_{iss}	—	—	6.0	pF	$V_{GS} = 0V$, $V_{DS} = +10V$, f = 1 MHz
Total Drain Output Capacitance	C_{oss}	—	—	5.0	pF	$V_{GS} = 0V$, $V_{DS} = +10V$, f = 1 MHz
Gate-to-Drain Capacitance	C_{gd}	—	—	0.8	pF	$V_{GS} = 0V$, $V_{DS} = 0V$ f = 1 MHz
Turn on Delay Time	t_d	—	—	25	nS	See Figure 1
Rise Time	t_r	—	—	35	nS	See Figure 1
Turnoff Time	$t_{(off)}$	—	—	140	nS	See Figure 1

LEAD CONFIGURATION

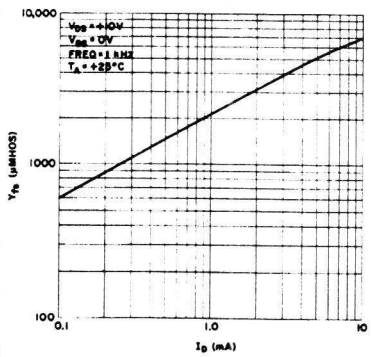
1. Substrate
2. Drain
3. Source
4. Gate



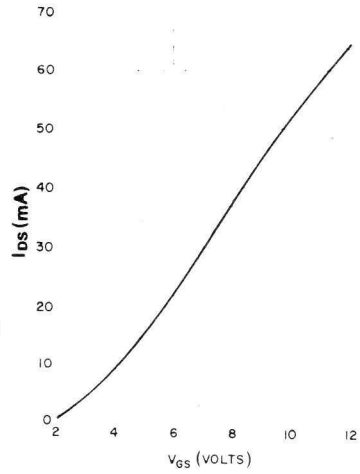
DRAIN TO SOURCE RESISTANCE vs GATE VOLTAGE



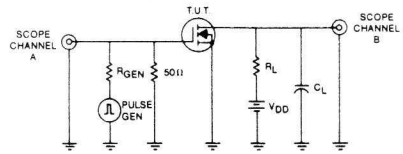
FORWARD TRANSADMITTANCE vs DRAIN CURRENT



DRAIN CURRENT vs GATE VOLTAGE TRANSFER CHARACTERISTICS



SWITCHING TEST CIRCUIT



GENERATOR:

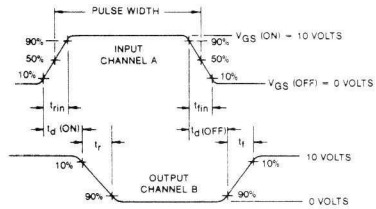
$t_r = t_f$	1.5 nS
PULSE WIDTH	100μS
DUTY CYCLE	2%
R_{GEN}	50 Ω

OSCILLOSCOPE:

t_r	1 nS
R_{in}	10^7 Ω
C_{in}	1.5 pF

LOAD:

R_L	1KΩ
C_L	7pF INCLUDING SCOPE INPUT C
V_{DD}	10 VDC



MEM 806 MEM 806A

P-Channel Enhancement Mode MOSFETS

FEATURES

- High breakdown voltage
- Low input and drain to gate capacitance
- High "off" resistance
- Very high ratio of "off" to "on" resistance
- Normally off and zero offset voltage

APPLICATIONS

- Low level chopper application
- Low level detector
- Sample and hold circuit
- Analog switching
- Muitiplexers
- Operational amplifiers

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

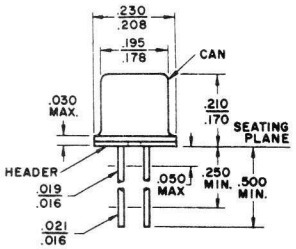
	MEM 806/MEM 806A
Drain to Source Voltage	−40V
Drain to Gate Voltage	−40V
Gate to Source Voltage	−40V
Transient Gate to Source Voltage	±125V
Storage Temperature	−65°C to +150°C
Operating Temperature	−65°C to +150°C
Total Dissipation at 25°C Case Temperature	600mW
Total Dissipation at 25°C Ambient Temperature	300mW

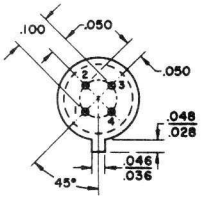
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

		MEM806		MEM806A			
SYMBOL	CHARACTERISTIC	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−2.0	−5.5	−2.0	−5.5	Volts	$V_{GS} = V_{DS}$, $I_D = 10\ \mu A$ $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current		−1.0		-0.10	nA	$V_{DS} = -20V$, $V_{GS} = V_{BS} = 0V$
I_{SDS}	Source Leakage Current		−1.0		-0.10	nA	$V_{SD} = -20V$, $V_{GD} = V_{BD} = 0V$
I_{GSS}	Gate Leakage Current		−3.0		−1.0	pA	$V_{GS} = -20V$, $V_{DS} = V_{BS} = 0V$
$I_{D(on)}$	Drain Current	−5.0		−5.0		mA	$V_{GS} = V_{DS} = -15V$
BV_{DSS}	Drain-Source Breakdown	−40		−40		Volts	$I_D = -10\ \mu A$, $V_{GS} = V_{BS} = 0V$
BV_{SDS}	Source-Drain Breakdown	−40		−40		Volts	$I_S = -10\ \mu A$, $V_{GD} = V_{BD} = 0V$
$R_{D(on)}$	Drain to Source on Resistance		300		300	ohms	$V_{GS} = -15V$, $I_D = 100\ \mu A$
Y_{fs}	Transadmittance	2000		2000		μmhos	$V_{DS} = -20V$, f = 1KHz, I_{DS}= 10mA
C_{gs}	Gate to Source Capacitance		2.0		2.0	pF	$V_{DS} = -10V$, $I_D = 10mA$
C_{ds}	Drain to Source Capacitance		0.3		0.3	pF	$V_{DS} = -10V$, $I_D = 10mA$
C_{gd}	Gate to Drain Capacitance		1.5		1.5	pF	$V_{DS} = -10V$, $I_D = 10mA$

TO-72



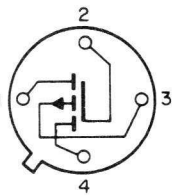


BOTTOM VIEW

Note: All dimensions in inches.

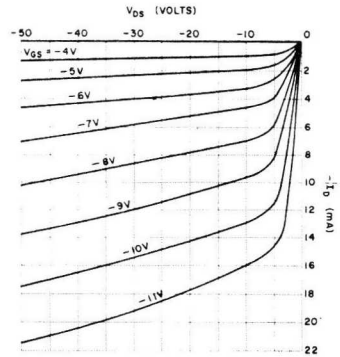
TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Substrate (Case)
4. Source

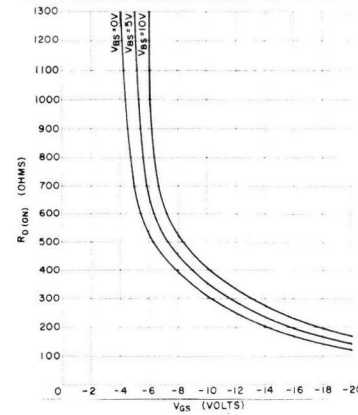


TYPICAL CHARACTERISTIC CURVES

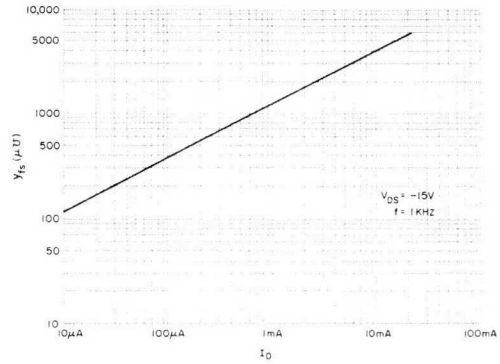
TRANSFER CHARACTERISTICS



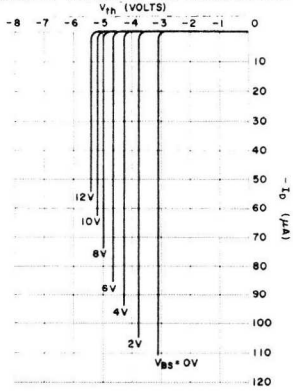
DRAIN TO SOURCE RESISTANCE vs. GATE VOLTAGE



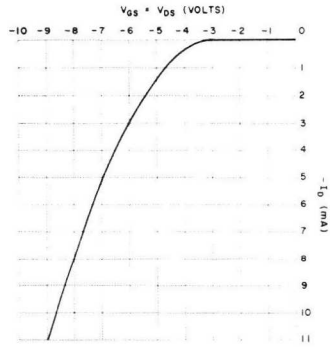
FORWARD TRANSCONDUCTANCE vs. DRAIN CURRENT



THRESHOLD VOLTAGE vs. SUBSTRATE BIAS



TURN-ON CHARACTERISTICS



INDUSTRIAL/ MOSFET

MEM 807 MEM 807A

P-Channel Enchancement Mode MOSFETS

FEATURES

- High breakdown voltage
- Low input and gate to drain capacitance
- High drain to source off resistance
- Very high ratio of "off" to "on" resistance
- Normally off with zero gate voltage
- Zener protective diode

APPLICATIONS

- Low level chopper application
- Analog switching
- Sample and hold circuit
- Multiplexers
- Audio amplifier
- Operational amplifiers

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

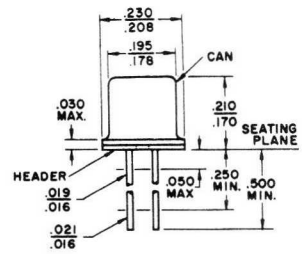
	MEM 807/MEM 807A
Drain to Source Voltage	−40V
Drain to Gate Voltage	−40V
Gate to Source Voltage	−40V
Transient Gate to Source Voltage	±125V
Storage Temperature	−65°C to +150°C
Operating Temperature	−65°C to +150°C
Total Dissipation at 25°C Case Temperature	600mW
Total Dissipation at 25°C Ambient Temperature	300mW

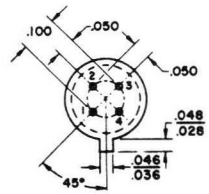
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

		MEM807		MEM807A			
SYMBOL	CHARACTERISTIC	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−2.0	−5.5	−2.0	−5.5	Volts	$V_{GS} = V_{DS}$, $I_D = 10\ \mu A$ $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current		−1.0		−0.10	nA	$V_{DS} = -20V$, $V_{GS} = V_{BS} = 0V$
I_{SDS}	Source Leakage Current		−1.0		−0.10	nA	$V_{SD} = -20V$, $V_{GD} = V_{BD} = 0V$
I_{GSS}	Gate Leakage Current		−0.20		−0.05	nA	$V_{GS} = -20V$, $V_{DS} = V_{BS} = 0V$
$I_{D(on)}$	Drain Current	−5.0		−5.0		mA	$V_{GS} = V_{DS} = -15V$
BV_{DSS}	Drain-Source Breakdown	−40		−40		Volts	$I_D = -10\ \mu A$, $V_{GS} = V_{BS} = 0V$
BV_{SDS}	Source-Drain Breakdown	−40		−40		Volts	$I_S = -10\ \mu A$, $V_{GD} = V_{BD} = 0V$
BV_{GSS}	Gate to Source Breakdown	−40		−40		Volts	$I_G = -10\ \mu A$, $V_{DS} = V_{BS} = 0V$
$R_{D(on)}$	Drain to Source on Resistance		300		300	ohms	$V_{GS} = -15V$, $I_D = 100\ \mu A$
Y_{fs}	Transadmittance	2000		2000		μmhos	$V_{DS} = -20V$, $f = 1KHz$, $I_{DS} = 10mA$
C_{gs}	Gate to Source Capacitance		2.0		2.0	pF	$V_{DS} = -10V$, $I_D = 10mA$
C_{ds}	Drain to Source Capacitance		0.3		0.3	pF	$V_{DS} = -10V$, $I_D = 10mA$
C_{gd}	Gate to Drain Capacitance		1.5		1.5	pF	$V_{DS} = -10V$, $I_D = 10mA$

TO-72



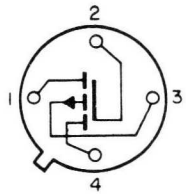


BOTTOM VIEW

Note: All dimensions in inches.

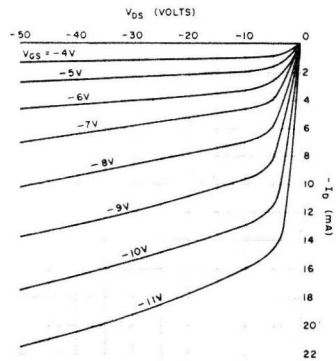
TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Substrate (Case)
4. Source

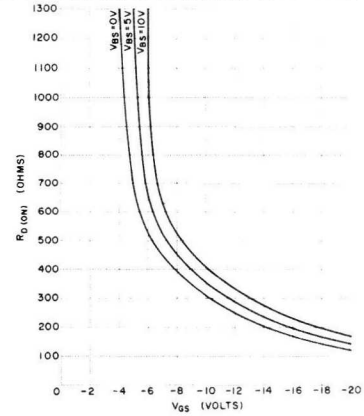


TYPICAL CHARACTERISTIC CURVES

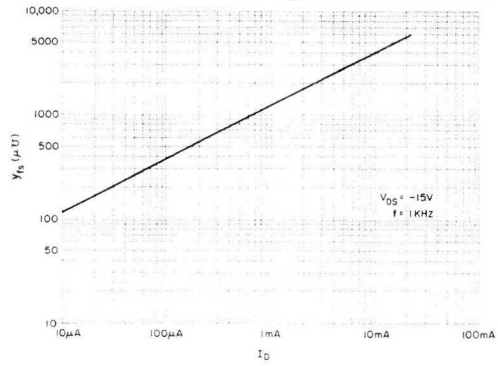
TRANSFER CHARACTERISTICS



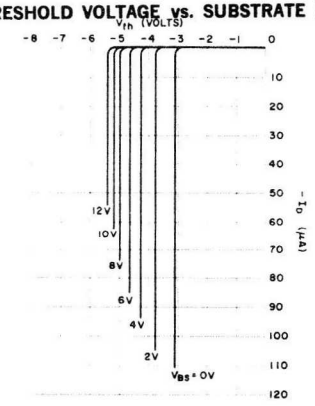
DRAIN TO SOURCE RESISTANCE vs. GATE VOLTAGE



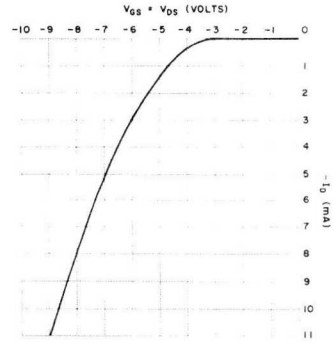
FORWARD TRANSCONDUCTANCE vs. DRAIN CURRENT



THRESHOLD VOLTAGE vs. SUBSTRATE BIAS



TURN-ON CHARACTERISTICS



MEM 814

P-Channel Enhancement Mode MOSFET

FEATURES

- Low threshold voltage
- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square law transfer characteristics
- Low input capacitance

APPLICATIONS

(Designed primarily for Audio, Radio Frequency, Chopper, Multiplex and Commutating Applications)

- High speed analog switch
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers
- Series and shunt choppers

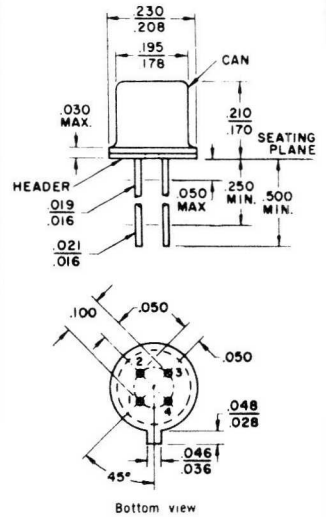
MAXIMUM RATINGS

Drain-to-Source Voltage ..... −35V
Gate-to-Source Voltage ..... −35V
Gate-to-Drain Voltage ..... −35V
Drain Current ..... −50mA
Gate Current (forward direction for zener clamp) ..... +0.1mA
Storage Temperature ..... −65 to +150°C
Operating Junction Temperature ..... −65 to +125°C
Total Dissipation at 25°C Case Temperature 900mW
Total Dissipation at 25°C Ambient Temperature 300mW

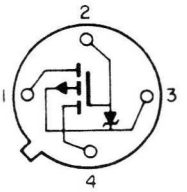
ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Gate-Source Threshold Voltage	$V_{GS\,(th)}$	−1.5	−2.0	−3.0	V	$V_{GS}=V_{DS}$, $I_D=-10\mu A$, $V_{BS}=0V$
Drain Leakage Current	I_{DSS}	—	—	−5.0	nA	$V_{DS}=-20V$, $V_{GSB}=0V$
Source Leakage Current	I_{SDS}	—	—	−5.0	nA	$V_{SD}=-20$, $V_{GDB}=0V$
Gate Leakaget Current	I_{GSS}	—	—	−500	pA	$V_{GS}=-20V$, $V_{DSB}=0V$
Drain-Source Breakdown Voltage	BV_{DSS}	−35	—	—	V	$I_D=-10\mu A$, $V_{GSB}=0V$
Source-Drain Breakdown Voltage	BV_{SDS}	−35	—	—	V	$I_S=-10\mu A$, $V_{GDB}=0V$
Gate-Source Breakdown Voltage	BV_{GSS}	−35	—	—	V	$I_G=-10\mu A$, $V_{DSB}=0V$
Drain Current	$I_{D(on)}$	−15	−20	—	mA	$V_{GS}=V_{DS}=-10V$
Drain-Source Resistance	$R_{ds\,(on)}$	—	80	125	ohms	$V_{GS}=-15V$, $I_{DS}=-0.1mA$, $V_{BS}=0V$
Transadmittance	Y_{fs}	2000	3500	—	μmhos	$V_{DS}=-10V$, $I_D=-5mA$, $V_{BS}=0V$, f=1KHz
Input Capacitance	C_{iss}	—	6.0	7.0	pF	$V_{DS}=10V$, $I_D=-5mA$, $V_{BS}=0V$, f=1MHz
Output Capacitance	C_{oss}	—	4.0	5.0	pF	$V_{DS}=-10V$, $I_D=-5mA$, $V_{BS}=0V$, f=1MHz
Drain-Gate Capacitance	C_{gd}	—	1.0	1.5	pF	$V_{DS}=-10V$, $V_{GS}=0$, $V_{BS}=0V$, f=1MHz
Gate-Source Capacitance	C_{gs}	—	1.0	1.5	pF	$V_{DS}=-10V$, $V_{GS}=0$, $V_{BS}=0V$, f=1MHz

TO-72



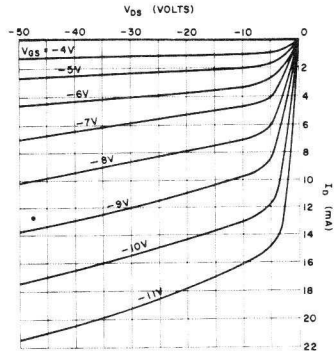
TERMINAL DIAGRAM



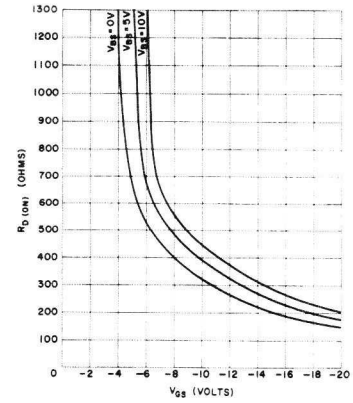
LEAD

1. Drain
2. Gate
3. Substrate (Case)
4. Source

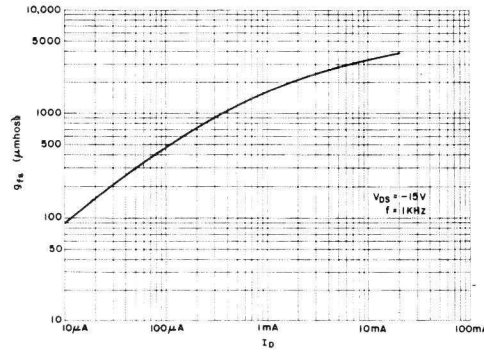
TRANSFER CHARACTERISTICS



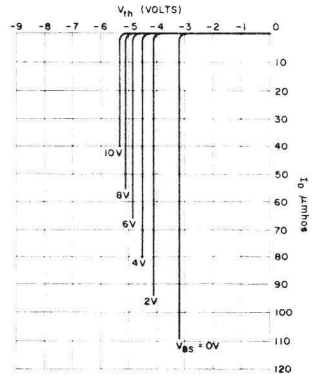
DRAIN TO SOURCE RESISTANCE vs. GATE VOLTAGE



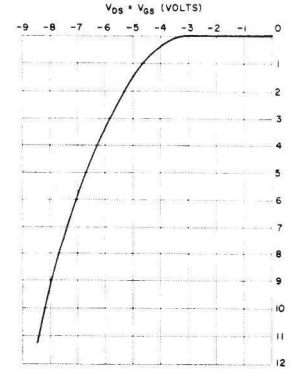
FORWARD TRANSCONDUCTANCE vs. DRAIN CURRENT



THRESHOLD VOLTAGE vs. SUBSTRATE BIAS



TURN-ON CHARACTERISTICS



MEM 816

P-Channel Enhancement Mode MOSFET

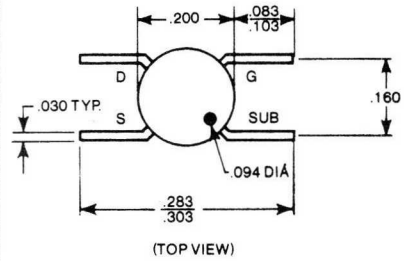
FEATURES

- 10^{10} ohms input resistance
- Monolithic Gate Protection Diode
- Normally off with zero gate drive
- Square law transfer characteristics
- Complementary Operation with MEM 712/712A

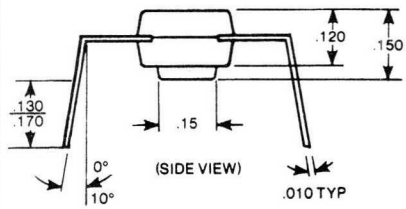
APPLICATIONS

- Analog Switches
- Series-shunt choppers
- Operational Amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers

Actual Size



(TOP VIEW)



MAXIMUM RATINGS

Drain to source Voltage ..... −30V
Gate to Source Voltage ..... −30V
Gate to Drain Voltage ..... −30V
Drain Current ..... −50mA
Gate Current (Fwd Direction for Zener Clamp) ..... +0.1mA
Storage Temperature ..... −50 To +100°C
Operating Junction Temperature ..... −50 To +85°C
Total Dissipation @ 25°C Ambient Temperature 200mW

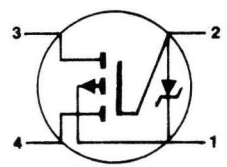
ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
$V_{GS\ (th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -10\mu A$, $V_{BS} = +10V$	−2.0	−3.5	−5.0	V
I_{DSS}	Drain Leakage Current	$V_{DS} = -20V$, $V_{GSB} = 0V$	—	—	−10	nA
I_{SDS}	Source Leakage Current	$V_{SD} = -20V$, $V_{GDB} = 0V$	—	—	−10	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = -20V$, $V_{DSB} = 0V$	—	—	−1	nA
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -10uA$, $V_{GSB} = 0V$	−30	—	—	V
BV_{SDS}	Source-Drain Breakdown Voltage	$I_S = -10uA$, $V_{GDB} = 0V$	−30	—	—	V
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -10uA$, $V_{DSB} = 0V$	−30	—	—	V
$I_{D\ (on)}$	Drain Current	$V_{GS} = V_{DS} = -10V$, $V_{BS} = +10V$	−10	—	—	mA
$R_{ds\ (on)}$	Drain-Source Resistance	$I_{DS} = -0.1mA$, $V_{BS} = 10V$, $V_{GS} = -10V$	—	—	300	Ω
Y_{fs}	Transadmittance	$V_{DS} = -10V$, $I_D = -5mA$, $V_{BS} = 0V$, $f = 1kHz$	2000	3000	—	μmhos
C_{iss}	Input Capacitance	$V_{DS} = -10V$, $I_D = -5mA$, $V_{BS} = 0V$, $f = 1MHz$	—	—	5.0	pF
C_{oss}	Output Capacitance	$V_{DS} = -10V$, $I_D = -5mA$, $V_{BS} = 0V$, $f = 1MHz$	—	—	8.5	pF
C_{gd}	Drain-Gate Capacitance	$V_{DS} = -10V$, $I_D = -5mA$, $V_{BS} = 0V$, $f = 1MHz$	—	—	4.5	pF

TERMINAL DIAGRAM

Lead

1. Substrate
2. Gate
3. Drain
4. Source



MEM 817

P-Channel Enhancement Mode MOSFETS

FEATURES

- High breakdown voltage
- Low input and drain to gate capacitance
- High "off" resistance
- Very high ratio of "off" to "on" resistance
- Normally off and zero offset voltage

Actual Size

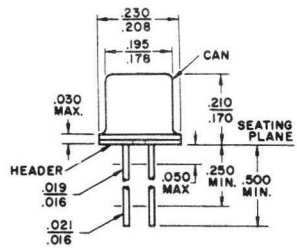
APPLICATIONS

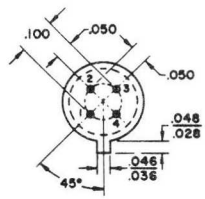
- Low level chopper application
- Low level detector
- Sample and hold circuit
- Analog switching
- Multiplexers
- Operational amplifiers
- Smoke Detector

MAXIMUM RATINGS

Drain to Source Voltage	45V
Drain to Gate Voltage	45V
Gate to Source Voltage	±200V
Storage Temperature	-50°C to 150°C
Operating Temperature	-50°C to 125°C
Total Dissipation at 25°C Case Temperature	400mW
Total Dissipation at 25°C Ambient Temperature	225mW

TO-72





Bottom View

Note: All dimensions in inches.

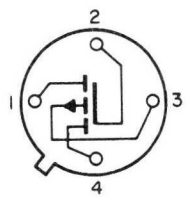
ELECTRICAL CHARACTERISTICS Body Connected To Source.

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{GS\,(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = -20V$, $I_{DS} = -10\mu A$	-2.5	—	-5.5	V
I_{DSS}	Drain Leakage Current	$V_{DS} = -20V$, $V_{GS} = 0V$	—	—	-3	nA
I_{SDS}	Source Leakage Current	$V_{SD} = -20V$, $V_{GBD} = 0V$	—	—	-5	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = -25V$, $V_{DS} = 0V$	—	—	-1	pA
BV_{DSS}	Drain Breakdown Voltage	$I_{DS} = -10\mu A$, $V_{GS} = -0V$	-35	-45	—	V
BV_{GOX}	Gate, Oxide Breakdown Voltage	$V_{DS} = 0V$	±200	±225	—	V
$I_{D\,(on)}$	Drain Current	$V_{GS} = V_{DS} = -10V$	-3	-12	—	mA
$R_{D\,(on)}$	Drain-to-Source on resistance	$V_{GS} = -15V$, $I_{DS} = -1mA$	—	—	350	Ω
Y_{fs}	Forward Transadmittance	$V_{GS} = V_{DS} = -10V$	1000	2000	—	μmhos
C_{iss}	Total Gate Input Capacitance	$V_{GS} = V_{DS} = -10V$ f = 1MHz	—	3.5	6	pF
C_{oss}	Total Drain Output Capacitance	$V_{GS} = V_{DS} = -10V$, f = 1MHz	—	2.5	5	pF
C_{rss}	Reverse Transfer Capacitance	$V_{GS} = V_{DS} = -10V$, f = 1MHz	—	1.2	2.5	pF
A_{GS}	Voltage Gain As Source Follower	$V_{DS} = -15V$, R = 10K (Source) R(from gate to ground) = 10^9 ohms	—	0.8	—	—

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



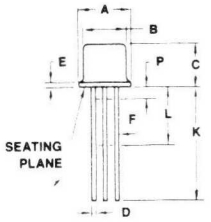
INDUSTRIAL/ MOSFET

MEM 823

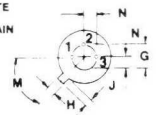
P-Channel Enhancement Mode MOSFET

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain to Source Voltage ..... −35V
Drain to Gate Voltage ..... ±200V
Gate to Source Voltage ..... ±200V
Storage Temperature ..... 50°C to 150°C
Operating Temperature ..... 50°C to 125°C
Total Dissipation @ 25°C Case Temperature ..... 400 mW
Total Dissipation @ 25°C Ambient Temperature ..... 225 mW



PIN 1 SOURCE SUBSTRATE CASE
2 GATE
3 DRAIN



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E		0.762	—	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	—	1.27	—	0.050

LEAD CONFIGURATION

1. Drain
2. Gate
3. Source, Case, & Substrate

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	−2.5	—	−5.0	V	V_{DS}= −20V, I_{DS}= −10μA
Drain Leakage Current	I_{DSS}	—	—	−3	nA	V_{DS}= −20V, V_{GS} = 0V
Source Leakage Current	I_{SDS}	—	—	−5	nA	V_{SD} = −20V, V_{GBD}=0V
Gate Leakage Current	I_{GSS}	—	—	−1	pA	V_{GS}= −25V, V_{DS}=0V
Drain Breakdown Voltage	BV_{DSS}	−35	−45	—	V	I_{DS}= −10μA, V_{GS}=0V
Gate Oxide Breakdown Voltage	BV_{GOX}	±200	±225	—	V	V_{DS}=0V
Drain Current	$I_{D(on)}$	−3	−12	—	nA	V_{GS}=V_{DS}= −10V
Drain-to-Source ON Resistance	$R_{D(on)}$	—	—	350	Ohms	V_{GS}= −15V, I_{DS}= −1mA
Forward Transadmittance	Y_{fs}	1000	2000	—	μmhos	V_{GS}=V_{DS}= −10V
Total Gate Input Capacitance	C_{iss}	—	3.5	6	pF	V_{GS}=V_{DS}= −10V, f=1MHz
Total Drain Output Capacitance	C_{oss}	—	2.5	5	pF	V_{GS}=V_{DS}= −10V, f=1MHz
Reverse Transfer Capacitance	C_{rss}	—	1.2	—	pF	V_{GS}=V_{DS}= −10V, f=1MHz
Voltage Gain as Source Follower	A_{GS}	—	0.8	—	—	V_{DS}= −15V, R=10K (Source) R (from gate to ground) = 10^9 ohms

MEM 954 Series
MEM 955 Series

Dual P-Channel Enhancement Mode MOSFETS

FEATURES

- Normally off with zero gate voltage
- Square law transfer characteristics
- Tight V_{GS} match
- Low temperature coefficient of ΔV_{GS}
- Specified for audio noise
- Low leakage currents
- 10^{15} OHMS input resistance (MEM 955 Series)
- 10^{12} OHMS input resistance (MEM 954 Series)
- Integrated zener clamp protects the gate (MEM 954 Series)

APPLICATIONS

Very high input impedance amplifiers
Series and shunt choppers
Operational amplifiers
Smoke detectors
Cryogenic amplifiers
Multiplexers
Analog switches

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

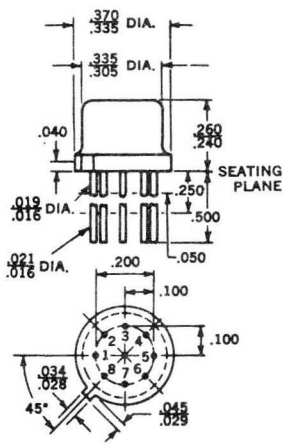
Drain to source voltage ..... -35V
Source to drain voltage ..... -35V
Gate to source voltage ..... -40V
Gate to drain voltage ..... -40V
Gate current ..... +0.1 mA
(Fwd. direction for zener clamp) (MEM 954 Series)
Drain current ..... -50 mA each side
Storage temperature ..... -50°C to +150°C
Operating junction temperature ..... -50°C to +125°C
Total dissipation at 25°C case temperature ..... .300 mW each side
Total dissipation at 25°C ambient temperature ..... .112 mW each side

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified—body grounded)

Characteristics	Symbol	MEM	Min	Typ	Max	Units	Conditions
Drain-Source Breakdown	BV_{DSS}		-35	–	–	V	V_{GS}=0V, V_{BS}=0V, I_D=-10μA
Source-Drain Breakdown	BV_{SDS}		-35	–	–	V	V_{GD}=0V, V_{BD}=0V, I_D=10μA
Gate-Source Breakdown	BV_{GSS}		-40	–	–	V	V_{DS}=V_{BS}=0V, I_G= -10μA
Gate-Source Threshold Voltage	$V_{GS(TH)}$		-2.0	-3.5	-5.0	V	V_{DS}=V_{GS}, I_D= -10μA
Drain To Source On Resistance	$R_{DS(ON)}$	954 Series 955 Series	–	100	150	Ω	V_{GS}= -15V, V_{BS}=0V, I_D=0.1 mA
Forward Transadmittance	Y_{fs}		700	1400	–	μmho	V_{DS}= -10V, I_D=500μA, V_{BS}=0V, f=1.0kHz
Transadmittance Ratio	Y_{fs1}/Y_{fs2}		0.9	–	1.1	–	V_{DS}= -10V, I_D=500μA, V_{BS}=0V, f=1.0kHz
Equivalent Input Noise Voltage	e_{n1}		–	–	700	$\frac{nV}{\sqrt{Hz}}$	V_{DS}= -10V, I_D=500μA, V_{BS}=0V, f=100Hz, BW=1Hz
Equivalent Input Noise Voltage	e_{n2}		–	–	175	$\frac{nV}{\sqrt{Hz}}$	V_{DS}= -10V, I_D=500μA, V_{BS}=0V f=1.0kHz, BW=1Hz
Drain Leakage Current	I_{DSS}	954, 954A, 955, 955A 954B, 955B	– –	.08 .05	1.0 .30	nA	V_{DS}= -20V, V_{GS}=V_{BS}=0V
Source Leakage Current	I_{SDS}	954, 954A, 955, 955A 954B, 955B	– –	.08 .05	1.0 .30	nA	V_{SD}= -20V, V_{GD}=V_{BD}=0V
Gate Leakage Current	I_{GSS}	954 954A, 954B 955, 955A 955B	– – – –	.03 .03 .02 .02	.30 .10 2.0 1.0	nA pA 	V_{GS}= -20V, V_{BS}=V_{DS}=0V V_{GS}= -40V, V_{BS}=V_{DS}=0V
Gate Voltage Differential	$\lvert V_{G1S}-V_{G2S}\rvert$	954, 955 954A, 955A 954B, 955B	– – –	– – –	75 25 10	mV	V_{DS}= -10V, I_D=500μA, V_{BS}=0V
Gate Voltage Differential Temp. Coeff T_1=25°C, T_2=100°C	$\frac{\Delta\lvert V_{G1S}-V_{G2S}\rvert}{\Delta T}$	954, 955 954A, 955A 954B, 955B	– – –	– – –	150 50 25	μV/°C	V_{DS}= -10V, I_D=500μA, V_{BS}=0V

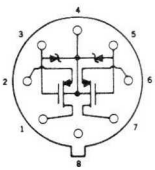
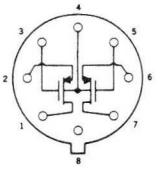
TO-77



Bottom view of 8 lead header
Note: All dimensions in inches

TERMINAL DIAGRAM

Lead
1. Drain 1
2. Source 1
3. Gate 1
4. Substrate (Body)
5. Gate 2
6. Source 2
7. Drain 2
8. Open

MEM 954 Series	MEM 955 Series
	

INDUSTRIAL/ MOSFET

MICRO ELECTRONICS

MOSFET ANALOG SWITCHES

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
ANALOG SWITCHES	4 CHANNEL SWITCH	MEM780	9-124
		MEM781	9-124
		MEM851	9-126
	6 CHANNEL SWITCH	MEM855	9-132
		MEM856	9-134
	8 CHANNEL SWITCH	MEM857	9-136
	10 CHANNEL SWITCH	MEM853	9-128
DRIVER	4 CHANNEL DRIVER	MEM4900	9-140

MEM 780 P/D/F
MEM 781 P/D/F

Four Channel MOSFET Analog Switches

FEATURES

- 20 Volt pk.-pk. signal input range
- Capacity symmetry between Cgd & Cgs
- Capacity symmetry between C_{Bd} & C_{BS}
- Crss x $R_{D(on)}$ product-6 pico secs Typical
- Matched low $r_{ds(on)}$
- Nanosecond switching times
- Low Cgd −0.3pF typical
- High $I_{D(on)}$ −75mA typical
- Low drive voltages— ±6 Volts
- Zener clamp protection
- Low crosstalk
- Low harmonic distortion
- MEM 780: 4 inputs—2 outputs
- MEM 781: individual channels

APPLICATIONS

- High speed multiplexers
- Memory read-write gates
- Memory read gates
- High speed choppers
- Video switching
- High speed quad mixers
- High speed mod-demods
- High speed dual differential switch

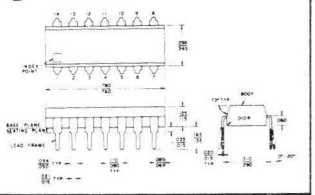
MAXIMUM RATINGS

Drain to Source Voltage ..... ±20V
Gate to Source Voltage ..... +30V to −20V
Drain to Gate Voltage ..... +30V to −12V
Substrate to All Terminals ..... −30V to +1.0V
Gate Current (FWD Direction) ..... ±0.1mA
Drain Current ..... limited by dissipation
Storage Temperature ..... −65°C to +150°C
Operating Temperature (P Package) ..... −65°C to 85°C
Operating Temperature (D/F Package) ..... −65°C to 125°C
Total Dissipation @T_C=25°C ..... 300mW per channel
Total Dissipation @T_A=25°C ..... 150mW per channel

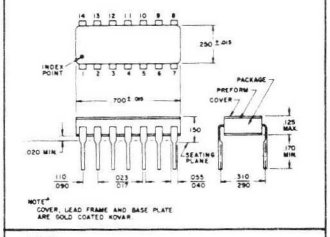
ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
$V_{GS(off)}$	Gate to Source Cutoff Voltage	V_{DS}=+10V I_D=100μa V_{BS}=−6V	—	−0.3	−2.0	V
I_{DSX}	Drain to Source Leakage Current	V_{DS}=+6V V_{GS}=V_{BS}=−6V	—	2.0	10	nA
I_{SDX}	Source to Drain Leakage Current	V_{SD}=+6V V_{GD}=V_{BD}=−6V	—	2.0	10	nA
I_{GS}	Gate to Source Leakage Current	V_{GS}=±10V Body Open	—	—	±10	nA
$I_{D(on)}$	Drain Current	V_{GS}=+6V V_{DS}=+3V V_{BS}=−6V	50	80	—	mA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=+6V V_{BS}=−6V V_{GS}=0V	—	1.0	10	mA
BV_{DSX}	Drain to Source Breakdown Voltage	V_{GS}=V_{BS}=−6V I_{DS}=+10μa	10	—	—	V
BV_{SDX}	Source to Drain Breakdown Voltage	V_{GD}=V_{BD}=−6V I_{SD}=+10μa	10	—	—	V
BV_{GB}	Gate to Substrate Breakdown Voltage	I_{GB}=±10μa	+20 −6	—	—	V
C_{iss}	Input Capacitance	V_{SB}=V_{DB}=0V	—	4.0	7.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+10V I_D=10mA f=44MHz	—	−0.3	1.0	pF
C_{oss}	Output Capacitance	V_{GS}=+6V	—	2.0	5.0	pF
$r_{ds(on)}$	Drain to Source On-Resistance	V_{BS}=−6V I_D=1.0mA	10	15	30	Ω

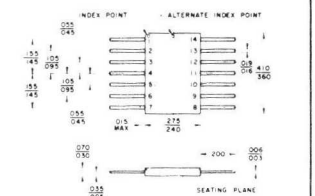
P 14 LEAD PLASTIC



D 14 LEAD CERAMIC DIP



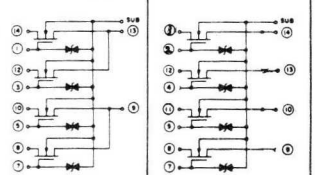
F 14 LEAD FLAT PACK



All dimensions in inches

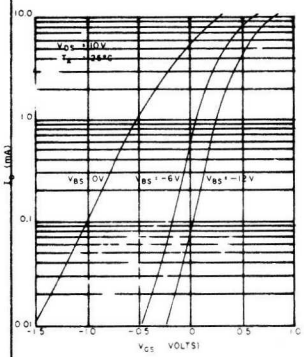
TERMINALS

PIN FUNCTION	PIN FUNCTION
1. Gate 1	1. Source 1
2. Substrate	2. Gate 1
3. Gate 3	3. Substrate
4. Substrate	4. Gate 2
5. Gate 3	5. Gate 3
6. Substrate	6. Substrate
7. Gate 4	7. Gate 4
8. Source 4	8. Source 4
9. Drain 3 & 4	9. Drain 4
10. Source 3	10. Drain 3
11. Substrate	11. Source 3
12. Source 2	12. Source 2
13. Drain 1 & 2	13. Drain 2
14. Source 1	14. Drain 1

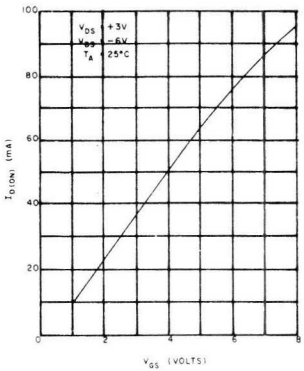


TYPICAL CHARACTERISTIC CURVES

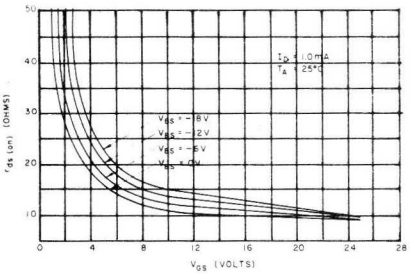
I_D vs. V_{GS} V_{BS} parameter



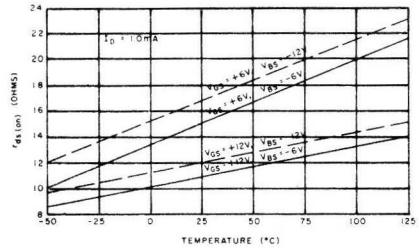
$I_{D(on)}$ vs. V_{GS}



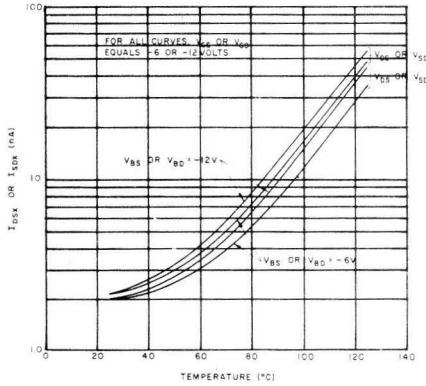
$r_{ds(on)}$ vs. V_{GS} V_{BS} parameter



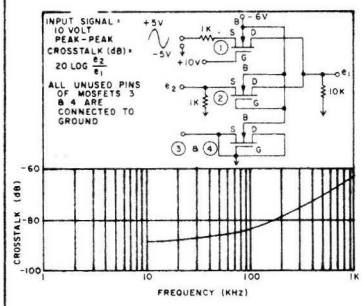
$r_{ds(on)}$ vs. TEMPERATURE V_{GS}, V_{BS} parameter



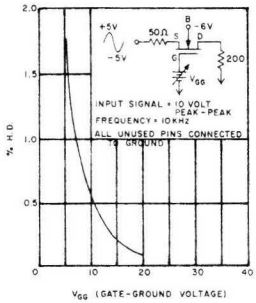
I_{DSX} or I_{SDX} vs. TEMPERATURE



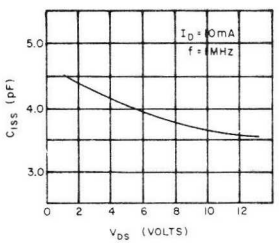
CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GG}



INPUT CAPACITANCE vs. V_{DS}



INDUSTRIAL/ MOSFET

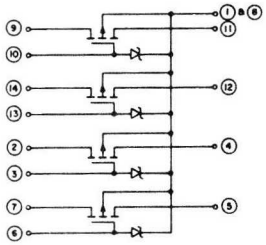
MEM 851P/D/F

Four Channel MOSFET Analog Switch

FEATURES

- 30 volt peak-peak signal input range
- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- Low "on" Resistance
- Low harmonic distortion

CIRCUIT DIAGRAM



APPLICATIONS

High speed analog multiplexing
Time division multiplexing
Series/shunt chopping
2-channel differential switch
Double pole-double throw switch
Digital switching

MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

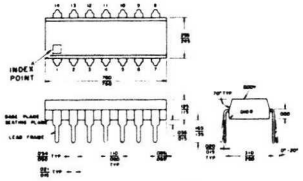
Drain to Source Voltage	−35V
Gate to Source Voltage	−35V
Gate to Drain Voltage	−35V
Drain Current	−50 mA
Gate Current (forward direction for zener clamp)	+0.1 mA
Storage Temperature	− 65 to 150°C
Operating Junction Temperature (851P)	− 65 to 85°C
Operating Junction Temperature (851 D/F)	− 65 to 125°C
Total dissipation at 25°C Ambient Temperature	600 mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	150 mW

ELECTRICAL CHARACTERISTICS

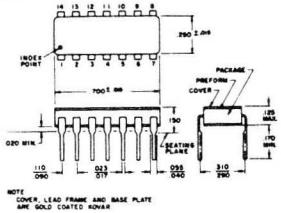
(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	- 1.0	—	-4.0	Volts	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$, $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current	—	—	−2.0	nA	$V_{DS} = -20V$, $V_{GSB} = 0V$
I_{SDS}	Source Leakage Current	—	—	−2.0	nA	$V_{SD} = -20V$, $V_{GDB} = 0$
I_{GSS}	Gate Leakage Current	—	−0.1	−1.0	nA	$V_{GS} = -20V$, $V_{DSB} = 0V$
$I_{D(ON)}$	Drain Current	− 5.0	—	—	mA	$V_{GS} = V_{DS} = -10V$, $V_{BS} = 0V$
BV_{DSS}	Drain—Source Breakdown	−35	—	—	Volts	$I_D = -10\ \mu A$, $V_{GSB} = 0V$
BV_{SDS}	Source—Drain Breakdown	−35	—	—	Volts	$I_S = -10\ \mu A$, $V_{GDB} = 0V$
BV_{GSS}	Gate—Source Breakdown	−35	—	−80	Volts	$I_G = -10\ \mu A$, $V_{DSB} = 0V$
Y_{fs}	Transadmittance	—	1500	—	μmho	1 kHz, $V_{DS} = -10V$, $I_D = -5$ ma
C_{gs}	Gate To Source Capacitance	—	—	3.0	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{gd}	Gate To Drain Capacitance	—	—	3.0	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{ds}	Drain To Source Capacitance	—	0.04	0.10	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain To Source On Resistance	—	—	100	Ohms	$V_{GS} = -20V$, $I_D = -100\mu A$, $V_{BS} = 0V$
$V_{DS(on)}$	Drain-Source "ON" Voltage	—	—	0.4	Volts	$V_{GS} = -10V$, $I_D = -2mA$
tr	Rise Time	—	—	25	ns	$V_{DD} = V_{GG} = -15V$
tf	Fall Time	—	—	130	ns	$R_D = R_G = 1.5K\Omega$

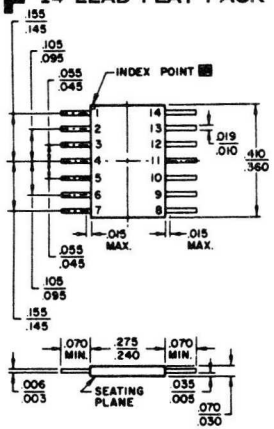
P 14 LEAD PLASTIC



D 14 LEAD CERAMIC DIP



F 14 LEAD FLAT PACK



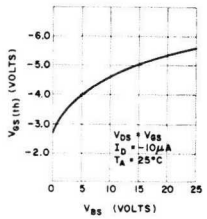
All dimensions in inches

TERMINALS

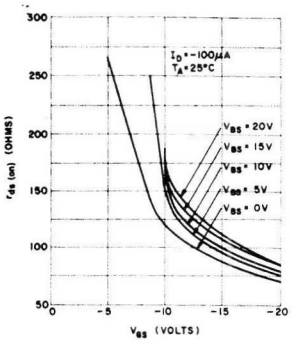
PIN	FUNCTION	PIN	FUNCTION
1	Substrate	8	Substrate
2	Drain 3	9	Drain 1
3	Gate 3	10	Gate 1
4	Source 3	11	Source 1
5	Source 4	12	Source 2
6	Gate 4	13	Gate 2
7	Drain 4	14	Drain 2

TYPICAL CHARACTERISTIC CURVES

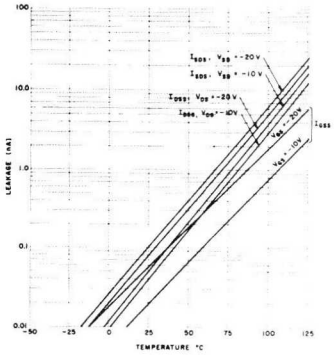
$V_{GS(th)}$ vs. V_{BS}



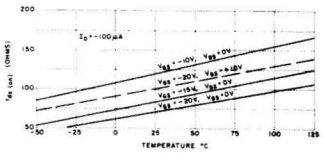
$r_{ds(on)}$ vs. V_{GS} V_{BS} parameter



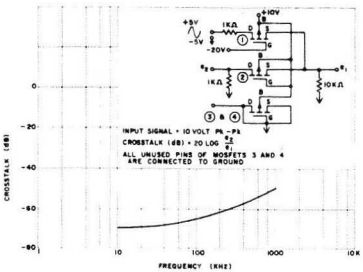
LEAKAGE vs. TEMPERATURE



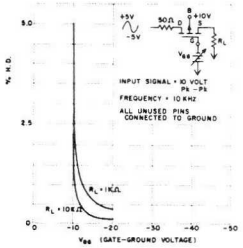
$r_{ds(on)}$ vs. TEMPERATURE V_{GS}, V_{BS} parameter



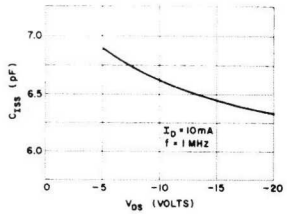
CROSSTALK (dB) vs. FREQUENCY



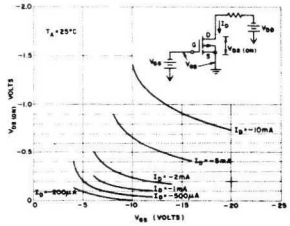
HARMONIC DISTORTION vs. V_{GG} R_L parameter



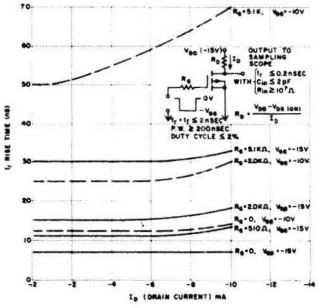
INPUT CAPACITANCE vs. V_{DS}



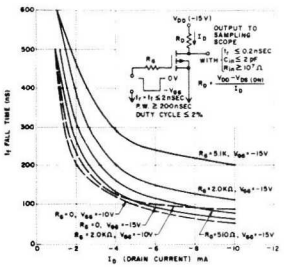
$V_{DS(on)}$ vs. V_{GS} I_D parameter



RISE TIME vs. DRAIN CURRENT R_G, V_{GG} parameter



FALL TIME vs. DRAIN CURRENT R_G, V_{GG} parameter



MEM 853P/D/F

Ten Channel MOSFET Analog Switch

FEATURES

- 25 Volt Peak-Peak Signal Input Range
- Low Threshold
- 10^{10} Ohms Input Resistance
- Integrated Zener Clamp Protection
- Normally Off with Zero Gate Voltage
- Square Law Linear Transfer Characteristics
- Low Crosstalk
- Low Leakage Presented to the Summing Junction
- Low "ON" Resistance
- Low Harmonic Distortion
- Less Than a 20 Ohm Change of "ON" Resistance from Channel to Channel

APPLICATIONS

Analog Multiplexing
Time Division Multiplexing
Chopper
4-channel Differential Switch
Serial to Parallel & Parallel to Serial Converter

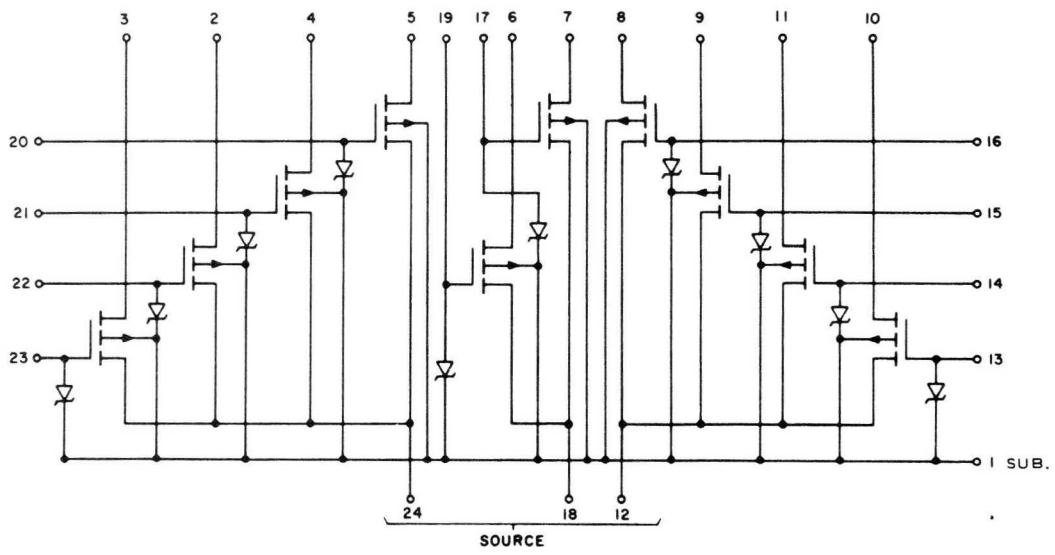
DESCRIPTION

This multiple switch contains 10 nitride passivated insulated gate field effect transistors. The sources are connected in such a way as to afford maximum flexibility for switching applications.

By properly biasing the devices, they can be used either as multiple switches, rotary switches, "AND" gates or "NOR" gates.

The nitride passivation process enables this device to have a low threshold voltage capability.

CIRCUIT DIAGRAM



MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

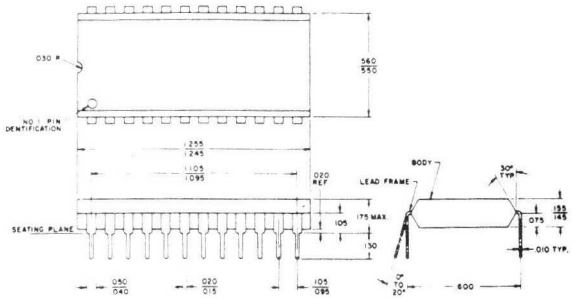
Drain to Source Voltage	−30V
Gate to Source Voltage	−30V
Gate to Drain Voltage	−30V
Drain Current	50mA
Gate Current (forward direction for Zener clamp)	+0.1mA
Storage Temperature	−65°C to 150°C
Operating Junction Temperature (853P)	−65°C to 85°C
Operating Junction Temperature (853 D/F)	−65°C to 125°C
Total Dissipation at 25°C Ambient Temperature	1.75W
Total Dissipation at 25°C Ambient Temperature for each gate circuit	175mW

ELECTRICAL CHARACTERISTICS

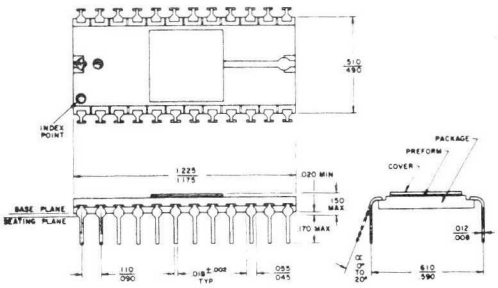
(T_A = 25°C unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate-Source Cutoff Voltage	1.5	—	4.5	Volts	$V_{DS} = V_{GS}$, $I_D = -10\mu A$, $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current	—	—	5	nA	$V_{DS} = -20V$, $V_{GSB} = 0$
I_{SDS} S1-4 S5-6 S7-10	Source Leakage Current	—	—	20 10 20	nA	$V_{SD} = -20V$, $V_{GDB} = 0$
I_{GSS}	Gate Leakage Current	—	—	1.0	nA	$V_{GS} = -20V$, $V_{DSB} = 0$
$I_{D(on)}$	Drain Current	10	—	—	mA	$V_{DS} = V_{GS} = -10V$, $V_{BS} = 0$
BV_{DSS}	Drain-Source Breakdown Voltage	30	—	—	Volts	$I_{DS} = -10\mu A$, $V_{GSB} = 0$
BV_{SDS}	Source-Drain Breakdown Voltage	30	—	—	Volts	$I_{SD} = -10\mu A$, $V_{GDB} = 0$
BV_{GSS}	Gate-Source Breakdown Voltage	30	—	—	Volts	$I_{GS} = -10\mu A$, $V_{DSB} = 0$
Y_{fs}	Transadmittance	1500	—	—	μmhos	$V_{DS} = -10V$, $I_D = -5mA$, f = 1kHz, $V_{BS} = 0$
C_{gs}	Gate-Source Capacitance	—	1.5	2.5	pF	$V_{GS} = V_{DS} = -10V$, f = 1MHz
C_{gd}	Gate-Drain Capacitance	—	1.0	2.0	pF	$V_{GS} = V_{DS} = -10V$, f = 1MHz
C_{ds}	Drain-Source Capacitance	—	0.04	0.10	pF	$V_{GS} = V_{DS} = -10V$, f = 1MHz
$r_{DS(on)}$	Drain-Source On Resistance	—	—	150	Ohms	$V_{GS} = -20V$, $I_D = -100\mu A$, $V_{BS} = 0$

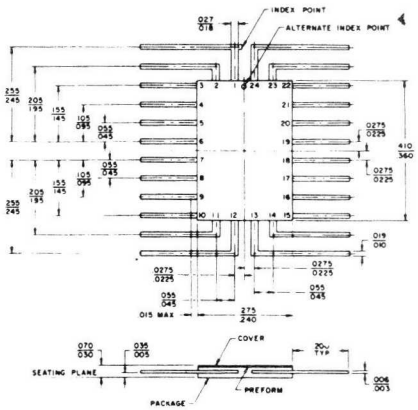
P 24 LEAD PLASTIC



D 24 LEAD CERAMIC DIP



F 24 LEAD FLAT PACK

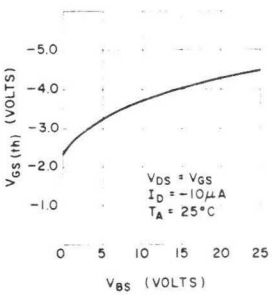


TERMINALS

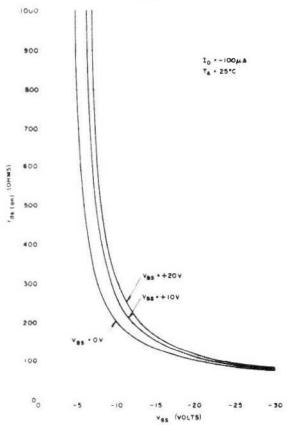
P/N	FUNCTION	P/N	FUNCTION
1	Substrate	13	Gate 8
2	Drain 2	14	Gate 7
3	Drain 1	15	Gate 6
4	Drain 3	16	Gate 5
5	N.C.	17	N.C.
6	Drain 4	18	N.C.
7	Drain 5	19	N.C.
8	N.C.	20	Gate 4
9	Drain 6	21	Gate 3
10	Drain 8	22	Gate 2
11	Drain 7	23	Gate 1
12	Source 5-8	24	Source 1-4

TYPICAL CHARACTERISTIC CURVES

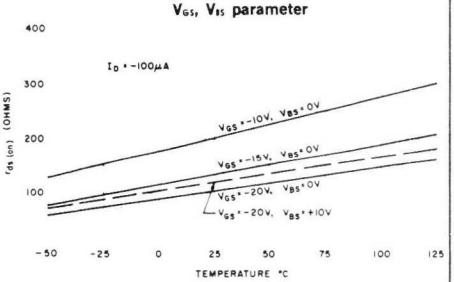
$V_{GS(th)}$ vs. V_{BS}



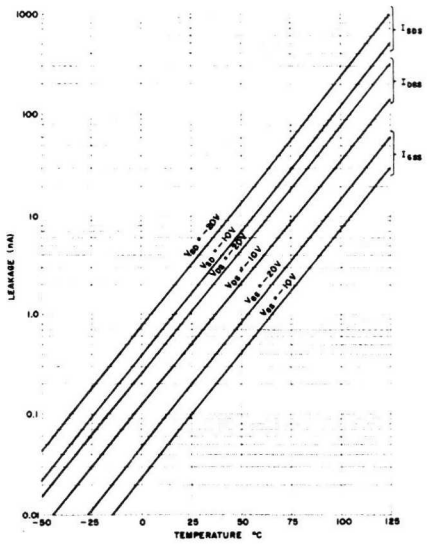
$r_{ds(on)}$ vs. V_{GS}
V_{BS} parameter



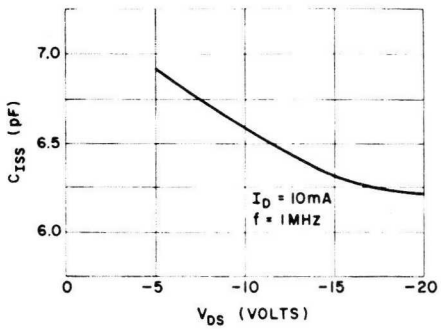
$r_{ds(on)}$ vs. TEMPERATURE
V_{GS}, V_{BS} parameter



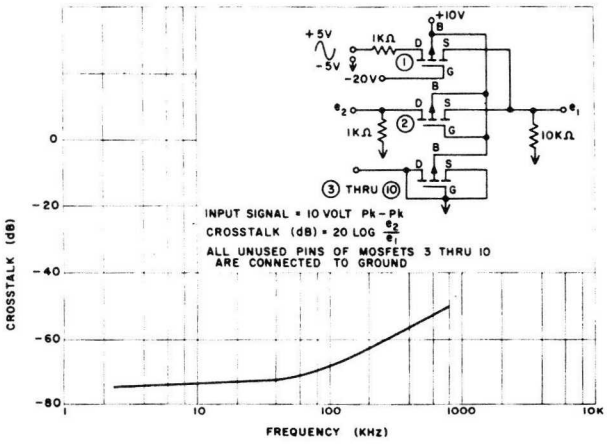
LEAKAGE vs. TEMPERATURE



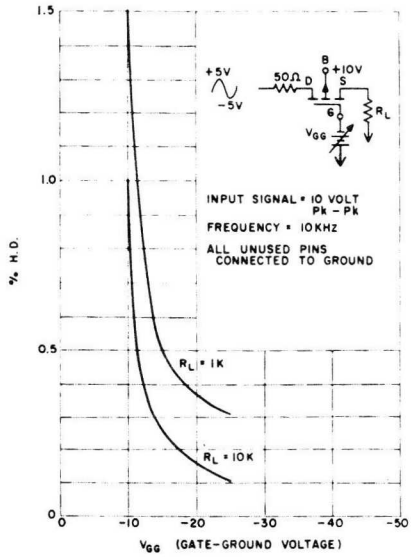
INPUT CAPACITANCE vs. V_{DS}



CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GG}
R_L parameter



INDUSTRIAL/ MOSFET

Six Channel MOSFET Analog Switch

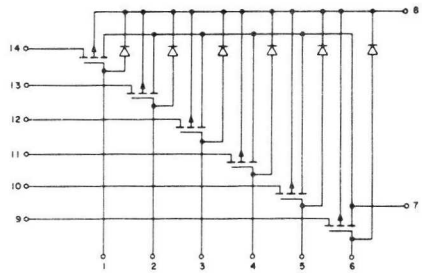
FEATURES

- 25 volt peak-peak signal input range
- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- Low "on" Resistance
- Low harmonic distortion

APPLICATIONS

- Analog Multiplexing
- Time division multiplexing
- Chopping
- Serial to parallel & parallel to serial converter

CIRCUIT DIAGRAM



MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

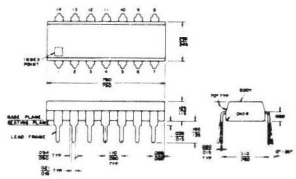
Drain to Source Voltage	—35V
Gate to Source Voltage	—40V
Gate to Drain Voltage	—40V
Drain Current	—50 mA
Gate Current (forward direction for zener clamp)	+0.1 mA
Storage Temperature	—65 to 150°C
Operating Junction Temperature (855P)	—65 to 85°C
Operating Junction Temperature (855 D/F)	—65 to 125°C
Total dissipation at 25°C Ambient Temperature	900 mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	150 mW

ELECTRICAL CHARACTERISTICS

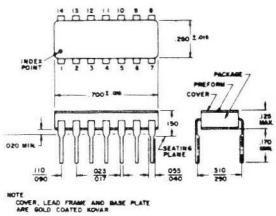
(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−1.5	—	−5.0	Volts	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$, $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current	—	−.10	−3.0	nA	$V_{DS} = -20V$ $V_{GSB} = 0$
I_{SDS}	Source Leakage Current (Total for all Units)	—	−0.6	−12	nA	$V_{SD} = -20V$, $V_{GDB} = 0$
I_{GSS}	Gate Leakage Current	—	−0.1	−1.0	nA	$V_{GS} = -20V$, $V_{DSB} = 0$
$I_{D(ON)}$	Drain Current	−3.0	−6.0	—	mA	$V_{GS} = V_{DS} = -10V$, $V_{BS} = 0V$
BV_{DSS}	Drain—Source Breakdown	−35	—	—	Volts	$I_D = -10\ \mu A$, $V_{GSB} = 0V$
BV_{SDS}	Source—Drain Breakdown	−35	—	—	Volts	$I_S = -10\ \mu A$, $V_{GDB} = 0V$
BV_{GSS}	Gate—Source Breakdown	−40	—	−80	Volts	$I_G = -10\ \mu A$, $V_{DSB} = 0V$
Y_{fs}	Transadmittance	—	2500	—	μmho	1 kHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate To Source Capacitance	—	3.0	6.0	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{gd}	Gate To Drain Capacitance	—	1.9	3.5	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{ds}	Drain To Source Capacitance	—	0.04	0.10	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain To Source On Resistance	—	150	350	Ohms	$V_{GS} = -20V$, $I_D = -100\ \mu A$ $V_{BS} = 0V$

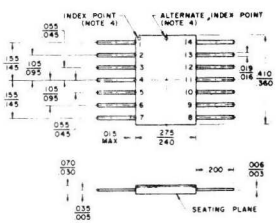
P 14 LEAD PLASTIC



D 14 LEAD CERAMIC DIP



F 14 LEAD FLAT PACK



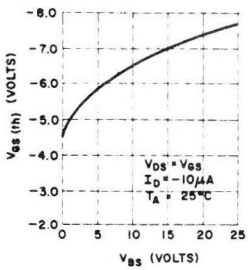
All dimensions in inches

TERMINALS

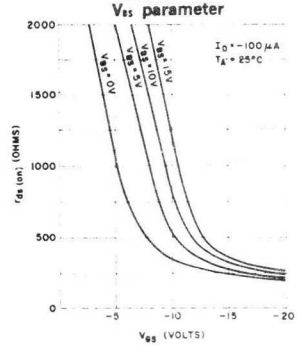
PIN	FUNCTION	PIN	FUNCTION
1	Gate 1	8	Substrate
2	Gate 2	9	Drain 6
3	Gate 3	10	Drain 5
4	Gate 4	11	Drain 4
5	Gate 5	12	Drain 3
6	Gate 6	13	Drain 2
7	Source	14	Drain 1

TYPICAL CHARACTERISTIC CURVES

$V_{GS(th)}$ vs. V_{BS}

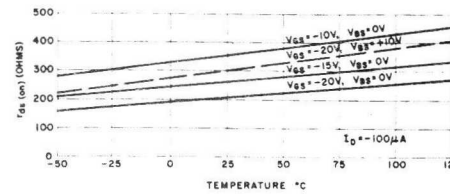


$r_{ds(on)}$ vs. V_{GS} V_{BS} parameter

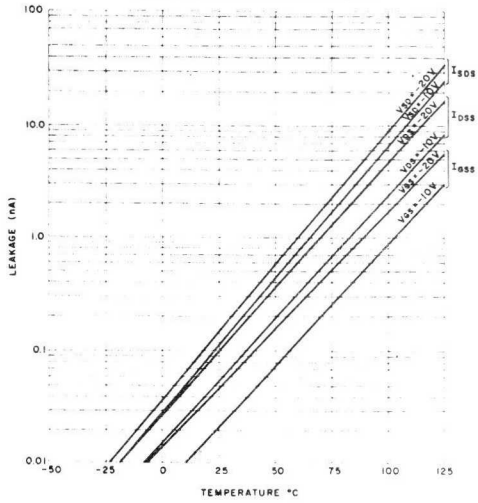


$r_{ds(on)}$ vs. TEMPERATURE

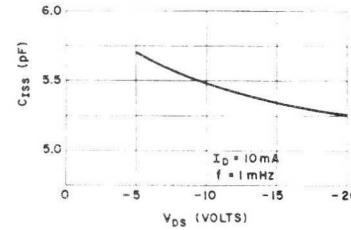
V_{GS}, V_{BS} parameter



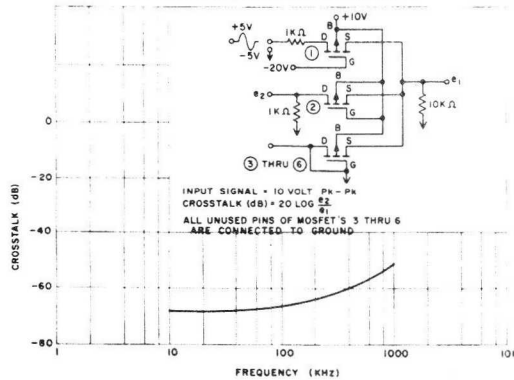
LEAKAGE vs. TEMPERATURE



INPUT CAPACITANCE vs. V_{DS}

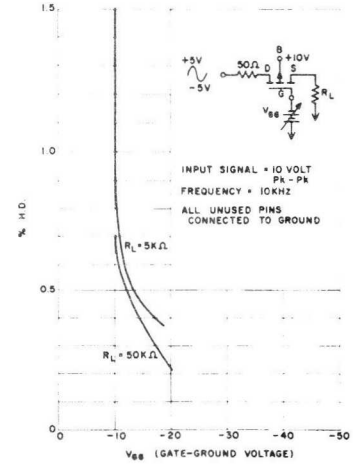


CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GG}

R_L parameter



INDUSTRIAL/ MOSFET

MEM 856P/D/F

Six Channel MOSFET Analog Switch

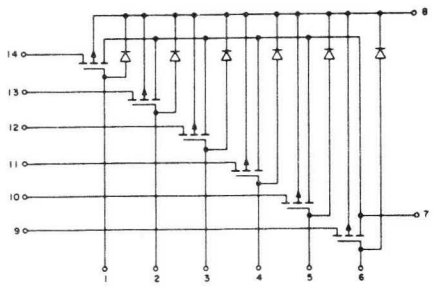
FEATURES

- Low input capacitance
- 40 volt peak-peak signal input range
- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- High Drain, Source and Gate Breakdown Voltages
- Low harmonic distortion

APPLICATIONS

- Analog Multiplexing
- Time division multiplexing
- Chopping
- Serial to parallel & parallel to serial converter

CIRCUIT DIAGRAM



MAXIMUM RATINGS

($T_A = 25°C$, unless otherwise specified — body grounded)

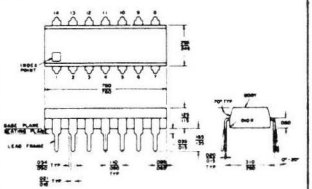
Drain to Source Voltage	—80V
Gate to Source Voltage	—80V
Gate to Drain Voltage	—80V
Drain Current	—20mA
Gate Current (forward direction for zener clamp)	+0.1mA
Storage Temperature	—65 to 150°C
Operating Junction Temperature (856P)	—65 to 85°C
Operating Junction Temperature (856 D/F)	—65 to 125°C
Total dissipation at 25°C Ambient Temperature	300mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	50mW

ELECTRICAL CHARACTERISTICS

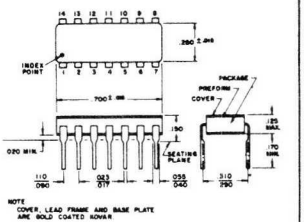
($T_A = 25°C$, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	—3.0	—	—6.0	Volts	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$, $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current	—	—.05	—0.5	nA	$V_{DS} = -20V$, $V_{GSB} = 0$
I_{SDS}	Source Leakage Current (Total for all Units)	—	—0.2	—2.0	nA	$V_{SD} = -20V$, $V_{GDB} = 0$
I_{GSS}	Gate Leakage Current	—	—0.1	—0.5	nA	$V_{GS} = -20V$, $V_{DSB} = 0$
$I_{D(ON)}$	Drain Current	—1.0	—3.0	—	mA	$V_{GS} = V_{DS} = -10V$, $V_{BS} = 0V$
BV_{DSS}	Drain—Source Breakdown	—50	—65	—80	Volts	$I_D = -10\ \mu A$, $V_{GSB} = 0V$
BV_{SDS}	Source—Drain Breakdown	—50	—60	—80	Volts	$I_S = -10\ \mu A$, $V_{GDB} = 0V$
BV_{GSS}	Gate—Source Breakdown	—50	—70	—80	Volts	$I_G = -10\ \mu A$, $V_{DSB} = 0V$
Y_{fs}	Transadmittance	—	700	—	μmho	1 kHz, $V_{DS} = -20V$, $I_D = -5mA$, $V_{BS} = 0V$
C_{gs}	Gate To Source Capacitance	—	0.2	0.5	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{gd}	Gate To Drain Capacitance	—	0.2	0.5	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
C_{ds}	Drain To Source Capacitance	—	0.04	0.10	pF	1 MHz, $V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain To Source On Resistance	—	700	1000	Ohms	$V_{GS} = -20V$, $I_D = -100\ \mu A$, $V_{BS} = 0V$

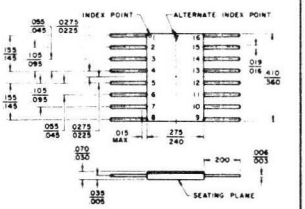
P 14 LEAD PLASTIC



D 14 LEAD CERAMIC DIP



F 14 LEAD FLAT PACK



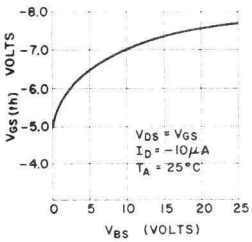
All dimensions in inches

TERMINALS

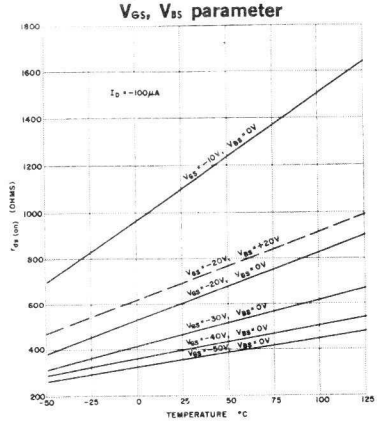
PIN	FUNCTION	PIN	FUNCTION
1	Gate 1	8	Substrate
2	Gate 2	9	Drain 6
3	Gate 3	10	Drain 5
4	Gate 4	11	Drain 4
5	Gate 5	12	Drain 3
6	Gate 6	13	Drain 2
7	Source	14	Drain 1

TYPICAL CHARACTERISTIC CURVES

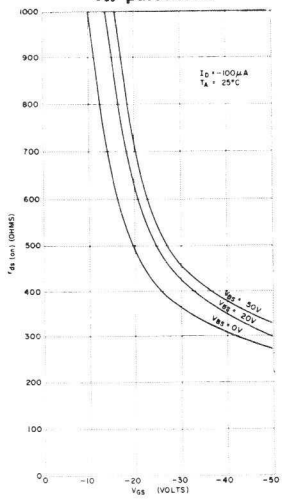
$V_{GS(th)}$ vs. V_{BS}



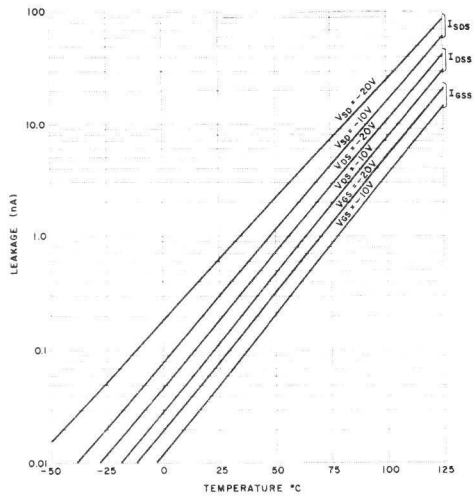
$r_{ds(on)}$ vs. TEMPERATURE
V_{GS}, V_{BS} parameter



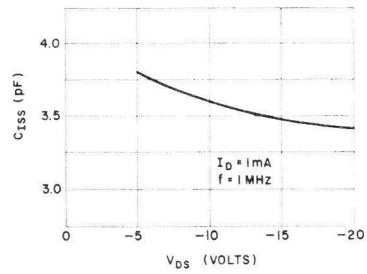
$r_{ds(on)}$ vs. V_{GS}
V_{BS} parameter



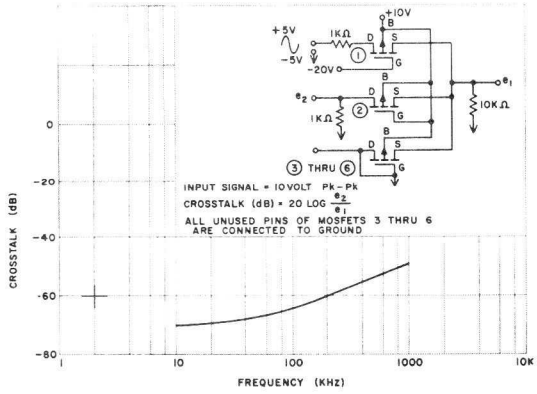
LEAKAGE vs. TEMPERATURE



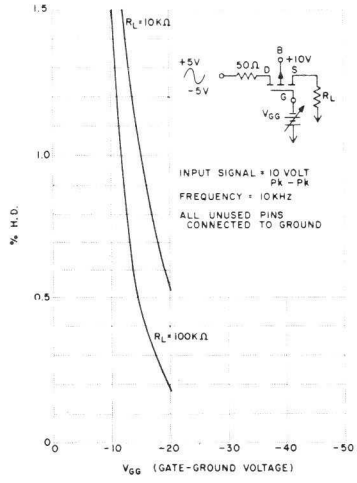
INPUT CAPACITANCE vs. V_{DS}



CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GG}
R_L parameter



MEM 857P/D/F

Eight Channel MOSFET Analog Switch

FEATURES

- 25 Volt Peak-Peak Signal Input Range
- Low Threshold
- 10^{10} Ohms Input Resistance
- Integrated Zener Clamp Protection
- Normally Off with Zero Gate Voltage
- Square Law Linear Transfer Characteristics
- Low Crosstalk
- Low Leakage Presented to the Summing Junction
- Low "ON" Resistance
- Low Harmonic Distortion
- Less Than a 20 Ohm Change of "ON" Resistance from Channel to Channel

APPLICATIONS

Analog Multiplexing
Time Division Multiplexing
Chopper
Serial to Parallel & Parallel to Serial Converter
4-channel Differential Switch

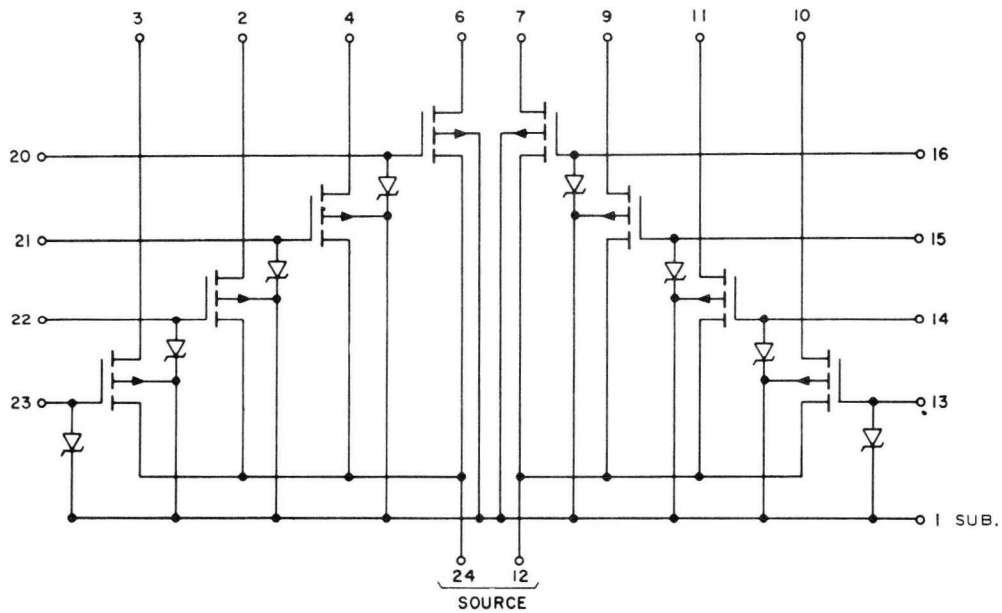
DESCRIPTION

This multiple switch contains 8 nitride passivated insulated gate field effect transistors. The sources are connected in such a way as to afford maximum flexibility for switching applications.

By properly biasing the devices, they can be used either as multiple switches, rotary switches, "AND" gates or "NOR" gates.

The nitride passivation process enables this device to have a low threshold voltage capability.

CIRCUIT DIAGRAM



MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

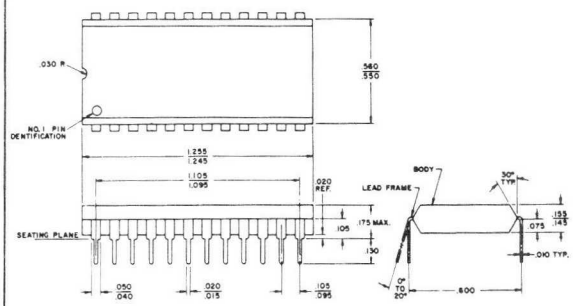
Drain to Source Voltage	−30V
Gate to Source Voltage	−30V
Gate to Drain Voltage	−30V
Drain Current	50mA
Gate Current (forward direction for zener clamp)	+0.1mA
Storage Temperature	−65°C to 150°C
Operating Junction Temperature (857P)	−65°C to 85°C
Operating Junction Temperature (857 D/F)	−65°C to 125°C
Total Dissipation at 25°C Ambient Temperature	1.75W
Total Dissipation at 25°C Ambient Temperature for each gate circuit	175mW

ELECTRICAL CHARACTERISTIC

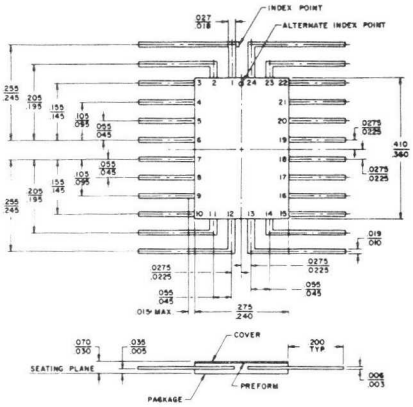
(T_A = 25°C unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate-Source Cutoff Voltage	1.5	—	4.5	Volts	$V_{DS} = V_{GS}$, $I_D = -10\mu A$, $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current	—	—	5	nA	$V_{DS} = -20V$, $V_{GSB} = 0$
I_{SDS} S1-4 S5-8	Source Leakage Current	—	—	20 20	nA	$V_{SD} = -20V$, $V_{GDB} = 0$
I_{GSS}	Gate Leakage Current	—	—	1	nA	$V_{GS} = -20V$, $V_{DSB} = 0$
$I_{D(on)}$	Drain Current	10	—	—	mA	$V_{DS} = V_{GS} = -10V$, $V_{BS} = 0$
BV_{DSS}	Drain-Source Breakdown Voltage	30	—	—	Volts	$I_{DS} = -10\mu A$, $V_{GSB} = 0$
BV_{SDS}	Source-Drain Breakdown Voltage	30	—	—	Volts	$I_{SD} = -10\mu A$, $V_{GDB} = 0$
BV_{GSS}	Gate-Source Breakdown Voltage	30	—	—	Volts	$I_{GS} = -10\mu A$, $V_{DSB} = 0$
Y_{fs}	Transadmittance	1500	—	—	μmhos	$V_{DS} = -10V$, $I_D = -5mA$, f = 1kHz, $V_{BS} = 0$
C_{gs}	Gate-Source Capacitance	—	1.5	2.5	pF	$V_{GS} = V_{DS} = -10V$, f = 1MHz
C_{gd}	Gate-Drain Capacitance	—	1.0	2.0	pF	$V_{GS} = V_{DS} = -10V$, f = 1MHz
C_{ds}	Drain-Source Capacitance	—	0.04	0.10	pF	$V_{GS} = V_{DS} = -10V$, f = 1MHz
$r_{DS(on)}$	Drain-Source On Resistance	—	—	150	Ohms	$V_{GS} = -20V$, $I_D = -100\mu A$, $V_{BS} = 0$

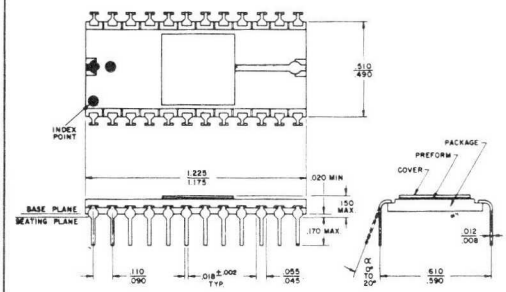
P 24 LEAD PLASTIC



F 24 LEAD FLAT PACK



D 24 LEAD CERAMIC DIP

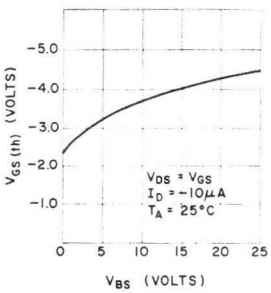


TERMINALS

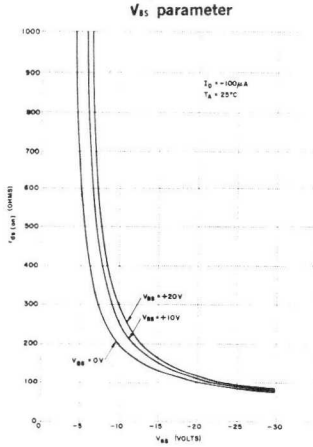
PIN	FUNCTION	PIN	FUNCTION
1	Substrate	13	Gate 10
2	Drain 2	14	Gate 9
3	Drain 1	15	Gate 8
4	Drain 3	16	Gate 7
5	Drain 4	17	Gate 6
6	Drain 5	18	Source 5-6
7	Drain 6	19	Gate 5
8	Drain 7	20	Gate 4
9	Drain 8	21	Gate 3
10	Drain 10	22	Gate 2
11	Drain 9	23	Gate 1
12	Source 7-10	24	Source 1-4

TYPICAL CHARACTERISTIC CURVES

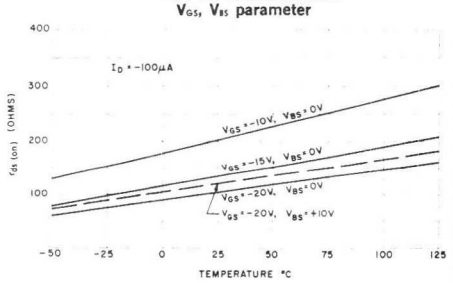
$V_{GS(th)}$ vs. V_{BS}



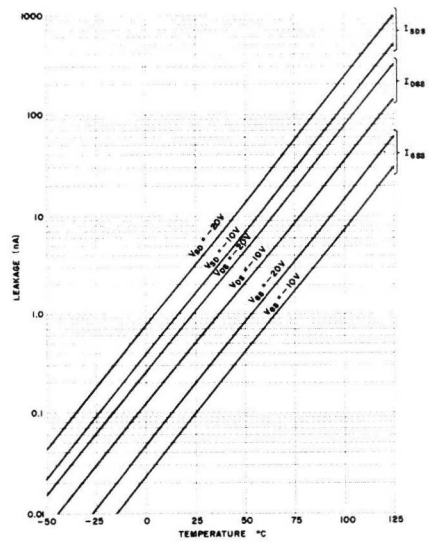
$r_{ds(on)}$ vs. V_{GS}
V_{BS} parameter



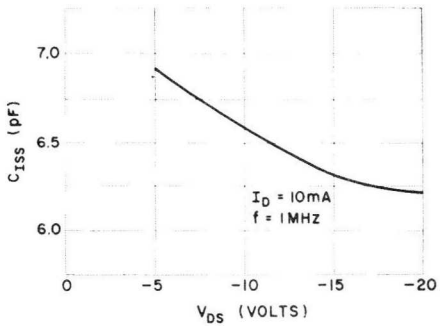
$r_{ds(on)}$ vs. TEMPERATURE
V_{GS}, V_{BS} parameter



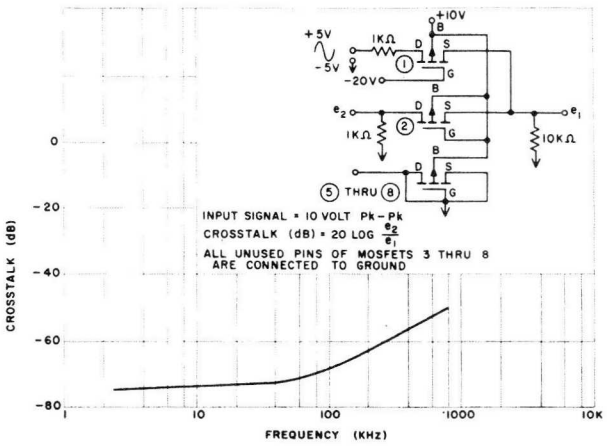
LEAKAGE vs. TEMPERATURE



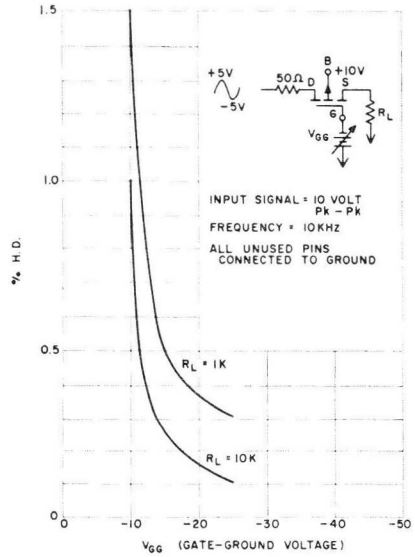
INPUT CAPACITANCE vs. V_{DS}



CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GG}
R_L parameter



INDUSTRIAL/ MOSFET

Four Channel Analog Switch Driver

FEATURES

- Wide range of input and output levels. Input 3 to 15V, output to 15V p-p
- Low quiescent power dissipation
- High switching speeds
- Excellent driving capability
- Inhibit input, providing an additional level of logic control

APPLICATIONS

- TTL to MOS logic level converter
- Driver for analog switches and multiplexers

DESCRIPTION

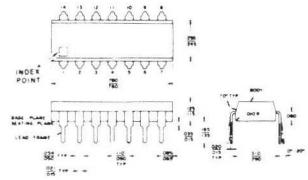
MEM 4900 consists of four independent drivers on a monolithic silicon chip. Each driver will accept input signal amplitudes of 3 to 15V and supplies output signal amplitudes of 15V p-p. For example, if $V_{DD} = +10V$, $V_{SS} = 0V$, and $V_{EE} = -5V$ output signals from −5V to +10V will be generated by an input swing of 0 to 3V. An inhibit control is also provided which when it is "HIGH", all four drivers are disabled.

The driver circuits dissipate very low quiescent power over the full supply voltage ranges and they also exhibit excellent driving capability and very high switching speeds.

MAXIMUM RATINGS ($T_A = 25°C$)

Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
D.C. Supply Voltages — $V_{DD} - V_{SS}$ ..... +15V to −0.5V
$V_{DD} - V_{EE}$ ..... +15V to −0.5V
Inputs ($V_{SS} \leq V_{IN} \leq V_{DD}$) — Logic "1" ..... 2.8V to V_{DD}
Logic "0" ..... −0.2 to +0.3V
Minimum recommended supply voltages — $V_{DD} - V_{SS}$ 5V
$V_{DD} - V_{EE}$ 5V

P 14 LEAD PLASTIC



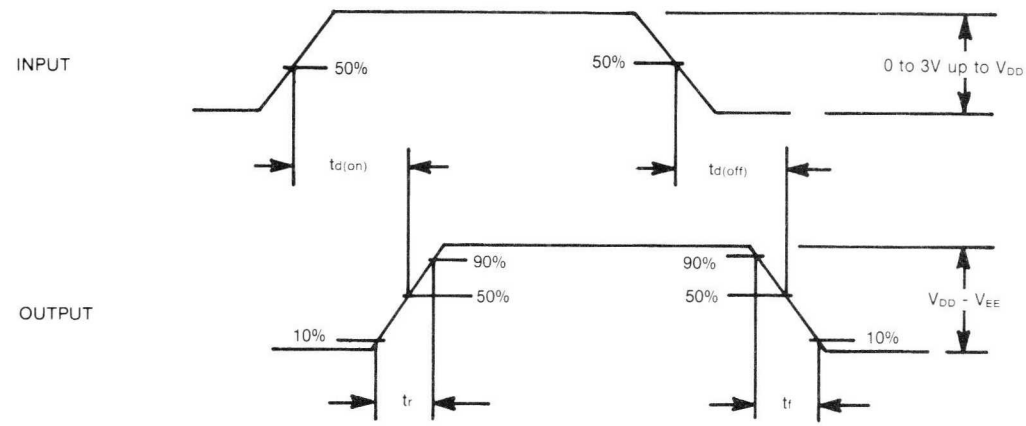
LEAD CONFIGURATION

Pin	Function	Pin	Function
1	Ch. 1 Input	8	Ch. 3 Input
2	Ch. 1 Output	9	Ch. 3 Output
3	$-V_{EE}$	10	$-V_{EE}$
4	Ch. 2 Output	11	Ch. 4 Output
5	Ch. 2 Input	12	Ch. 4 Input
6	Inhibit Input	13	Open
7	V_{SS} (GND)	14	$+V_{DD}$

ELECTRICAL CHARACTERISTICS (@T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent power dissipation per package	P_T	—	2.5	—	uw	V_{DD}=+5V, V_{EE}=−5V, V_{SS}=GND
Average input capacitance	C_I	—	6	—	pF	V_{DD}=+5V, V_{EE}=−5V, V_{SS}=GND
Average output capacitance	C_O	—	8	—	pF	V_{DD}=+5V, V_{EE}=−5V, V_{SS}=GND
Output current	I_O					
V_O = High		—	5	—	mA	V_{DD} — V_{EE}=+10V
V_O = Low		—	12	—	—	V_{SS}=GND
Propagation delay on	$t_{d(on)}$	—	180	—	nsec	V_{DD}=+10V, V_{EE}=V_{SS}=GND,
Propagation delay off	$t_{d(off)}$	—	180	—	nsec	V_{in}=0-3V @ f=500kHz
Output rise time	t_r	—	30	—	nsec	C_L=100 pF
Output fall time	t_f	—	30	—	nsec	

SWITCHING WAVEFORMS



GENERAL INFORMATION 10

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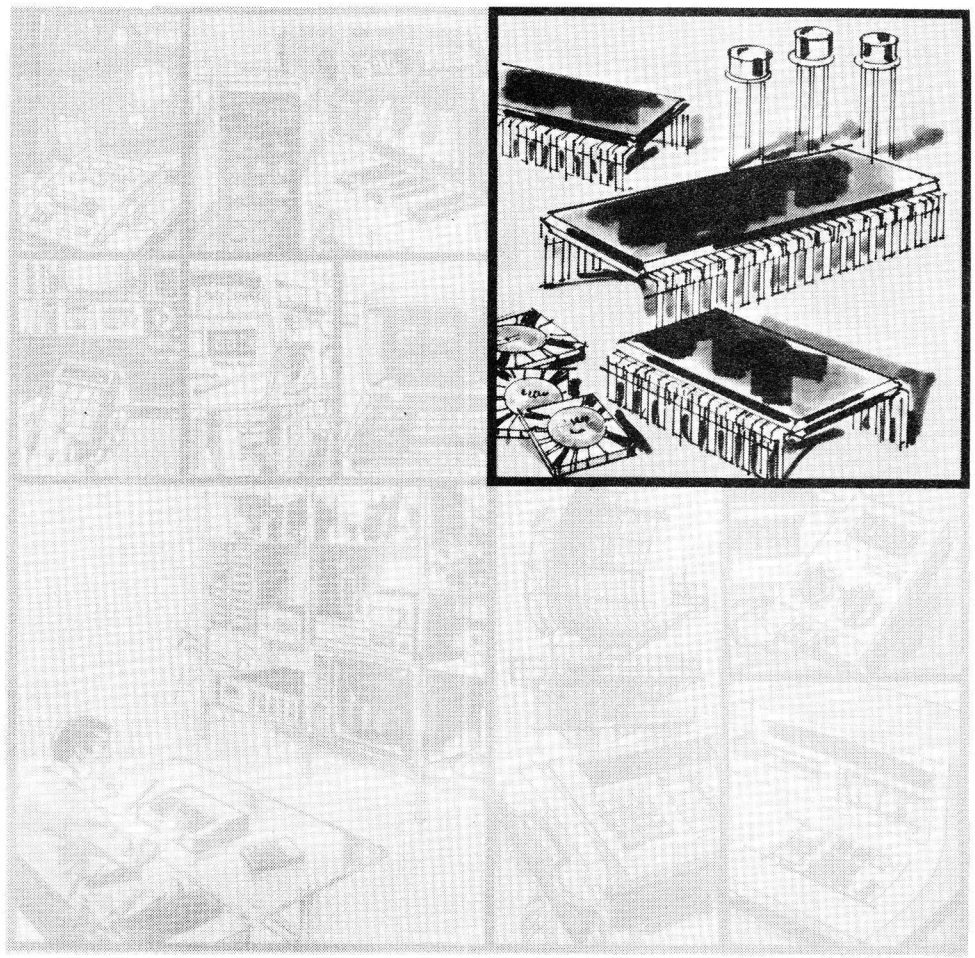
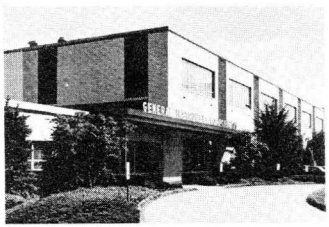
Package Outlines	10- 8
Sales Offices	10-13

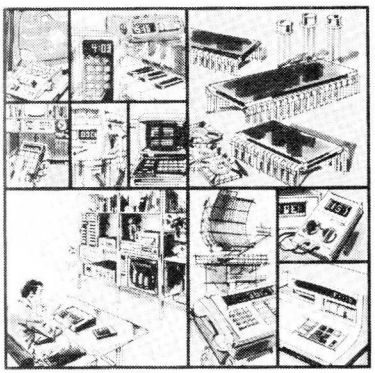


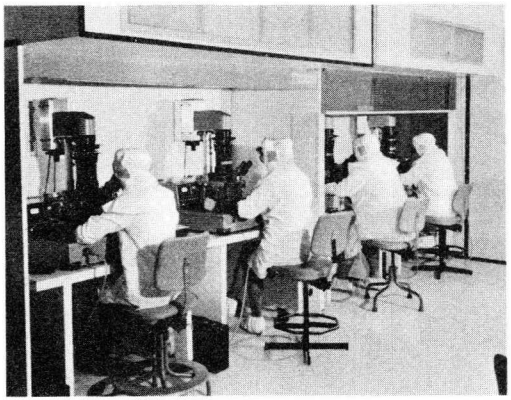
MICRO ELECTRONICS

A TOTAL TECHNOLOGICAL SERVICE

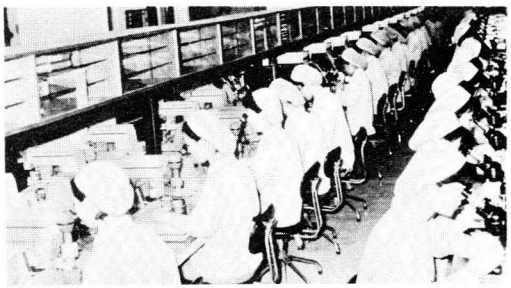


Hicksville, New York—
Microelectronics World Headquarters.





Glenrothes, Scotland—*Mask Aligners.*



Kaohsiung, Taiwan—*Assembly operation.*

MICRO ELECTRONICS

General Instrument Microelectronics is one of the world's leading manufacturers of LSI (Large Scale Integrated) microcircuits. A pioneer in MOS in 1966, General Instrument is now a worldwide source of microcircuits utilizing Hybrid, Bipolar and MOS technologies in service to the consumer, industrial and public service marketplaces.

General Instrument Microelectronics has facilities in every major market providing customers with a full spectrum of services including new product development... applications engineering...high volume circuit manufacturing...and immediate delivery of over 350 standard products "off the shelf."

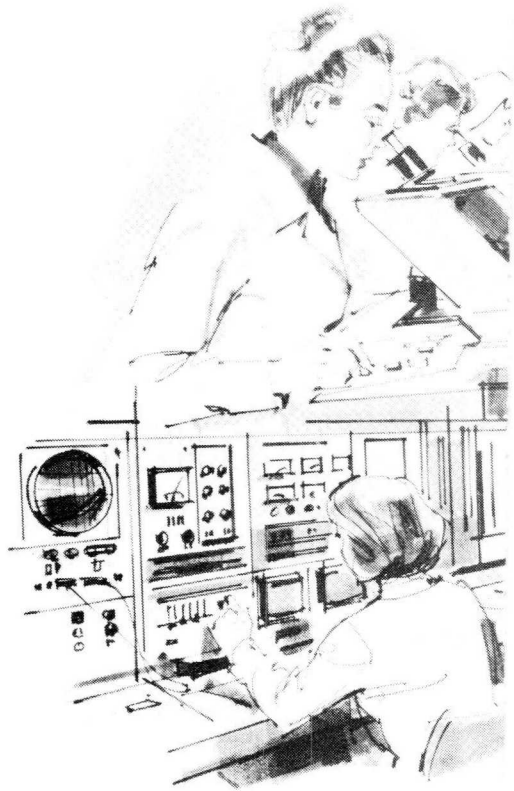
Strategically Located Plants

The Microelectronics Group operates four main production facilities in the United States, Europe and Far East. Plants at Glenrothes, Scotland; Chandler, Arizona; and Hicksville, New York, have complete capability for product design, mask making, diffusion, assembly, test and quality assurance. The factory in Kaohsiung, Taiwan, is dedicated to high volume assembly, test, quality assurance and applications of Microelectronics products.

In addition to providing reliable sources of supply on three continents, General Instrument operates each plant as a backup facility to the others, to insure uninterrupted delivery. Common processes and equipment are employed and major product styles are always produced in at least two separate locations. To maintain uniform standards from plant to plant, the quality assurance and process control groups at each facility are directed by quality control policy established at Group and Corporate levels.

Product Quality

With a major investment in product test and in-line quality control equipment, General Instrument Microelectronics is dedicated to delivery of complex integrated circuits to the incoming quality level and with the reliability its customers require. Many products routinely receive final test at elevated temperature and extensive burn-in facilities exist for 100% preshipment stress as well as confirmation of outgoing product quality.



Customer Service

General Instrument Microelectronics believes in CUSTOMER SERVICE. Customer Service departments are maintained at each major location to provide immediate response to questions concerning order service and delivery. Our customer service personnel are trained to consider our customers' needs as their most urgent requirement. Call on them and let us prove that we are dedicated to responsive service.

Advanced Design Centers

To provide our customers with the latest in LSI technology, General Instrument Microelectronics maintains R&D centers at Glenrothes, Scotland; Hicksville, New York; and Chandler, Arizona. In addition, the Microelectronics activity is supported by general research in various fields carried out with such prestigious organizations as the Massachusetts Institute of Technology and the University of Utah.

In addition to its extensive catalog of standard products, General Instrument Microelectronics is happy to provide custom design service to satisfy special requirements. In some cases, the application is best served by a software or firmware modification of one of our standard microprocessors. In other cases, a dedicated microprocessor is more cost effective. These services may be arranged through any of the Microelectronics sales offices.

Applications Assistance Around the Globe

To provide the special applications assistance that customers may require, General Instrument Microelectronics maintains fully staffed Applications Centers at strategic locations around the world...
U.S.A. — Hicksville, New York; Chandler, Arizona; and Los Angeles, California.
EUROPE — Glenrothes, Scotland; London, England; and Munich, Germany
ASIA — Kaohsiung, Taiwan; Tokyo, Japan; and Hong Kong

Arrangements can be made for immediate assistance from these centers by contacting any of the sales offices listed in this book.

Corporate Support
General Instrument Microelectronics is backed by the full resources of the General Instrument Corporation, which has for over 50 years been among the leaders in the application of modern technology to entertainment, industrial, military, data and communications electronics. The skills, production know-how, and technological capability of the entire General Instrument organization are utilized by the Microelectronics Group to further improve its products and customer services.

Among the many other electronic components manufactured by General Instrument are discrete semiconductors, relays, miniature lamps, and TV components. General Instrument is a leading manufacturer of cable TV products, off-track and on-track wagering systems, point-of-sale equipment and apparatus for defense applications.

CHICAGO MINIATURE LAMP WORKS

COMMERCIAL DATA SYSTEMS

JERROLD

F.W. SICKLES

SIGNALITE

ELECTRONIC SYSTEMS

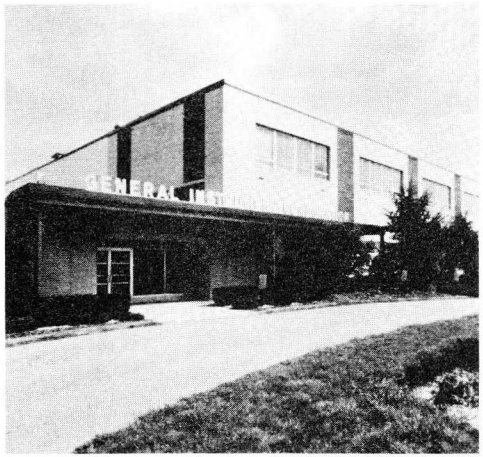
AMERICAN TOTALISATOR

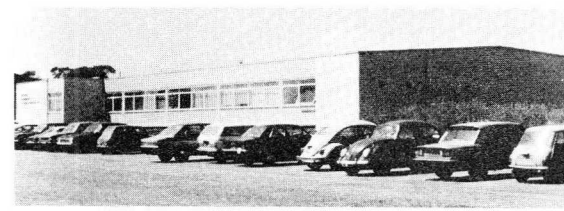
UNITOTE/REGITEL

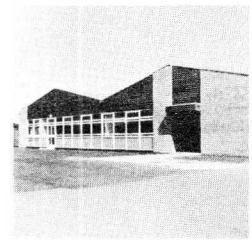
C.P. CLARE

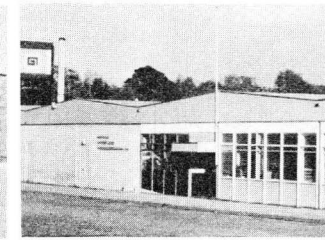
DISCRETE SEMICONDUCTOR

MANUFACTURING FACILITIES



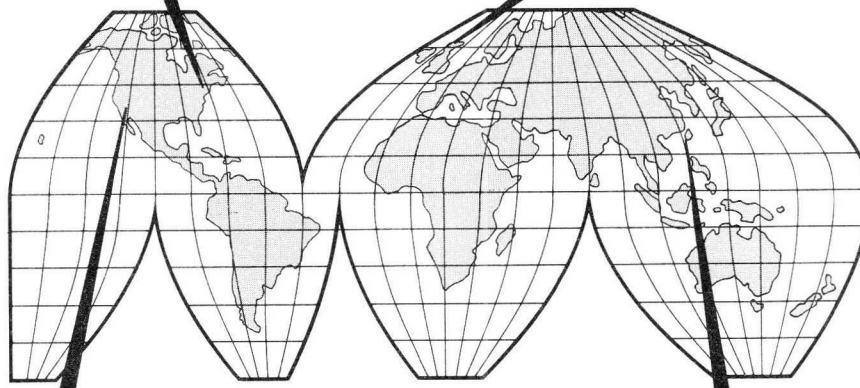






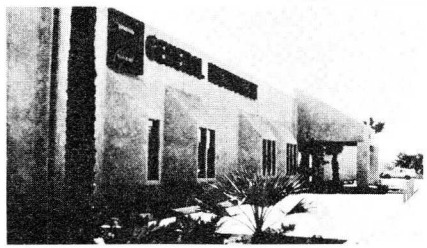
HICKSVILLE, NEW YORK

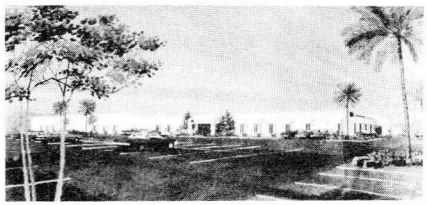
GLENROTHES, SCOTLAND

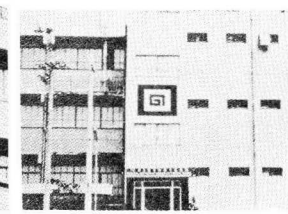


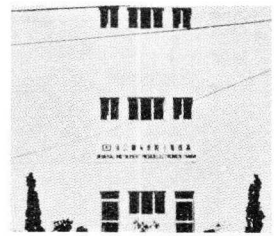
CHANDLER, ARIZONA

KAOHSIUNG, TAIWAN







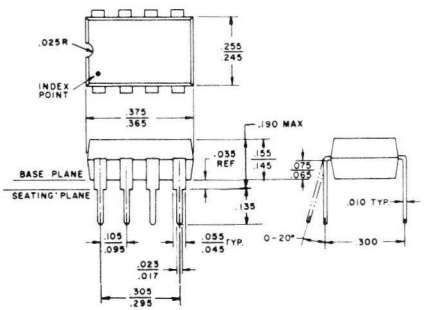


GENERAL INFORMATION

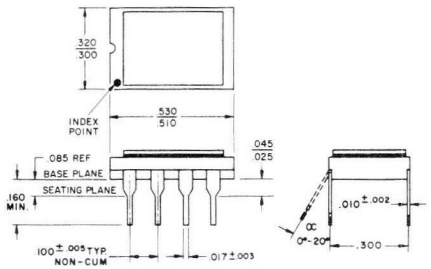
PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)

8 LEAD DUAL IN LINE

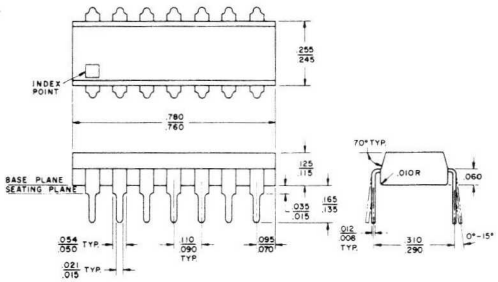


PLASTIC



CERAMIC

14 LEAD DUAL IN LINE



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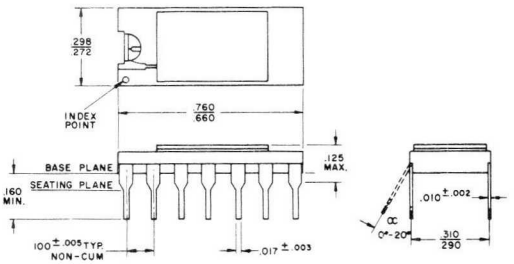
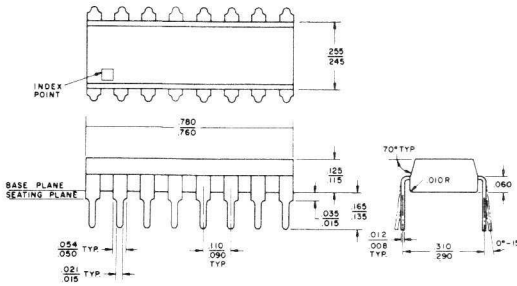


CERAMIC

PACKAGE OUTLINES (All dimensions in inches)

16 LEAD DUAL IN LINE



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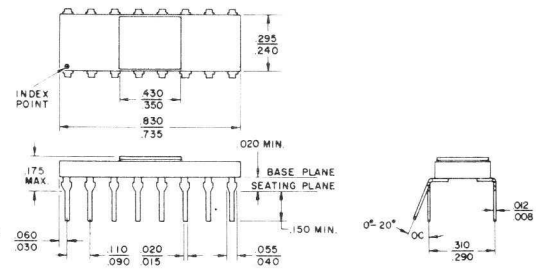

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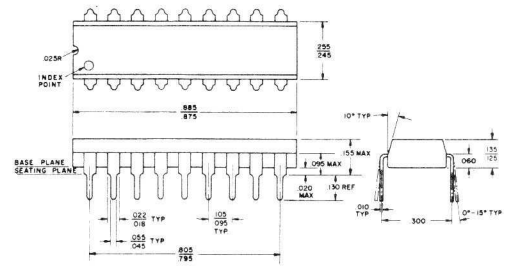

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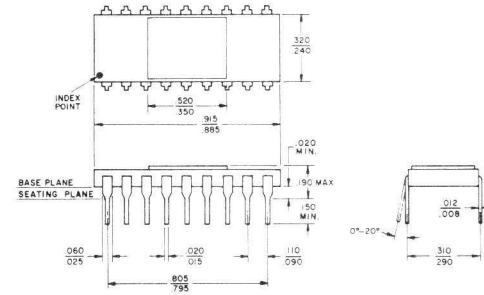

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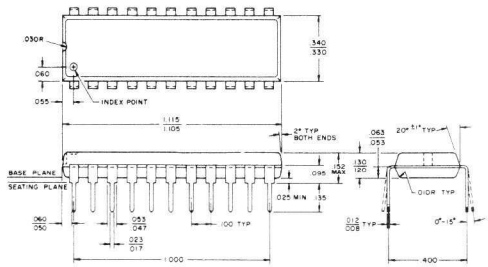

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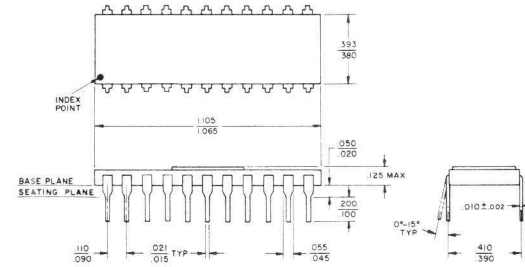


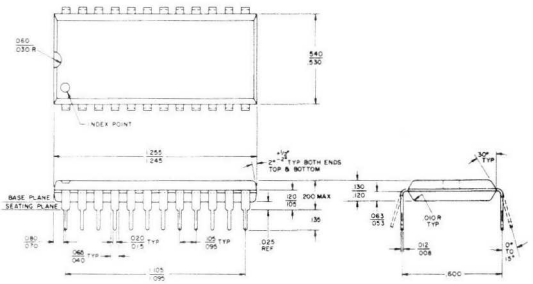
CERAMIC

GENERAL INFORMATION

PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)

24 LEAD DUAL IN LINE



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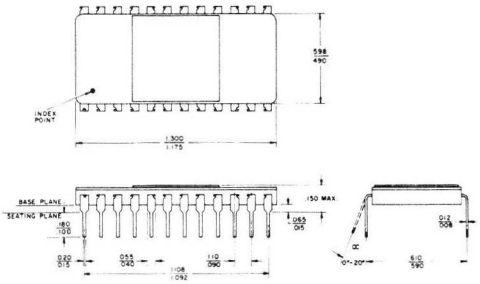
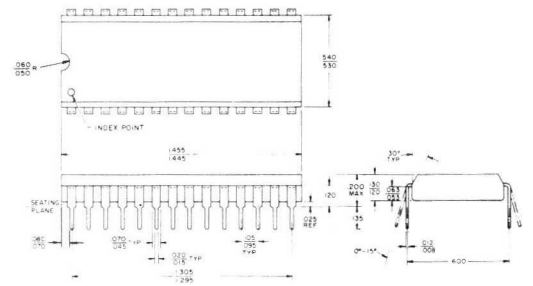


CERAMIC

28 LEAD DUAL IN LINE



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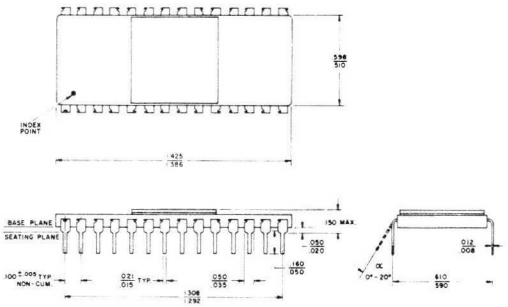

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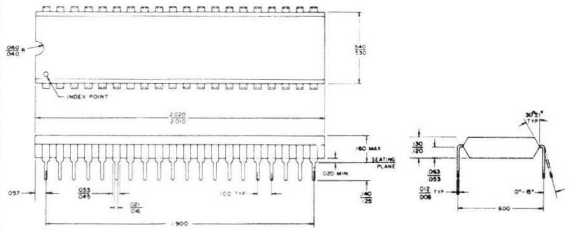

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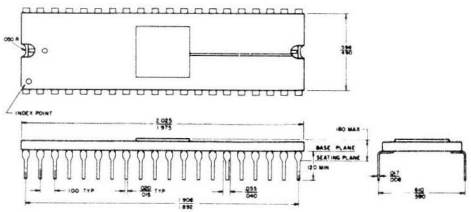
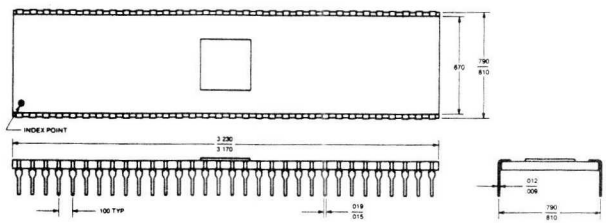


CERAMIC

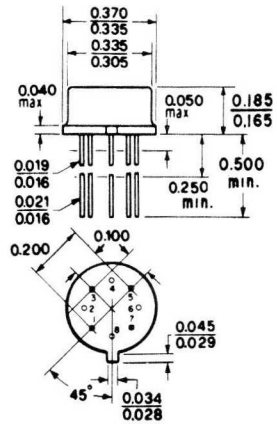
PACKAGE OUTLINES (All dimensions in inches)

64 LEAD DUAL IN LINE

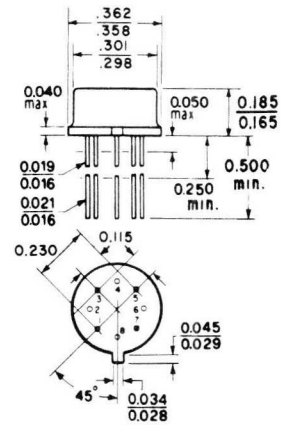


CERAMIC

8 LEAD TO-78



8 LEAD TO-99



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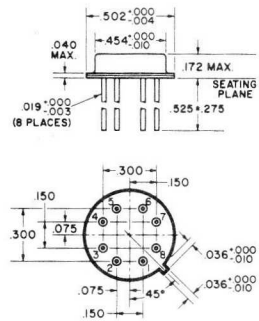
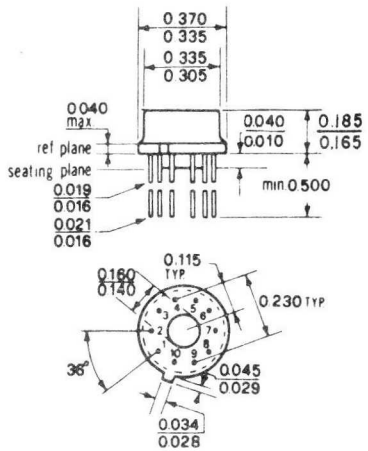


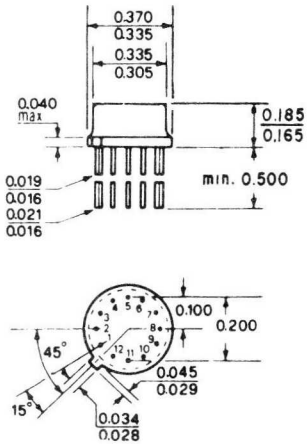
PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)

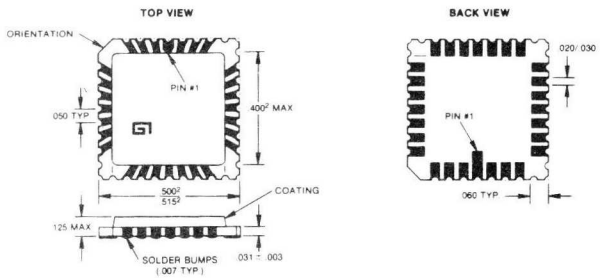
10 LEAD TO-100



12 LEAD TO-73



28 LEAD MINI-PAK



TERMS OF SALE

1. INVOICE TERMS

(a) All orders are subject to the final acceptance by Seller's credit department.

(b) All shipments are F.O.B., Seller's plant, unless otherwise stated hereon.

(c) The Seller reserves the right to make shipments in part or in whole, and the Seller's Invoices for such shipments shall be accepted and paid as rendered without regard to whether or not the balance of the order is shipped.

2. PRICES

(a) Prices are based upon shipments being made F.O.B. Seller's plants.

(b) Prices do not include any Municipal, State, or Federal sales, use, excise or similar taxes. Consequently, in addition to the prices specified, the amount of any present or future sales, use, excise, or any other tax that may be imposed shall be paid by the Purchaser, or in lieu thereof the Purchaser will provide the Seller with a tax exemption certificate acceptable to the taxing authorities.

(c) The price of the merchandise covered by this order is based upon the Seller's interpretation of the Purchaser's specifications.

(d) The Seller reserves the right to invoke a minimum billing charge of $100.00.

(e) Seller reserves the right to invoke a minimum cancellation charge of $50.00.

3. DELIVERY SCHEDULE

(a) Dates of shipment are approximate and are subject to the Seller's ability to conform to same, but Seller shall not incur any liability, consequential or otherwise, due to delay or failure to deliver for any reason. All orders are accepted subject to delays occasioned by labor, strikes, fires, war, or floods, accidents at factory, or any causes whatever beyond the Seller's control. Delivery schedules are predicated upon the Seller's ability to acquire materials, tools, dies and equipment, where necessary. In the event of any such delay beyond the Seller's control, the date of delivery of this order shall be extended by a period approximately equal to the time lost by reason of the delays.

(b) If the Seller does not receive a schedule from the Purchaser promptly, the rate and schedule of shipments will be set by the Seller.

(c) Subject to change, based upon delay in prompt receipt of approval of sample.

(d) Subject to change upon any modification of specifications previously agreed upon, or delay in submission of specification acceptable to Seller.

(e) Seller reserves the right to overship or undership a quantity totalling 5% of the last scheduled release of any order for non-standard parts.

4. SHIPMENT

(a) Unless specified the Seller will select the mode of transportation and the Seller will not be responsible for differences in cost between one mode and another.

(b) The Seller is not responsible for damage or loss in transit and any such claims are to be placed by the Purchaser with the carrier, where shipment is made F.O.B. Seller's plant.

5. INSPECTION AND ACCEPTANCE

(a) It is understood that the conditions of the Purchaser's inspection or test of the material covered by this order shall be mutually agreed upon and the Seller reserves the right to inspect any material which the Purchaser claims to be defective on the Purchaser's premises and decide whether or not it should be replaced. Any required repairs which the Seller's inspection determines to be the Purchaser's responsibility will be made at the Purchaser's expense and at the Seller's option on the Purchaser's premises.

(b) If the material covered by this order is proven defective and the Seller was notified of such defects in writing within twenty days from the date of shipment, the Seller will be responsible only for the costs of repair or replacement of the Seller's product, and in no event will Seller be liable for any damage consequential or otherwise or for an amount in excess of the price (at the time of adjustment) of the defective item(s). The Seller will not be responsible for any charges resulting from the use of defective material.

(c) No material may be returned for credit and no material may be returned to the Seller for correction without the Seller's prior written approval, but if such unauthorized return shipments are made to the Seller, the Seller reserves the right to refuse the shipment or to accept it, and in the latter case, the shipment will be held as the Purchaser's property and without responsibility to the Seller.

(d) All claims, including claims for shortages must be made within five (5) days after receipt of shipment, except as otherwise contained in this Terms of Sale.

6. TOOLS

Payment of the Seller's charges for tools, dies, jigs, fixtures, etc. and/or equipment required for the production of this or other orders does not convey ownership of such items to the Purchaser nor the right to remove them from the Seller's plant, as such charges do not represent prices that would be charged for the sale of such items and oftentimes represent the costs of modifications and/or additions to standard tools or equipment.

7. CANCELLATION

Cancellation of this order for any reason whatsoever will be accepted only upon terms that will fully indemnify the Seller.

8. REMEDIES OF THE SELLER

(a) If, at the Purchaser's request or for any other reason for which the Purchaser is responsible, production or shipment of this order is held or delayed, the Seller reserves the right to immediately invoice the Purchaser for same in accordance with the provisions of Clause 7 above and payment is to be made promptly in accordance with this Terms of Sale. Should the Purchaser release the hold or remove the cause for delay and the Seller agrees to reinstate the order, the schedule of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(b) If, in the Seller's judgment, the Purchaser's financial condition at any time does not justify continuance of production or shipment of the material covered by this or any other of the Purchaser's orders, the Seller reserves the right to require full or partial payment in advance and/or to withhold further shipments and stop production, in which case the conditions of Cancellation Clause 7 above will apply.

(c) If payment of the Seller's invoice(s) for shipments in part or in whole is not made promptly and in compliance with this Terms of Sale above, the Seller reserves the right to withhold further shipments and/or stop production and, at the Seller's option, to require full payment in accordance wih Clause 7 of this Terms of Sale. If, as a result of the purchaser's failure to pay the Seller's invoice(s) promptly, the Seller stops production of this order and later agrees to reinstate it, the scheduled rate of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(d) If at any time prior to the date of initial production and/or shipment, of this order or at any subsequent time during the course of this order, there shall be filed by or against the Purchaser in any Court, pursuant to any statute either of the United States or of any State or Municipality a petition of bankruptcy or insolvency, or for reorganization, or for the appointment of a receiver or trustee of all or a portion of the Purchaser's property, or if the Purchaser makes an assignment for the benefit of creditors, this order shall ipso facto be cancelled and terminated and, in which event, neither the Purchaser nor any person claiming through or under the Purchaser or by virtue of any statute or an order of any Court shall be entitled to any rights of the Purchaser's order and the Seller reserves the right to impose all applicable conditions of this Terms of Sale, including Cancellation Clause 7 above, as well as to retain as partial liquidated damages any payments, security, deposits or monies received by the Seller from the Purchaser or others in the Purchaser's behalf against this order. Should the receiver, trustee, the operating committee, or other similar agency desire to reinstate this order or any uncompleted portion thereof, the Seller reserves the right to either refuse or accept such requests for reinstatement and, in the latter case, to determine what appropriate credits, if any, are to be issued to offset charges previously made as herein above in this clause provided for. If the Seller elects to reinstate the order it is subject to this Terms of Sale and the schedule and rate of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(e) If the Seller accepts notes, trade acceptances or other paper as part or entire payment for this order, all shall become due at the Seller's option, upon default in the payment of any one of them, and the Seller reserves the right to impose the conditions of Cancellation Clause 7 above.

9. The terms and conditions of this order acknowledgment supersede the Purchaser's order, and no variation of this agreement shall be valid unless same be in writing signed by a duly authorized officer of the Seller.

10. General Instrument Corporation, warrants its devices against defects in material and workmanship for a period of ninety (90) days in the case of entertainment type devices, or one (1) year in case of all other devices, from the date of shipment provided they are used within their voltage and current limits and under conditions specified by General Instrument Corporation. Adjustments if any are subject to clauses 5(a), (b), and (c) of the Seller's Standard Terms of Sale, and devices returned to factory for adjustment must be shipped with all transportation charges prepaid.

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